Switching (60V, 200mA)

SM6K2

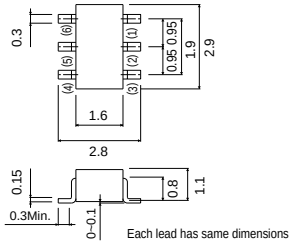
●Features

1) Two RHU002N06 chips in a SMT package.
2) Mounting possible with SMT3 automatic mounting machines.
3) Transistor elements are independent, eliminating interference.
4) Mounting cost and area can be cut in half.

●Structure

Silicon N-channel
MOSFET transistor

●External dimensions (Units : mm)

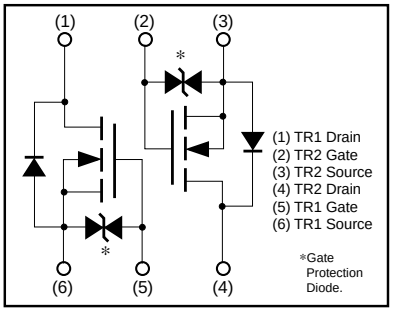


ROHM : SMT6
EIAJ : SC-74
JEDEC : SOT-457

Abbreviated symbol : K2

The following characteristics apply to both Tr1 and Tr2.

●Equivalent circuit



* A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use.
Use the protection circuit when fixed voltages are exceeded.

●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	60	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	200	mA
	Pulsed	I_{DP}*1	800	mA
Drain reverse current	Continuous	I_{DR}	200	mA
	Pulsed	I_{DRP}*1	800	mA
Total power dissipation		P_D*2	200	mW
Channel temperature		Tch	150	°C
Storage temperature		Tstg	−55~+150	°C

*1 Pw≤10μs, Duty cycle≤1%
*2 When using 1×0.75×0.062 inch glass epoxy board.

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate leakage current	I_{GSS}	–	–	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	60	–	–	V	I_D=10μA, V_{GS}=0V
Drain cutoff current	I_{DSS}	–	–	1	μA	V_{DS}=60V, V_{GS}=0V
Gate threshold voltage	$V_{GS\,(th)}$	1	–	2.5	V	V_{DS}=10V, I_D=1mA
Drain-source on-state resistance	$R_{DS\,(on)}$*1	–	1.7	2.4	Ω	I_D=200mA, V_{GS}=10V
		–	2.8	4.0		I_D=200mA, V_{GS}=4V
Forward transfer admittance	$\|Y_{fs}\|$*1	100	–	–	mS	V_{DS}=10V, I_D=200mA
Input capacitance	C_{iss}	–	15	–	pF	V_{DS}=25V V_{GS}=0V f=1MHz
Output capacitance	C_{oss}	–	8	–	pF	
Reverse transfer capacitance	C_{rss}	–	4	–	pF	
Turn-on delay time	$t_{d\,(on)}$*2	–	6	–	ns	I_D=100mA, V_{DD}≒30V V_{GS}=10V R_L=300Ω R_{GS}=10Ω
Rise time	t_r*2	–	5	–	ns	
Turn-off delay time	$t_{d\,(off)}$*2	–	12	–	ns	
Fall time	t_f*2	–	95	–	ns	
Total gate charge	Q_g*2	–	2.2	4.4	nC	V_{DD}≒30V V_{GS}=10V I_D=200mA
Gate-source charge	Q_{gs}*2	–	0.6	–	nC	
Gate-drain charge	Q_{gd}*2	–	0.3	–	nC	

*1 Pw≤300μs, Duty cycle≤1%
*2 Pulsed

●**Packaging specifications**

	Package	Taping
	Code	T110
Type	Basic ordering unit (pieces)	3000
SM6K2		○

●**Electrical characteristic curves**

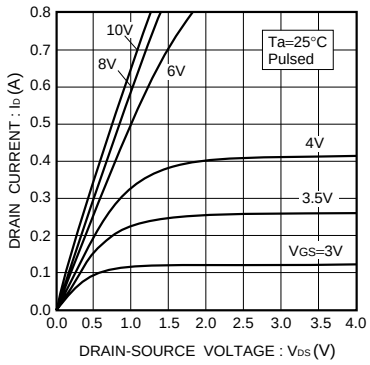


Fig.1 Typical output characteristics

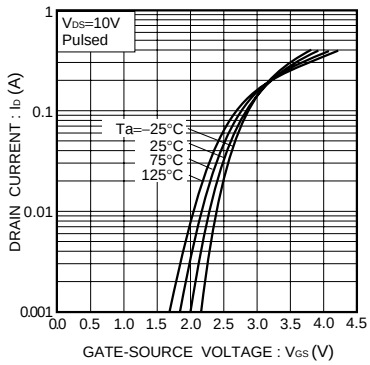


Fig.2 Typical transfer characteristics

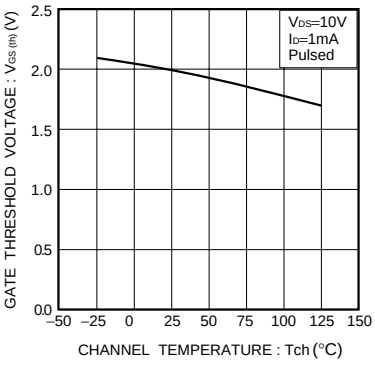


Fig.3 Gate threshold voltage vs. channel temperature

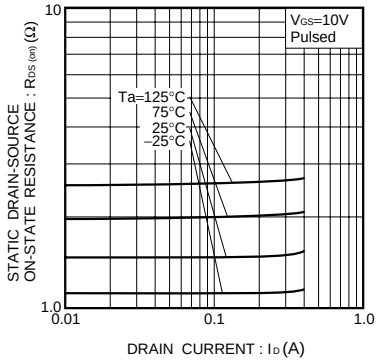


Fig.4 Static drain-source on-State resistance vs. drain current (I)

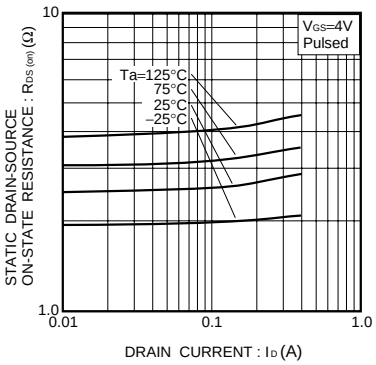


Fig.5 Static drain-source on-state resistance vs. drain current (II)

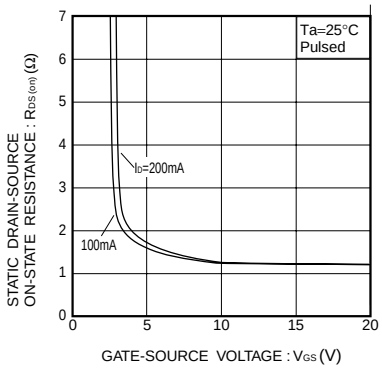


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

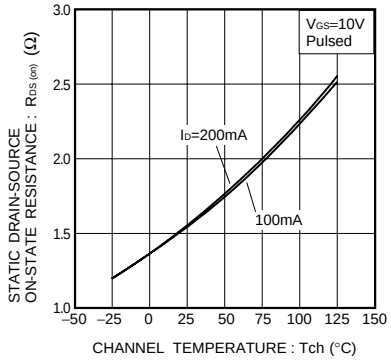


Fig.7 Static drain-source on-state resistance vs. channel temperature

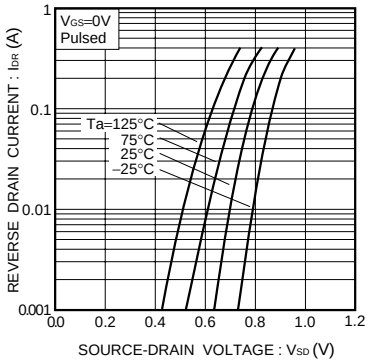


Fig.8 Reverse drain current vs. source-drain voltage (I)

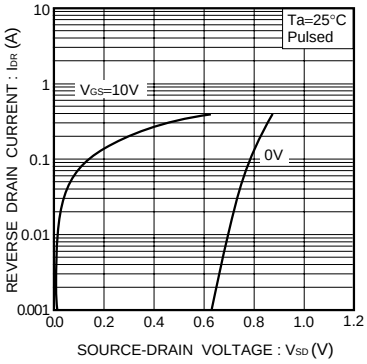


Fig.9 Reverse drain current vs. source-drain voltage (II)

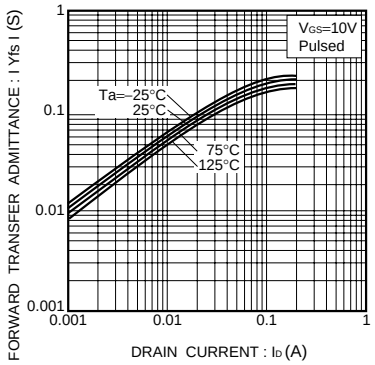


Fig.10 Forward transfer admittance vs. drain current

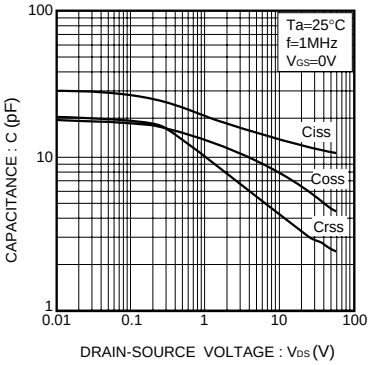


Fig.11 Typical capacitance vs. drain-source voltage

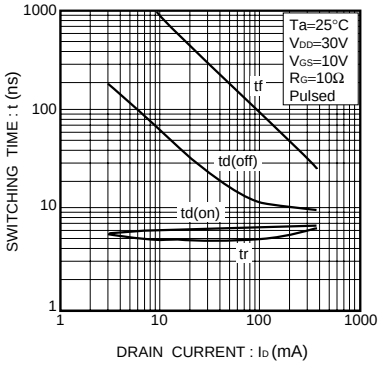


Fig.12 Switching characteristics

●**Switching characteristics measurement circuit**

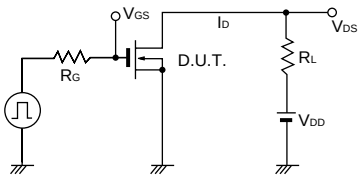


Fig.13 Switching time test circuit

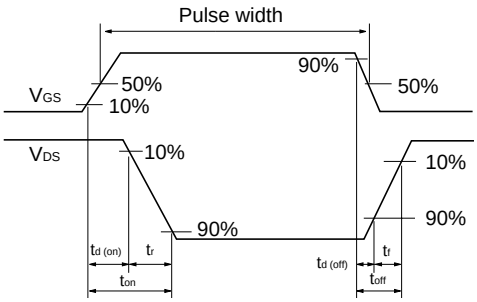


Fig.14 Switching time waveforms