Value ASIC for high function and price-performance applications

ASIC SA-12E Standard Cell/Gate Array

Highlights

Extensive portfolio of cores

0.18 µm effective channel length high performance

Designs of up to 10 million gates

0.05 µW/MHz/gate power dissipation

Optimized for low 1.8-2.5 volt operation

I/O library elements to support multiple industry requirements

One- and two-port high-performance compilable SRAMS

Data path optimization with bit stacking for performance and density

Automatic gate array fill of free space for quick turn engineering change options

SOC technology for mainstream applications

In full manufacturing production today, SA-12E ASIC has delivered on the IBM promise of advanced technology for system-on-a-chip (SOC) design. Serving the needs of data processing, communication and pervasive computing the IBM Blue Logic Core Program has nearly 100 predesigned cores available for your use.

SA-12E is a standard cell and gate array ASIC with up to 10 million gates, multiple supported voltages, low-power features, and a broad array of price-performance packages.

Product specifications

- L_{eff} = 0.18 µm, L_{drawn} = 0.25 µm
- 10 million wireable gates
- Power supply (internal logic and I/O): 2.5/1.8 V
- Second power supply (I/O): 3.3/2.5/1.5 V
- Power dissipation of 0.05 µW/MHz/gate @ 1.8 V
- Gate delays of 50 ps @ 2.5 V
- 5 levels of metal for global routing
- Ambient operating temperature range: -40° C to 100° C
- High reliability options available

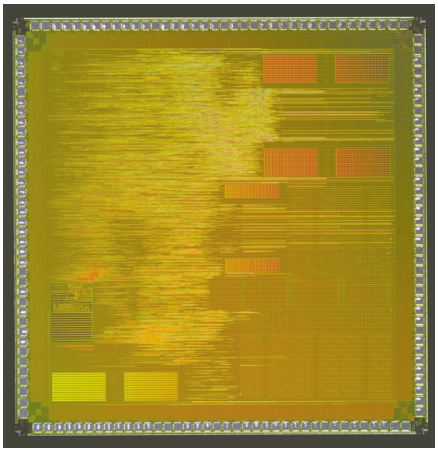
IBM Blue Logic™ core program

The IBM Blue Logic core program adds the value of our unique ASIC intellectual property to your ASIC design, quickly and easily. Our Blue Logic cores are designed for the communications, data processing, and consumer industries. By using cores optimized for your industry, you can quickly build and deliver to market customer-specific products. Our experience in linking complex functions means that we can help you get to market faster and less expensively. SA-12E offers a rich portfolio of cores, from processors to voice/data networking to data compression to multimedia functions.

IBM Blue Logic design methodology and tools

IBM delivers first-time-right design to help reduce product development time and improve your market responsiveness. IBM Blue Logic design methodology is flexible enough to produce half-million gate ASICs and extensible enough to handle multimillion-gate designs, with seamless inclusion of your choice of cores for system-level-silicon. For your convenience, we support many industry-standard CAD tools, and to make your life even easier, we offer IBM design tools with special features such as:

- *Static timing analysis*, which replaces gate-level simulation, resulting in shorter run times and maximum path checking
- *Automatic test pattern generation* (ATPG), which does away with the tedious, time-consuming generation of test vectors
- *A new clock distribution methodology*, which improves skew, latency, and power management
- *ASIC sign-off toolkit*, which integrates an extensive and important process into a single EDA package
- *Floorplanning*, which avoids congested areas.



ASIC with cores

Specifications

Function	Capability
High performance compilable 1-Port SRAM	Maximum size: 1M bits, Maximum words: 32768 Maximum width: 128 bits, Multiple Array Built-In Self Test 1.9 ns Access, 2.6 ns Cycle (typical, 4096 words x 32 bits)
High density compilable 1-Port SRAM	Maximum size: 1M bits, Maximum words: 32768 Maximum width: 128 bits, Array Built-In Self Test 1.9 ns Access, 2.5 ns Cycle (typical, 4096 words x 32 bits)
Low power compilable 1-Port SRAM	Maximum size: 256 K bits, Maximum words: 16384 Maximum width: 36 bits, Multiple Array Built-In Self Test 2.4 ns Access, 3.7 ns Cycle (typical, 4096 words x 32 bits)
High performance compilable 2-Port SRAM	Maximum size: 128 K bits, Maximum words: 4096 Maximum width: 128 bits, Multiple Array Built-In Self Test 2.0 ns Access, 2.1 ns Cycle (typical, 1024 words x 32 bits)
High performance compilable ROM	Maximum size: 1M bits, Maximum words: 32768 Maximum width: 64 bits, Array Built-In Self Test TBD ns Access, TBD ns Cycle (typical, 4096 words x 32 bits)
Low power compilable ROM	Maximum size: 1M bits, Maximum words: 32768 Maximum width: 64 bits, Array Built-In Self Test TBD ns Access, TBD ns Cycle (typical, 4096 words x 32 bits)
Compilable register arrays 2-Port through 6-Port	Up to 10.2 K bits
Phase-locked loop (PLL)	35 MHz-600 MHz lock-in range. Fully integrated mixed-mode design. No external components. Programmable multiplication factor (1-16)

IBM Blue Logic design services

The IBM ASIC Design Centers are staffed by a team of highly experienced engineers, programmers, and technicians to provide you with expert design, development, consultation, and logical and physical processing services for every phase of CMOS chip design. Our services are customized to meet your specific needs through one-on-one design consultation, extensive documentation, and focused education in tools and methodology, tailored to your team and your project requirements.

Packaging

SA-12E packaging options offer both density and price performance.

- Ceramic ball grid array (CBGA): Flip-chip 937 maximum total leads
- Ceramic column grid array (CCGA): Flip-chip 1657 maximum total leads
- Plastic ball grid array (PBGA): Flip-chip 1680 maximum total leads; Wire bond 580
- Plastic quad flat pack (PQFP): Wire bond 240 maximum total leads
- Low profile plastic quad flat pack (LQFP): Wire bond 176 maximum total leads
- Thin fine pitch ball grid array (TFBGA): Wire bond 220 maximum total leads

Input/output library elements

- LVCMOS/LVTTL, 2.5 V CMOS, PCI, SSTL-3, AGP
- Three-state, push-pull, open drain drivers with transceiver option
- ESD protection ≥ 3.0 kV

Internal library elements (Multiple drive strengths available)

SA-12E power dissipation is 0.05 µW/MHz/gate at 1.8 V operation. All library elements are available in three to five drive strengths, and a set of the most commonly used elements is available in three additional lower drive strengths for further power reduction.

- AND/NAND-OR/NOR (2 to 4 inputs)
- Multiplexer
- AND-OR/AND-OR-INVERT
- Full adder
- OR-AND/OR-AND-INVERT
- Clock timing terminators
- XOR/XNOR (2 or 3 inputs)
- Clock drivers, splitters, and choppers with balanced rise/fall times
- Comparators
- Delay line
- Data path elements

Full-scan latch library elements (Multiple drive strengths available)

- D Latches (1 and 2 ports)
- Set-reset latches
- Scannable D flip-flops

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