ASIC SA-27 Standard Cell/Gate Array

Highlights

0.12 µm effective channel length high performance

Designs of up to 12 million gates

Copper metallurgy for high performance in sub-quarter-micron technology

0.03 µW/MHz/gate power dissipation

1.8 volt power supply with optional 2.5 or 3.3 volt I/O interfacing

7 levels of metal — 6 for global routing, 1 for local interconnects

Data path optimization with bit stacking for performance and density

Design advantages

The IBM ASIC SA-27 is optimized for high integration and performance, and has been successfully designed into a wide variety of applications ranging from switch fabrics and servers to multimedia workstations and chip testers. With effective channel lengths of 0.12 µm, the IBM copper process, and 7 levels of metal, SA-27 has been proven in designs up to 12 million usable gates capable of operating at 33 picoseconds, as modeled for a 2 input NAND with fan out of 2 at 1.8 volts.

Our experience with multimillion gate design and our seamless migration of designs from one technology to the next brings you first-time-right design. SA-27 gives you the flexibility to design with both gate array and standard cell circuitry on a single die. SA-27 package options include both ceramic and organic packages for pin counts of up to 1657. SA-27 is optimized for 1.8 volt operation with optional 2.5 and 3.3 volt I/O interfacing. SA-27 brings you industry-leading performance and integration in an ASIC for your advanced data processing and communication products.

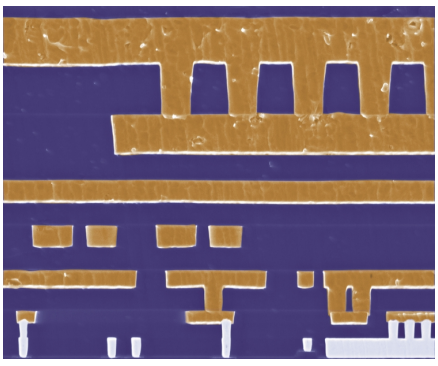
Product specifications

- L_{eff} = 0.12 µm, L_{drawn} = 0.16 µm
- 12 million wireable gates
- Power supply (internal logic and I/O): 1.8 V
- Second power supply (I/O): 2.5 V or 3.3 V
- Power dissipation of 0.03 µW/MHz/gate @ 1.8 V
- Gate delays of 33 ps @ 1.8 V
- 7 levels of metal: 6 for global routing, 1 for local interconnect
- Ambient operating temperature range: -40° C to 100° C
- High reliability option available

IBM Blue Logic™ design methodology and tools

IBM delivers first-time-right design to help reduce product development time and improve your market responsiveness. IBM Blue Logic design methodology is flexible enough to produce half-million gate ASICs and extensible enough to handle multimillion-gate designs, with seamless inclusion of your choice of cores for system-level-silicon. For your convenience, we support many industry-standard CAD tools, and to make your life even easier, we offer Blue Logic design tools with special features such as:

- *Static timing analysis,* which replaces gate-level simulation, resulting in shorter run times and maximum path checking
- *Automatic test pattern generation* (ATPG), which does away with the tedious, time-consuming generation of test vectors
- *A new clock distribution methodology*, which improves skew, latency, and power management
- *ASIC sign-off toolkit,* which integrates an extensive and important process into a single EDA package
- *Floorplanning,* which avoids congested areas



Section showing copper metallurgy

Specifications

Function	Capability
High performance compilable 1-Port SRAM	Maximum Size: 1M bits, Maximum words: 32768 Maximum width: 128 bits, Multiple Array Built-in Self Test 1.5 ns Access, 1.8 ns Cycle (typical, 4096 words x 32 bits)
High performance compilable 2-Port SRAM	Maximum Size: 128 K bits, Maximum words: 4096 Maximum width: 128 bits, Multiple Array Built-in Self Test 1.3 ns Access, 1.7 ns Cycle (typical, 1024 words x 32 bits)
Compilable register arrays 2-Port through 6-Port	Up to 10.2 K bits 0.8 ns read (typical conditions, 32 words x 32 bits, 2-port)
Phase-locked loop (PLL)	66 MHz-1 GHz lock-in range. Fully integrated mixed-mode design. No external components. Programmable multiplication factor (1-16)

IBM Blue Logic design services

The IBM ASIC design centers are staffed by a team of highly experienced engineers, programmers, and technicians to provide you with expert design, development, consultation, and logical and physical processing services for every phase of CMOS chip design. Our services are customized to meet your specific needs through one-on-one design consultation, extensive documentation, and focused education in tools and methodology, tailored to your team and your project requirements.

Packaging

SA-27 packaging options focus on density and performance.

- Ceramic ball grid array (CBGA): C4; 624 maximum total leads
- Ceramic column grid array (CCGA): C4; 1657 maximum total leads
- Organic ball grid array (HyperBGA™): C4; 1657 maximum total leads

Input/output library elements

- 1.8 V CMOS, 2.5 V CMOS, 3.3 V LVTTL, HSTL, LVDS, GTL/GTL+, STI, PECL, SSTL
- Three-state, push-pull, open drain drivers with transceiver option
- ESD protection ≥ 4.0 kV

Internal library elements (Multiple drive strengths available)

SA-27 typical power dissipation is 0.03 µW/MHz/gate at 1.8 V operation. All library elements are available in three to five drive strengths, and a set of the most commonly used elements is available in three additional lower drive strengths for further power reduction.

- AND/NAND-OR/NOR (2 to 4 inputs)
- Multiplexer
- AND-OR/AND-OR-INVERT
- Full adder
- OR-AND/OR-AND-INVERT
- Clock timing terminators
- XOR/XNOR (2 or 3 inputs)
- Clock drivers, splitters, and choppers with balanced rise/fall times
- Comparators
- Delay line
- Data path elements

Full-scan latch library elements (Multiple drive strengths available)

- D Latches (1 and 2 ports)
- Set-reset latches
- Scannable D flip-flops

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