SONET/SDH/ATM OC-48 DIFFERENTIAL 16:1 TRANSMITTER S3063

FEATURES

- Micro-power Bipolar supply
- Complies with Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation
- Supports 2.488 Gbps (OC-48)
- Reference frequency of 155.52 MHz
- Interface to both LVPECL and LVTTL logic
- 16-bit Differential LVPECL data path
- Compact 100 TQFP/TEP package
- Diagnostic loopback mode
- Line loopback mode
- Lock detect
- Low jitter LVPECL interface
- Internal FIFO to decouple transmit clocks
- Single 3.3V supply
- Typical power 1.45 W

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- DWDM Systems
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

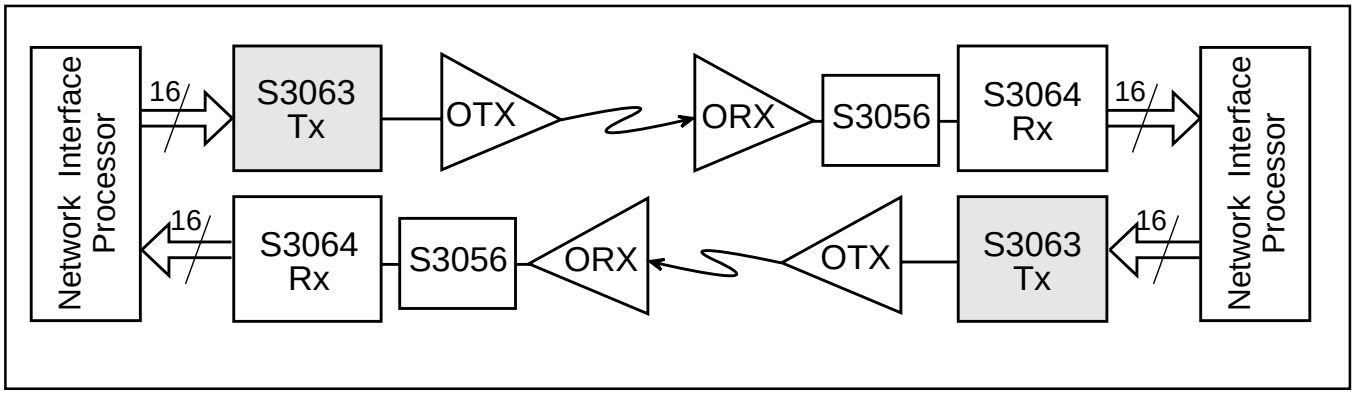
GENERAL DESCRIPTION

The S3063 SONET/SDH MUX chip is a fully integrated serialization SONET OC-48 (2.488 Gbps) interface device. The chip performs all necessary parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis PLL components are contained in the S3063 MUX chip allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 MHz reference clock, in support of existing system clocking schemes.

The low jitter LVPECL interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3063 is packaged in a 100 TQFP/TEP, offering designers a small package outline.

Figure 1. System Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3063 chip supports the OC-48 data rate (2.488 Gbps).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-48 consists of 144 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 144 overhead and 4176 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the Bellcore SONET standard document.

Figure 2. SONET Structure

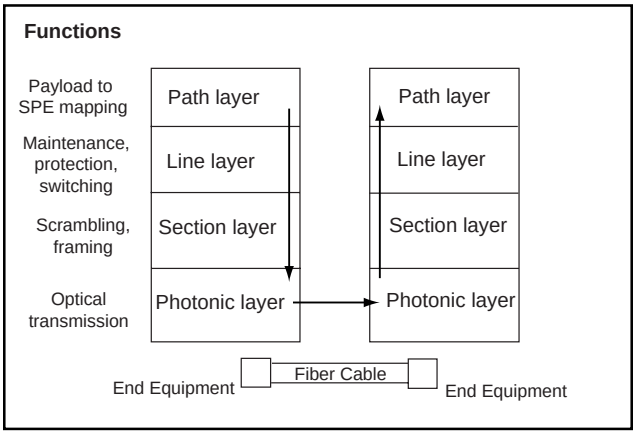
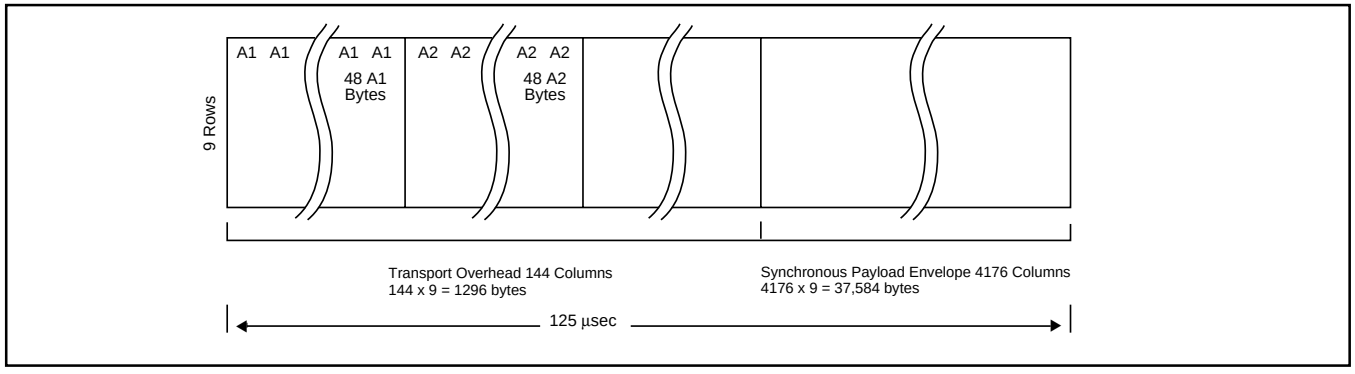


Table 1. SONET Signal Hierarchy

Elec.	CCITT	Optical	Data Rate (Mbps)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 3. STS-48/OC-48 Frame Format



S3063 OVERVIEW

The S3063 transmitter implements SONET/SDH serialization and transmission functions. The block diagram in Figure 4 shows the basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes parallel-to-serial conversion and system timing. The system timing circuitry consists of a high-speed phase detector, clock divider, and clock distribution throughout the front end.

The sequence of operations is as follows:

Transmitter Operations:

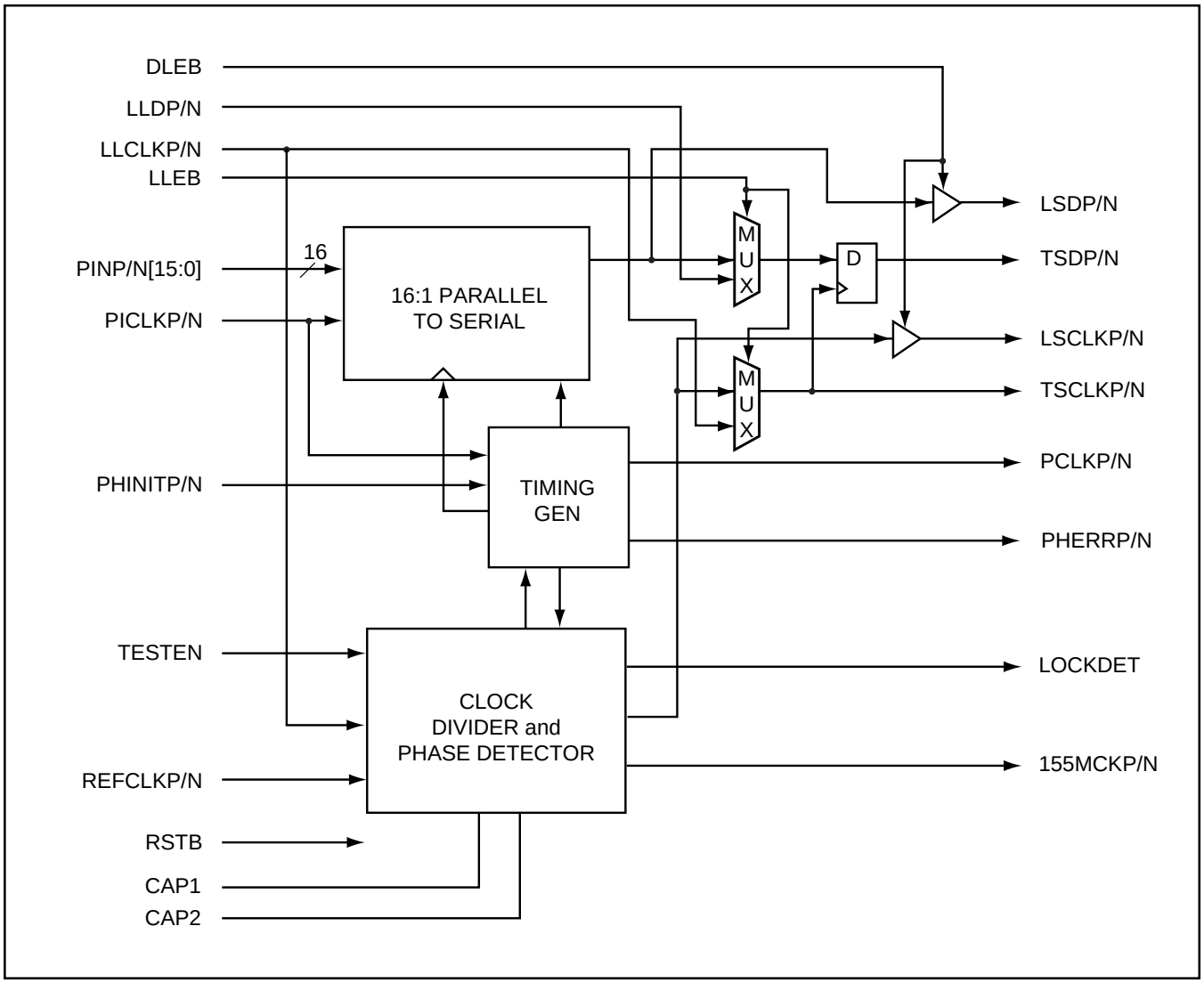
1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 7, 8 and 9.

Suggested Interface Devices

AMCC	S3056	OC-48 Clock Recovery Device
AMCC	S3064	OC-48 Receiver

Figure 4. S3063 Functional Block Diagram



S3063 ARCHITECTURE/FUNCTIONAL DESIGN

MUX OPERATION

The S3063 performs the serializing stage in the processing of a transmit SONET STS-48 bit serial data stream. It converts the 16-bit serial 155.52 Mbyte/sec data stream to bit serial format at 2.488 Gbps. Diagnostic loopback is provided (transmitter to receiver), and line loopback is also provided (receiver to transmitter).

A high-frequency bit clock is generated from a 155.52 MHz frequency reference by using a frequency synthesizer consisting of an on-chip phase-locked loop circuit with a divider, VCO and loop filter.

Clock Divider and Phase Detector

The clock divider and phase detector, shown in the block diagram in Figure 4, contains monolithic PLL components that generate signals required to drive the loop filter.

The REFCLK input must be generated from a differential LVPECL crystal oscillator which has a frequency accuracy which exceeds the value stated in Table 6 in order for the VCOCLK frequency to have the same accuracy required for operation in a SONET system.

In order to meet the 0.01 UI SONET jitter generation, the maximum reference clock jitter must be guaranteed over the 12 kHz to 20 MHz bandwidth. For details of reference clock jitter requirements, see Table 2.

The on–chip phase detector, which compares the phase relationship between the VCO input and the REFCLKP/N input, drives the loop filter.

Timing Generator

The timing generator function, seen in Figure 4, provides two separate functions. It provides a 16-bit parallel rate version of the TSCLK, and a mechanism for aligning the phase between the incoming 16-bit parallel clock and the clock which loads the parallel-to-serial shift register.

The PCLK output is a 16-bit parallel rate version of TSCLK. For STS-48, the PCLK frequency is 155.52 MHz. PCLK is intended for use as a 16-bit rate clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3063 device.

In the parallel-to-serial conversion process, the incoming data is passed from the PICLK 16-bit parallel clock timing domain to the internally generated 16-bit parallel clock timing domain, which is phase aligned to TSCLK.

The timing generator also produces a feedback reference clock to the phase detector. A counter divides the synthesized clock down to the same frequency as the Reference Clock.

Table 2. Reference Jitter Limits

Maximum Reference Clock Jitter in 12 kHz to 20 MHz Band	Operating Mode
1 ps rms	STS-48

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 4 is comprised of a FIFO and a parallel-to-serial register. The FIFO input latches the data from the PINP/N[15:0] bus on the rising edge of PICLKP. The parallel-to-serial register is a loadable shift register which takes its parallel input from the FIFO output.

An internally generated divide by 16 clock, which is phase aligned to the transmit serial clock as described in the Timing Generator description, activates the parallel data transfer between registers. The serial data is shifted out of the parallel-to-serial register at the TSCLK rate.

FIFO

A FIFO is added to decouple the internal and external (PICLK) clocks. The internally generated divide by 16 clock is used to clock out data from the FIFO. PHINIT and LOCKDET are used to center or reset the FIFO. The PHINIT and LOCKDET signals will center the FIFO after the third PICLK pulse. This is in order to insure that PICLK is stable. This scheme allows the user to have an infinite PCLK to PICLK delay through the ASIC. Once the FIFO is centered, the PCLK to PICLK delay can have a maximum drift as specified in Table 20.

FIFO Initialization

The FIFO can be initialized in one of the following three ways:

1. During power up, once the PLL has locked to the reference clock provided on the REFCLK pins, the LOCKDET will go active and initialize the FIFO.
2. When RSTB goes active, the entire chip is reset. This causes the PLL to go out of lock and thus the LOCKDET goes inactive. When the PLL reacquires the lock, the LOCKDET goes active and initializes the FIFO. Note: PCLK is held reset when RSTB is active.
3. The user can also initialize the FIFO by raising PHINIT.

During normal running operation, the incoming data is passed from the PICLK timing domain to the internally generated divide by 16 clock timing domain. Although the frequency of PICLK and the internally generated clock is the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PICLK and the internally generated clock. When a potential setup or hold time violation is detected, the phase error goes high. If the condition persists, PHERR will remain high. When PHERR conditions occur, PHINIT should be activated to recenter the FIFO (at least 2 PCLK periods). This can be done by connecting PHERR to PHINIT. When realignment occurs up to ten bytes of data will be lost. The user can also take in the PHERR signal, process it and send an output to PHINIT in such a way that idle bytes are lost during the realignment process. PHERR will go inactive when the realignment is complete. (See Figure 11).

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output clock and data from the transmitter (LSCLK and LSD) is routed to the serial-to-parallel block in place of the normal data stream (RSCLK and RSD).

Line Loopback

The line loopback circuitry consists of alternate clock and data output drivers. For the S3063, it selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable (LLEB) input is inactive, it selects data and clock from the parallel to serial converter block. When LLEB is active, it forces the output data multiplexer to select data and clock from the LLD and LLCLK inputs, and a receive-to-transmit loopback can be established at the serial data rate. The LLEB and DLEB can be active at the same time.

Table 3. Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PINP0 PINP1 PINP2 PINP3 PINP4 PINP5 PINP6 PINP7 PINP8 PINP9 PINP10 PINP11 PINP12 PINP13 PINP14 PINP15 PINN0 PINN1 PINN2 PINN3 PINN4 PINN5 PINN6 PINN7 PINN8 PINN9 PINN10 PINN11 PINN12 PINN13 PINN14 PINN15	Diff. LVPECL	I	23 26 28 30 32 34 36 38 40 42 44 46 48 52 54 56 24 27 29 31 33 35 37 39 41 43 45 47 49 51 53 55	Parallel Data Input. A 155.52 Mbyte/sec word, aligned to the PICLK parallel input clock. PINP/N[15] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PINP/N[0] is the least significant bit (corresponding to bit 16 of each PCM word, the last bit transmitted). PINP/N[15:0] is sampled on the rising edge of PICLKP.
PICLKP PICLKN	Diff. LVPECL	I	19 20	Parallel Input Clock. A 155.52 MHz nominally 50% duty cycle input clock, to which PINP/N[15:0] is aligned. PICLK is used to transfer the data on the PINP/N inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLKP samples PINP/N[15:0].
LLDP LLDN	Externally Biased Diff. LVPECL	I	12 13	Line Loopback Data. Inputs normally provided from a companion S3064 device. Used to implement a line loopback function in which the receive serial bit data and clock signals are regenerated and passed through the S3063 transmitter. Internally terminated.
LLCLKP LLCLKN	Externally Biased Diff. LVPECL	I	9 10	Line Loopback Clock. Inputs normally provided from a companion S3064 device. Used to implement a line loopback function in which the receive serial bit data and clock signals are regenerated and passed through the S3063 transmitter. Internally terminated.

Table 3. Input Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
TESTEN	LVTTL	I	76	Test Clock Enable. Set High to bypass the VCO using the LLCLK inputs. This mode operates at 2.488 GHz.
REFCLKP REFCLKN	Internally Biased Diff. LVPECL	I	96 95	Reference Clock. Input used as the reference for the internal bit clock frequency synthesizer. Internally terminated and biased.
DLEB	LVTTL	I	77	Diagnostic Loopback Enable. Active Low. When active, selects diagnostic loopback. When DLEB is inactive, LSD is powered down and inactive and LSCLK is inactive. When active, the diagnostic loopback clock, (LSCLK), and data (LSD) outputs are active. TSD and TSCLK remain active in both states of DLEB.
RSTB	LVTTL	I	7	Master Reset. Reset input for the device. Active Low. During reset, PCLK does not toggle.
PHINITP PHINITN	Diff. LVPECL	I	60 59	Phase Initialization. Rising edge will realign internal timing.
LLEB	LVTTL	I	78	Line Loopback Enable. Active Low. Selects line loopback. When LLEB is active, the S3063 will route the data from the LLD/LLCLK inputs to the TSD/TSCLK outputs.
CAP1 CAP2	Analog	I	84 83	Loop Filter Pins. Connections for external loop filter capacitor and resistors. (See Figure 12).

Table 4. Output Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
TSCLKP TSCLKN	Diff. CML	O	71 70	Transmit Clock output. Transmit serial clock output that can be used to retime the TSD signal.
TSDP TSDN	Diff. CML	O	68 67	Transmit Serial Data. Serial data stream signals, normally connected to an optical transmitter module.
PCLKP PCLKN	Diff. LVPECL	O	21 22	Parallel Clock. A reference clock generated by dividing the internal bit clock by sixteen. It is normally used to coordinate 16-bit parallel data transfers between upstream logic and the S3063 device.
LSDP LSDN	Low Swing Diff. CML	O	5 6	Loopback Serial Data. Serial data stream signals normally connected to a companion S3064 device for diagnostic loopback purposes. The LSDP/N outputs are updated on the falling edge of the LSCLKP.
LSCLKP LSCLKN	Diff. CML	O	1 2	Loopback Serial Clock. Serial clock signals normally connected to a companion S3064 device for diagnostic loopback purposes. The LSD outputs are updated on the falling edge of the LSCLKP.
155MCKP 155MCKN	Diff. LVPECL	O	17 18	155.52 MHz Clock Output. 155.52 MHz clock output from the clock synthesizer. This output should be connected to the reference clock input of the external clock recovery function (such as the S3056).
LOCKDET	LVTTL	O	61	Lock Detect. Active Low. Goes active after the PLL has locked to the clock provided on the REFCLK pins. LOCKDET is an asynchronous output.
PHERRP PHERRN	Diff. LVPECL	O	58 57	Phase Error Signal. Active High. Pulses High during each PCLK cycle for which there is a potential setup/hold timing violation between the internal 16-bit parallel clock and PICLK timing domains. PHERR is updated on the falling edge of the PCLKP output.

Table 5. Common Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
CORE_GND	GND		4, 64, 66, 69, 72, 75, 80, 82, 93, 97, 98	Core Ground
CORE_VCC	+3.3V		3, 63, 65, 73, 74, 79, 81, 87, 99, 100	Core VCC
LVP_VCC	+3.3V		11, 14, 25	LVPECL VCC
LVP_GND	GND		8, 15, 50	LVPECL Ground
TTL_VCC	+3.3V		62	TTL VCC
TTL_GND	GND		16	TTL Ground
NC			90 94	Not Connected
AVCC	+3.3V		86, 89, 92	Analog VCC
AGND	GND		85, 88, 91	Analog Ground

Figure 5. S3063 Pinout 100 TQFP/TEP

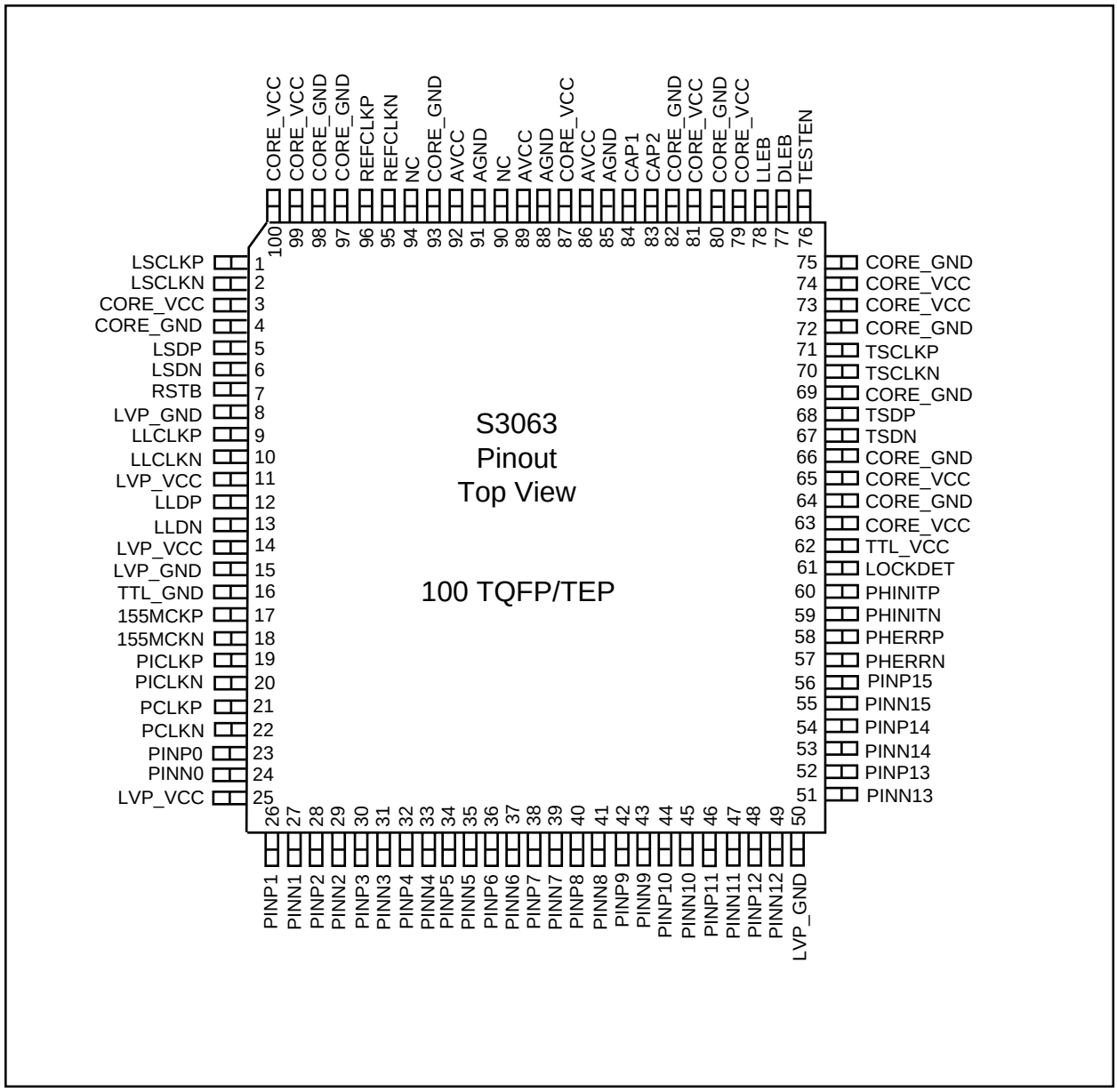
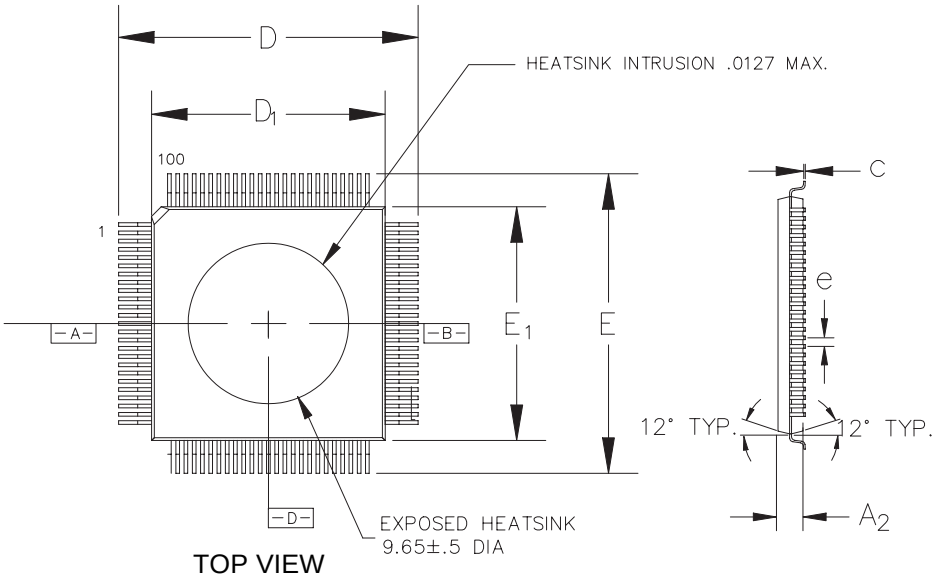
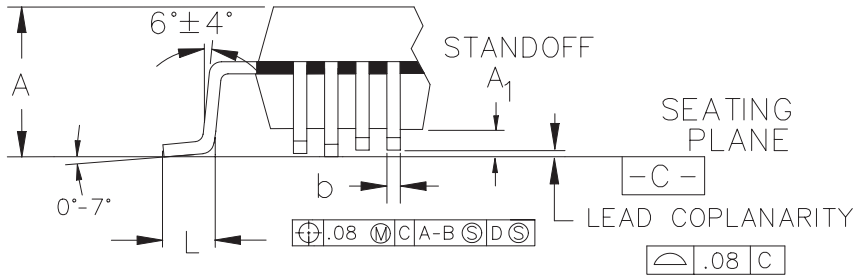


Figure 6. 100 TQFP/TEP Package





DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	b	e	c
MIN		0.05	1.35	15.80	13.95	15.80	13.95	0.50	0.17	0.50 BSC.	
NOM			1.40	16.00	14.00	16.00	14.00	0.60	0.22		
MAX	1.60	0.15	1.45	16.20	14.05	16.20	14.05	0.75	0.27		0.17

Note: The S3063 pacakge is equipped with an embedded conductive heatsink on the top.

Table 6. Thermal Management

Max Package Power	Θjc
1.8 W	2.5° C/W

1. Add 45 mA for loopback active.
2. Open outputs.

Table 7. Performance Specifications

Parameter	Min	Typ	Max	Units	Conditions
Nominal VCO Center Frequency		2.488		GHz	
Reference Clock Frequency Tolerance	-100		+100	ppm	± 20 ppm. Required to meet SONET output frequency specification.
Reference Clock Input Duty Cycle	45		55	%	
Reference Clock Rise & Fall Times			1.5	ns	20% to 80% of amplitude.

Table 8. Output Jitter Generation vs. Case Temperature with Heatsink (DW0045-28) and 100 LFPM

	Temperature	Jitter Generation			Unit
Voltage		3.135	3.3	3.465	V
	0˚ C	0.006	0.006	0.006	UI (rms)
	25˚ C	0.007	0.006	0.006	UI (rms)
	70˚ C	0.007	0.007	0.007	UI (rms)
	100˚ C	0.007	0.007	0.007	UI (rms)

Table 9. Output Jitter Generation vs. Case Temperature In Still Air

	Temperature	Jitter Generation			Unit
Voltage		3.135	3.3	3.465	V
	0˚ C	0.006	0.006	0.006	UI (rms)
	25˚ C	0.007	0.007	0.007	UI (rms)
	70˚ C	0.008	0.007	0.007	UI (rms)
	100˚ C	0.008	0.008	0.008	UI (rms)

Table 10. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on V_{CC} with Respect to GND	-0.5		V_{CC}	V
Voltage on any LVTTL Input Pin	-0.5		V_{CC}	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
LVTTL Output Sink Current			8	mA
LVTTL Output Source Current			8	mA

ESD Ratings

The S3063 is rated to the following voltages based on the human body model:
1. All pins are rated at or above 2000 V except LLCLKP/N, LLDP/N, LOCKDET, REFCLKP, CAP1, CAP2, Pin #85, 86, 89.

Table 11. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	0		100	˚C
Voltage on V_{CC} with Respect to GND	3.135	3.3	3.465	V
Voltage on any LVPECL Input Pin	V_{CC} -2		V_{CC}	V

Table 12. Power Consumption

Parameter	Min	Typ	Max	Units
ICC[1,2]		440	530	mA

1. Add 45 mA for loopback active.
2. Open outputs.

Table 13. LVTTL Input/Output DC Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions
V_{IH}	Input High Voltage	2.0		TTL V_{CC}	V	TTL V_{CC} = Max
V_{IL}	Input Low Voltage	0.0		0.8	V	TTL V_{CC} = Max
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5 V
V_{OH}	Output High Voltage	2.1			V	V_{IH} = Min. V_{IL} = Max. I_{OH} = -100 µA
V_{OL}	Output Low Voltage			0.5	V	V_{IH} = Min. V_{IL} = Max. I_{oL} = 4 mA

Table 14. Differential CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Condition
V_{OL}	CML Output LOW Voltage	V_{CC} -1.05		V_{CC} -0.55	V	100Ω line-to-line.
V_{OH}	CML Output HIGH Voltage	V_{CC} -0.45		V_{CC} -0.10	V	100Ω line-to-line.
$\Delta V_{OUTDIFF}$ Clock	CML Serial Output Differential Voltage Swing	700		1400	mV	100Ω line-to-line. See Figure 10.
$\Delta V_{OUTSINGLE}$ Clock	CML Serial Output Single-ended Voltage Swing	350		700	mV	100Ω line-to-line. See Figure 10.
$\Delta V_{OUTSINGLE}$ Data	CML Serial Output Single-ended Voltage Swing	400		700	mV	100Ω line-to-line. See Figure 10.
$\Delta V_{OUTDIFF}$ Data	CML Serial Output Differential Voltage Swing	800		1400	mV	100Ω line-to-line. See Figure 10.

Table 15. Low Swing Differential CML Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OL}	Loopback CML Output LOW Voltage	V_{CC} -0.55		V_{CC} -0.25	V	100Ω line-to-line.
V_{OH}	Loopback CML Output HIGH Voltage	V_{CC} -0.25		V_{CC} -0.05	V	100Ω line-to-line.
$\Delta V_{OUTDIFF}$	Loopback CML Serial Output Differential Voltage Swing	360		800	mV	100Ω line-to-line. See Figure 10.
$\Delta V_{OUTSINGLE}$	Loopback CML Serial Output Single-ended Voltage Swing	180		400	mV	100Ω line-to-line. See Figure 10.

Table 16. Internally Biased Differential LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	260		1200	mV	See Figure 10.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	130		600	mV	See Figure 10.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 17. Externally Biased Differential LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IL}	LVPECL Input LOW Voltage	V_{CC} -2.000		V_{CC} -0.25	V	
V_{IH}	LVPECL Input HIGH Voltage	V_{CC} -1.20		V_{CC} -0.05	V	
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 10.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		600	mV	See Figure 10.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

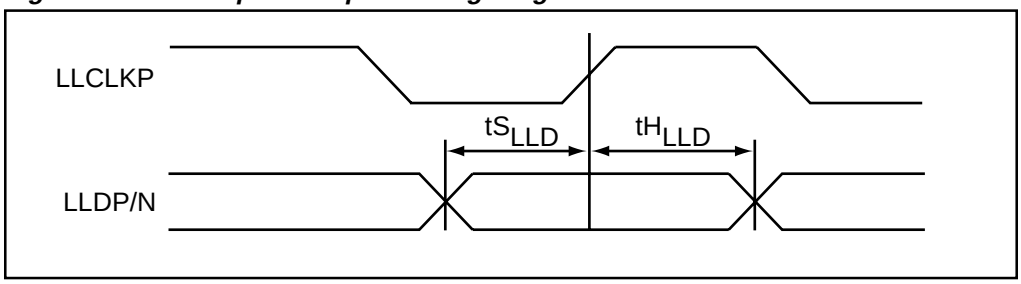
Table 18. Differential LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Comments
V_{IL}	LVPECL Input Low Voltage	V_{CC} -2.0		V_{CC} -0.5	V	
V_{IH}	LVPECL Input High Voltage	V_{CC} -1.2		V_{CC} -0.3	V	
ΔV_{INDIFF}	Differential Input Voltage Swing	400		2000	mV	See Figure 10.
$\Delta V_{INSINGLE}$	Single Ended Input Voltage Swing	200		1000	mV	See Figure 10.

Table 19. Differential LVPECL Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Comments
$\Delta V_{OUTSINGLE}$	Single Ended Output Voltage Swing	320		950	mV	220 Ω to GND and 100 Ω line-to-line.
$\Delta V_{OUTDIFF}$	Differential Output Voltage Swing	640		1900	mV	220 Ω to GND and 100 Ω line-to-line.
V_{OH}	Output High Voltage	V_{CC} -1.15		V_{CC} -0.60	V	220 Ω to GND and 100 Ω line-to-line.
V_{OL}	Output Low Voltage	V_{CC} -1.95		V_{CC} -1.45	V	220 Ω to GND and 100 Ω line-to-line.

Figure 7. Line Loopback Input Timing Diagram



Notes on High-Speed LVPECL Input Timing:

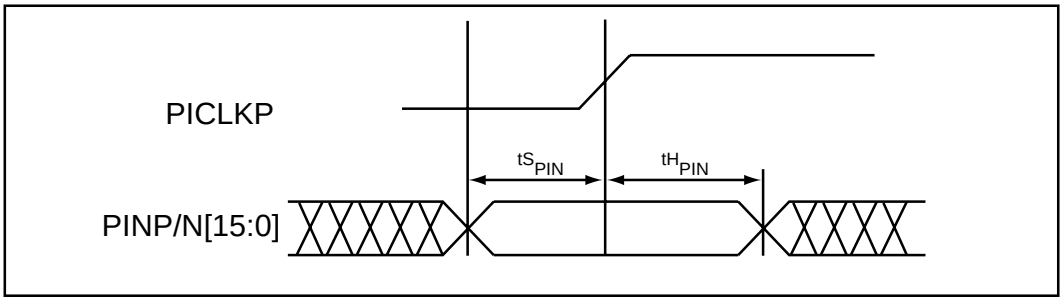
1. Timing is measured from the cross-over point of the reference signal to the cross-over point of the input.

Table 20. AC Transmitter Timing Characteristics

Symbol	Description	Min	Max	Units
	TSCLK/LSCLK Frequency (nom. 2.488 GHz)		2.5	GHz
	TSCLK/LSCLK Duty Cycle [1]	40	60	%
	PICLK Duty Cycle [1]	40	60	%
tS_{PIN}	PINP/N[15.0] Set-up Time w.r.t. PICLKP	1.5		ns
tH_{PIN}	PINP/N[15.0] Hold Time w.r.t. PICLKP	0.5		ns
tS_{TSD}	TSDP/N Set-up Time w.r.t. TSCLKP	90		ps
tH_{TSD}	TSDP/N Hold Time w.r.t. TSCLKP	100		ps
tS_{LLD}	LLDP/N Set-up Time w.r.t. LLCLKP/N	110		ps
tH_{LLD}	LLDP/N Hold Time w.r.t. LLCLKP/N	60		ps
	PCLKP/N Duty Cycle/155 MCKP/N	45	55	%
	CML Clock Output Rise and Fall Time (20% - 80%)		170	ps
	CML Data Output Rise and Fall Time (20% - 80%)		250	ps
tS_{LSD}	LSDP/N Set-Up Time w.r.t. LSCLKP	100		ps
tH_{LSD}	LSDP/N Hold Time w.r.t. LSCLKP	150		ps
	LSCLK Duty Cycle	45	55	%
tP_{CLK}	PCLK to PICLK drift after FIFO is centered		5.2	ns

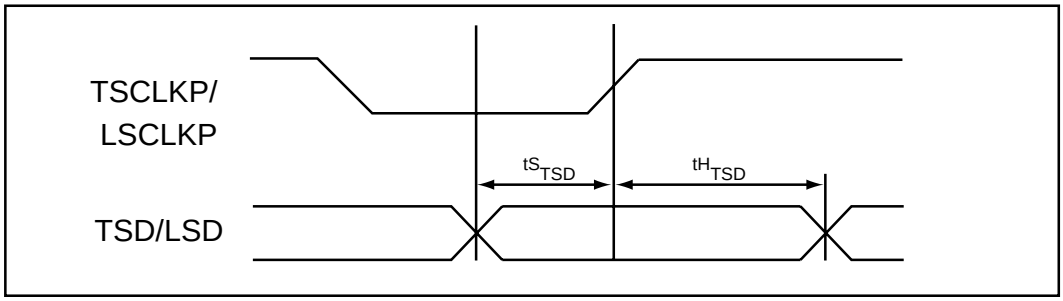
1. Measured at 50% point of P-N.

Figure 8. AC Input Timing



1. When a set-up time is specified on LVPECL signals between an input and a clock, the set-up time is the time in nanoseconds from the crossover point of the input to the crossover point of the clock.
2. When a hold time is specified on LVPECL signals between an input and a clock, the hold time is the time in nanoseconds from the crossover point of the clock to the crossover point of the input.

Figure 9. Output Timing



Notes on High Speed PECL Output Timing

1. When a set-up time is specified on differential CML signals between an output and a clock, the set-up time is thetime in picoseconds from the crossover point of the input to the crossover point of the clock.
2. When a hold time is specified on differential CML signals between an output and a clock, the hold time is the time in picoseconds from the crossover point of the clock to the crossover point of the input.

Figure 10. Differential Voltage Measurement

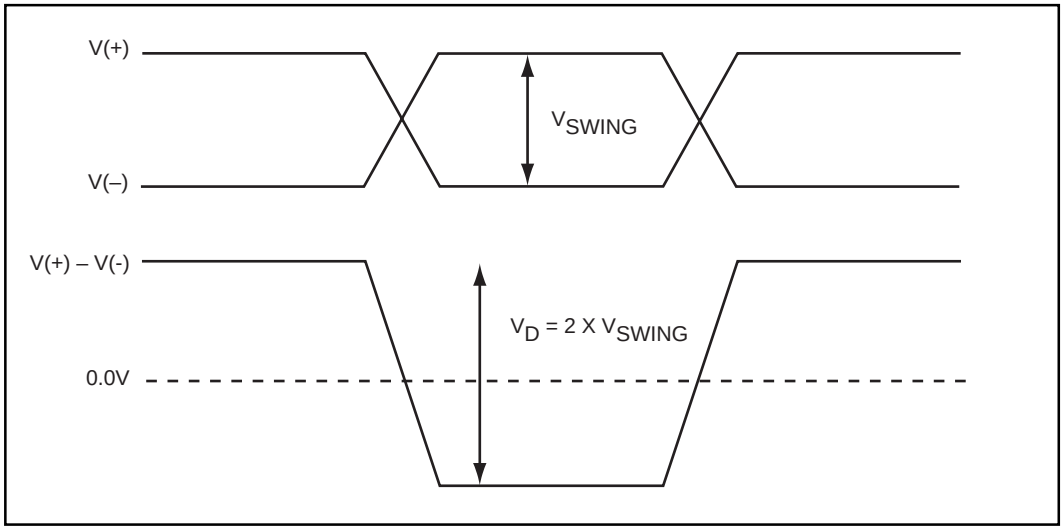
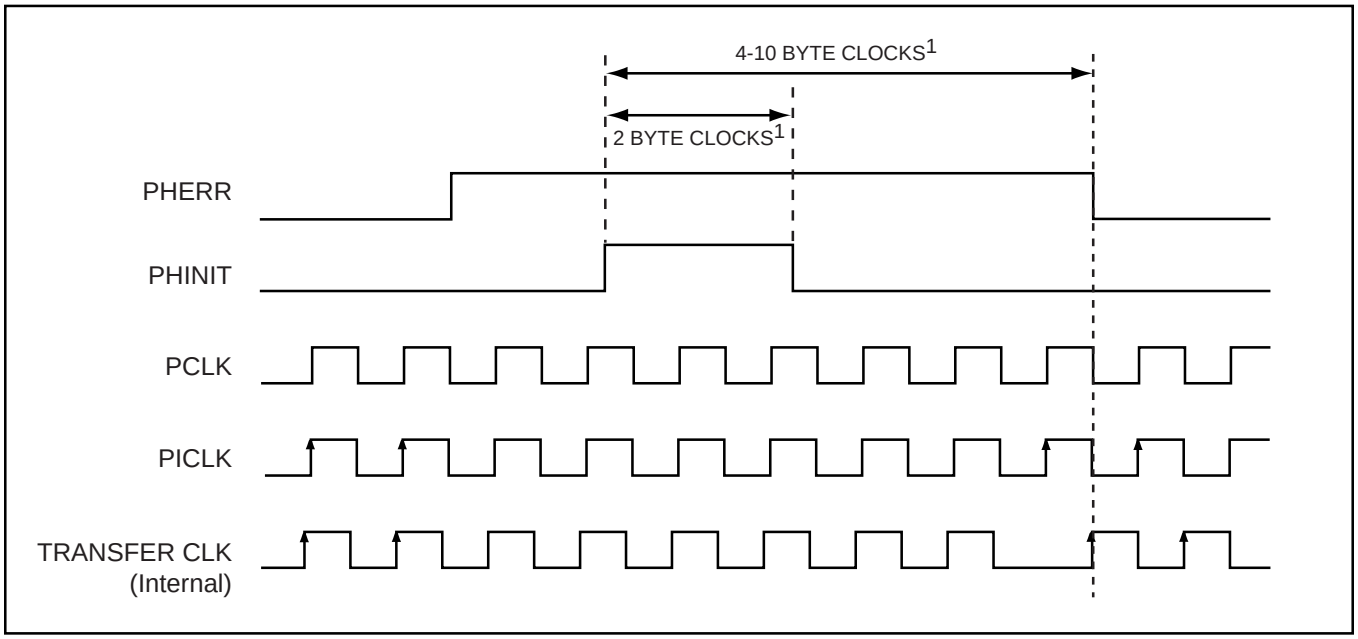


Figure 11. Phase Adjust Timing



1. Byte Clock = 155.52 MHz.

Figure 12. External Loop Filter

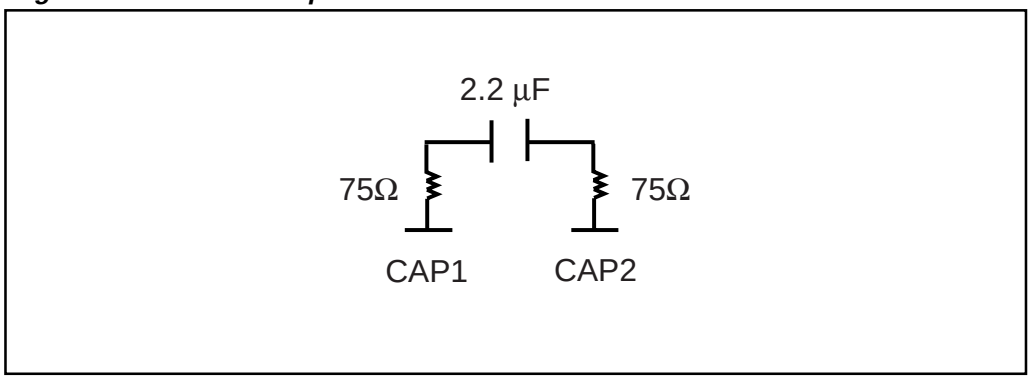


Figure 13. Differential CML Output to +5V PECL Input AC Coupled Termination

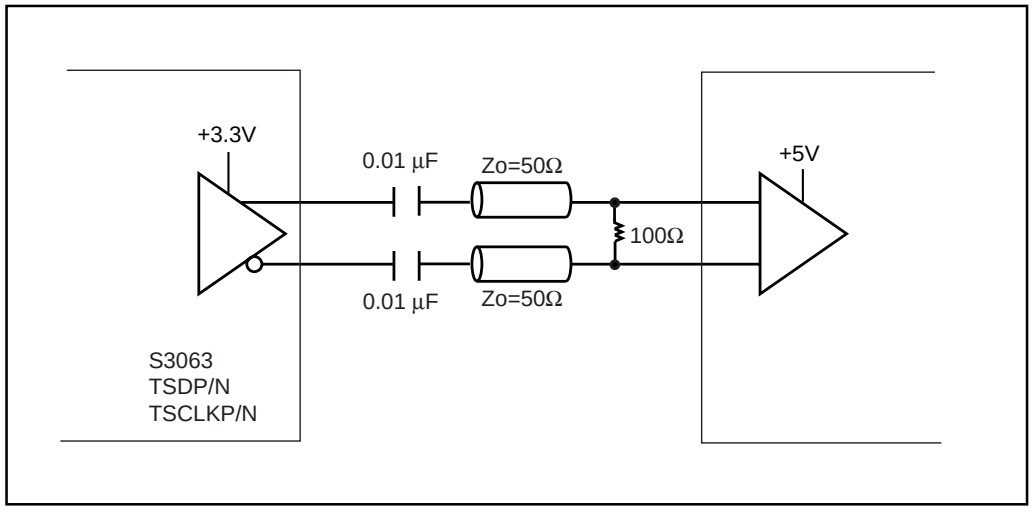


Figure 14. +5V Differential PECL Driver to S3063 Differential LVPECL Input AC Coupled Termination

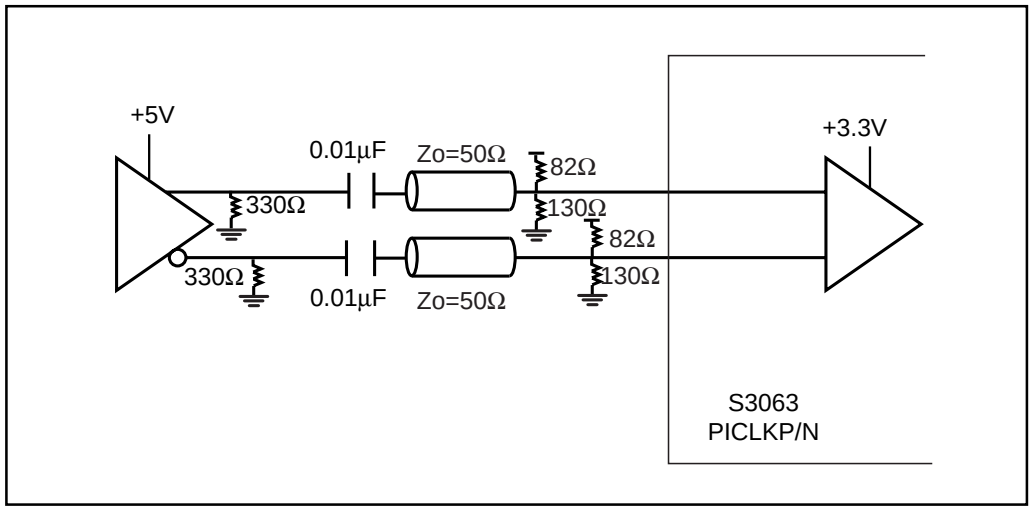


Figure 15. S3063 to Differential LVPECL Input S3063 Terminations

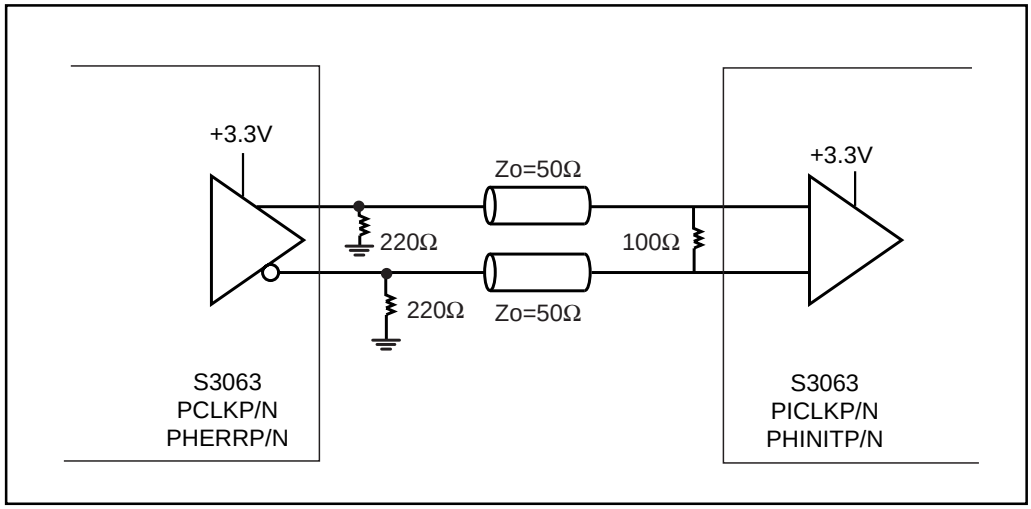
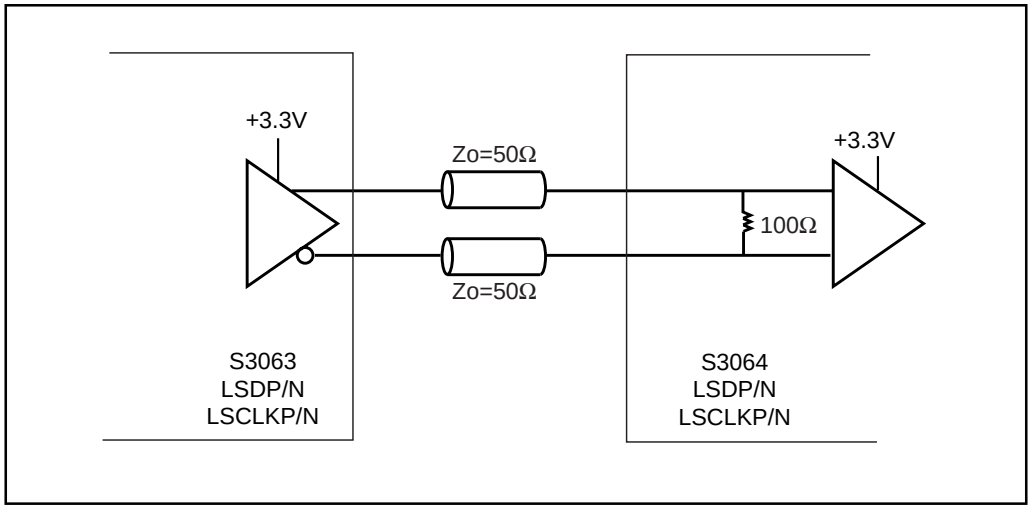


Figure 16. S3063 to S3064 for Diagnostic Loopback



F***igure 17. Differential LVPECL Driver to S3063 Internally Biased Differential LVPECL Input AC Coupled Termination***

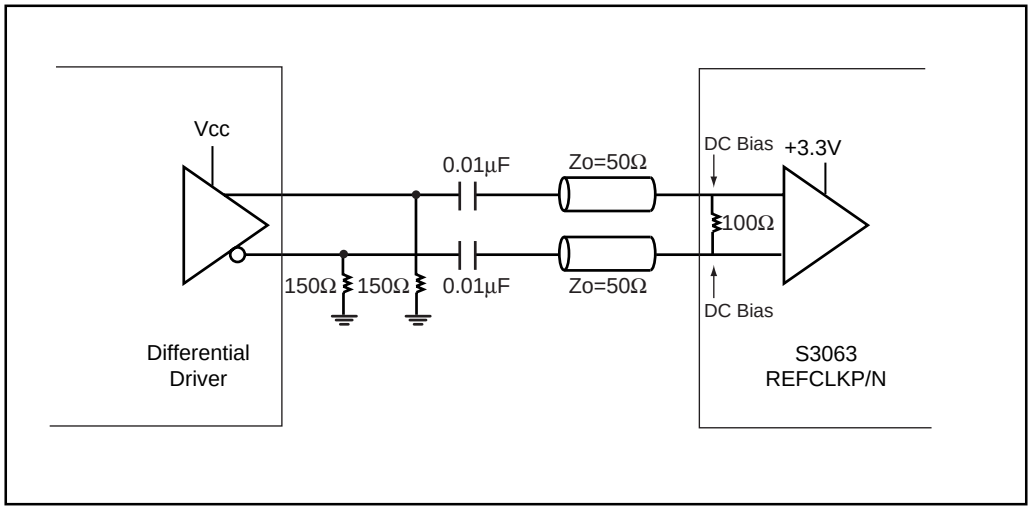
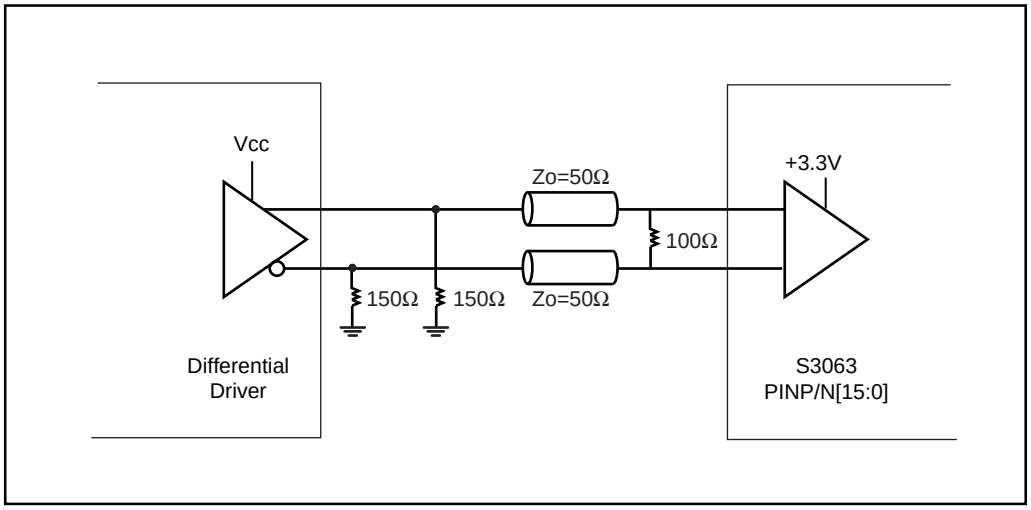
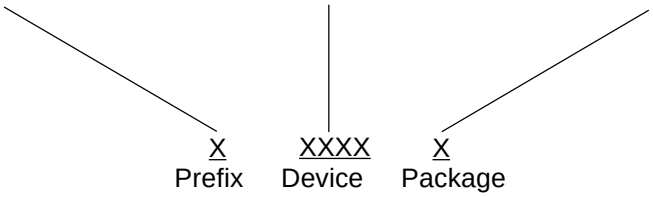


Figure 19. Differential LVPECL Driver to Differential LVPECL Input PINP/N[15:0]



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3063	TT – 100 TQFP/TEP



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