

# SLK2501

## OC-48/24/12/3 SONET/SDH MULTIRATE TRANSCEIVER

SLLS502A – OCTOBER 2001 – REVISED NOVEMBER 2001

- Fully Integrated SONET/SDH Transceiver to Support Clock/Data Recovery and Multiplexer/Demultiplexer Functions
- Supports OC-48, OC-24, OC-12, Gigabit Ethernet and OC-3 Data Rate With Autorate Detection
- Supports Transmit Only, Receiver Only, Transceiver and Repeater Functions in a Single Chip Through Configuration Pins
- Supports SONET/SDH Frame Detection
- On-Chip PRBS Generation and Verification
- Supports 4-Bit LVDS (OIF99.102) Electrical Interface
- Parity Checking and Generation for the LVDS Interface
- Single 2.5-V Power Supply
- Interfaces to Back Plane, Copper Cables, or Optical Modules
- Hot Plug Protection
- Low Jitter PECL Compatible Differential Serial Interface With Programmable De-Emphasis for the Serial Output
- On-Chip Termination for LVDS and PECL Compatible Interface
- Receiver Differential Input Thresholds 150 mV Min
- Supports SONET Loop Timing
- Low Power <900 mW at OC-48 Rate
- ESD Protection >2 kV
- 622-MHz Reference Clock
- Maintains Clock Output in Absence of Data
- Local and Remote Loopback
- 100-Pin PZP Package With PowerPad™ Design

### description

The SLK2501 is a single chip multirate transceiver IC used to derive high speed timing signals for SONET/SDH based equipment. The chip performs clock and data recovery, serial-to-parallel/parallel-to-serial conversion and frame detection function conforming to the SONET/SDH standards.

The device can be configured to operate under OC-48, OC-24, OC-12, or OC-3 data rates through the rate selection pins or the autorate detection function. An external reference clock operating at 622.08 MHz is required for the recovery loop, and it also provides a stable clock source in the absence of serial data transitions.

The SLK2501 accepts 4 bit LVDS parallel data/clock and generates a NRZ SONET/SDH-compliant signal at OC-3, OC-12, OC-24 or OC-48 rates. It also recovers the data and clock from the serial SONET stream and demultiplexes it into 4-bit LVDS parallel data for full duplex operation. TXDATA0 and RXDATA0 are the first bits that are transmitted and received in time, respectively. The serial interface is a low jitter, PECL compatible differential interface.

The SLK2501 provides a comprehensive suite of built-in tests for self-test purposes including local and remote loopback and PRBS (2<sup>7</sup>-1) generation and verification.

The device comes in a 100-pin VQFP package that requires a single 2.5-V supply with 3.3-V tolerant inputs on the control pins. The SLK2501 is very power efficient, dissipating less than 900 mW at 2.488 Gbps, the OC-48 data rate, and it is characterised for operation from -40°C to 85°C.

#### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE
	-40°C to 85°C



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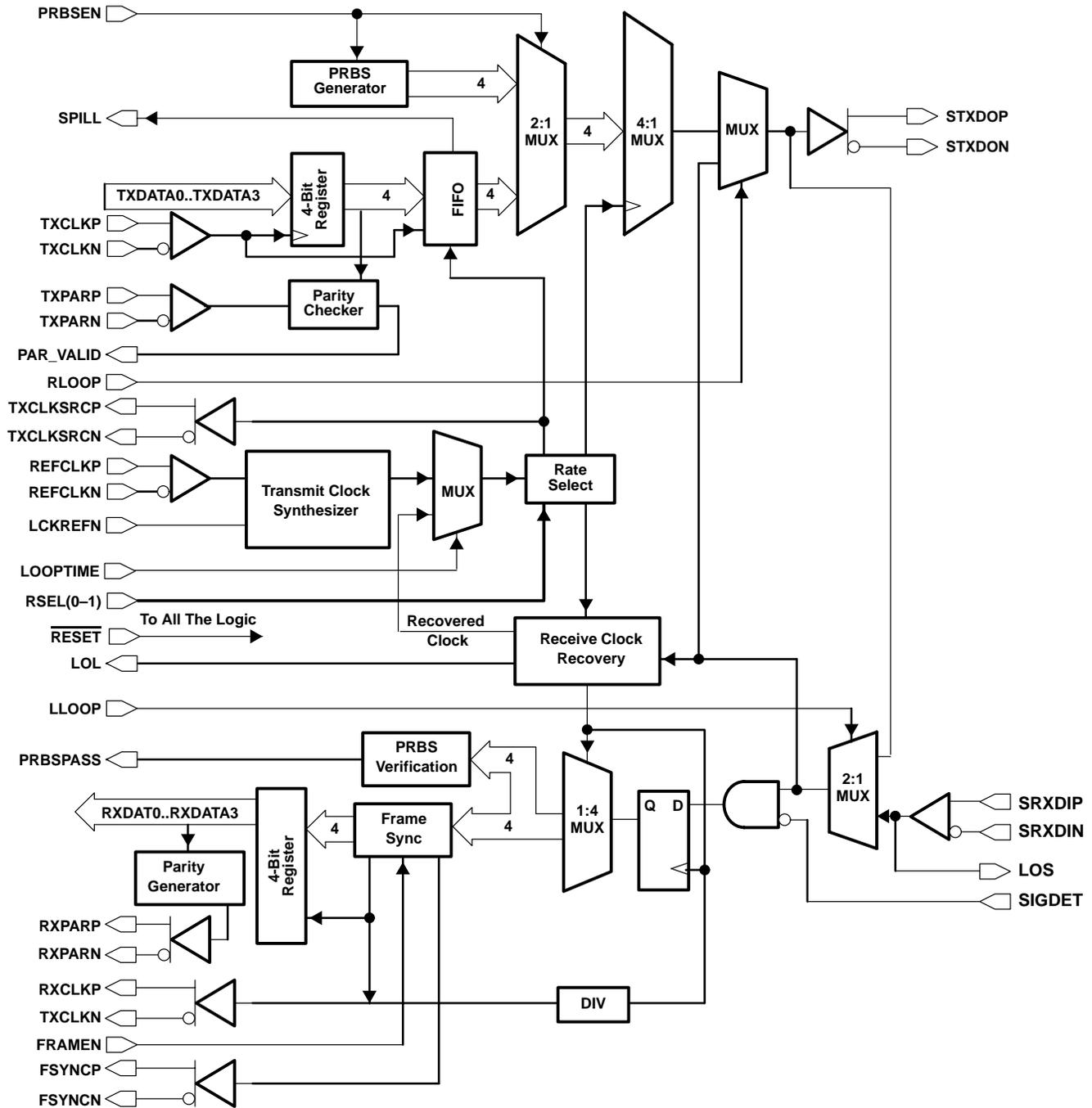


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## block diagram

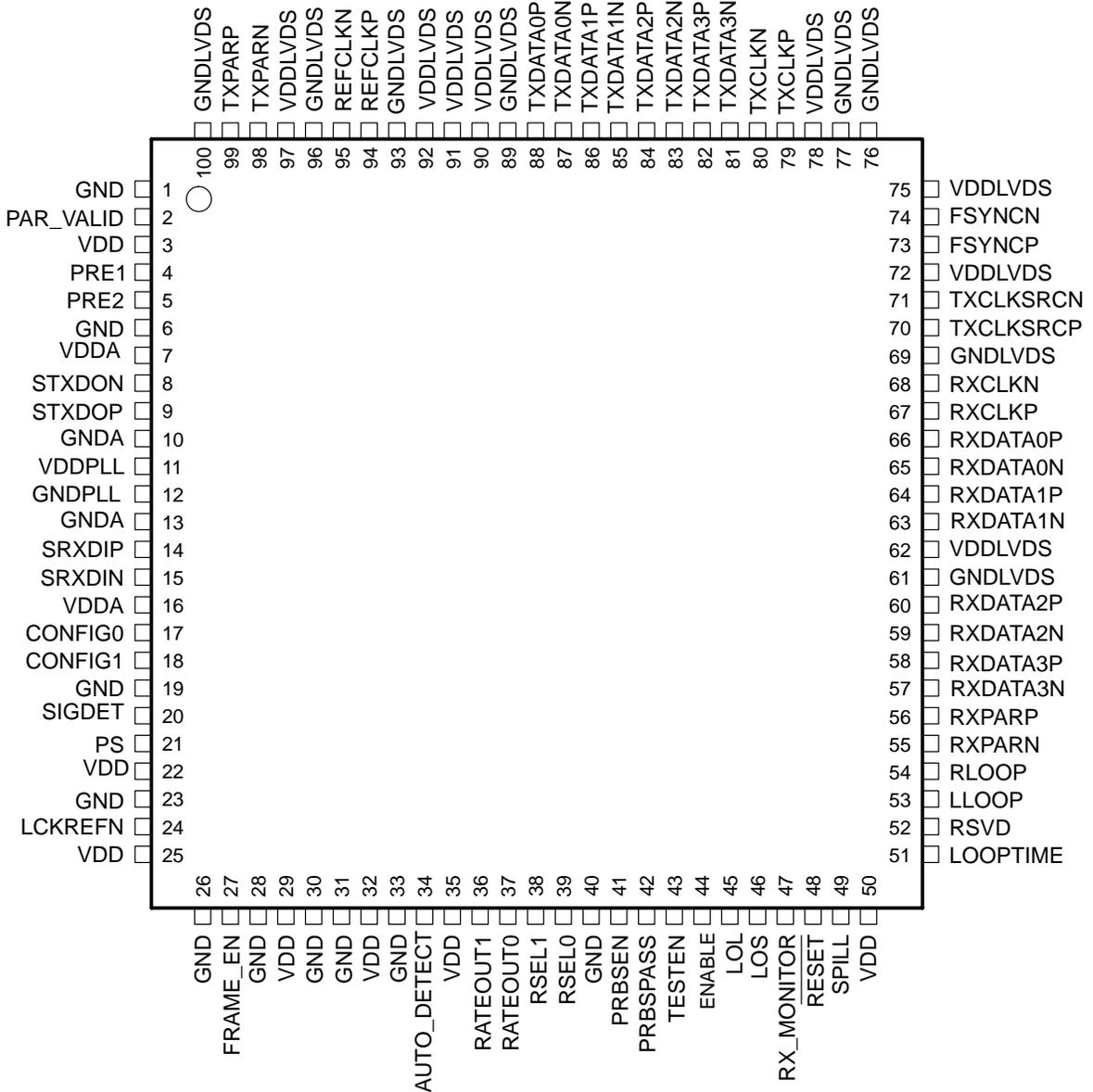


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### PZP PACKAGE (TOP VIEW)



# SLK2501

## OC-48/24/12/3 SONET/SDH MULTIRATE TRANSCEIVER

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### Terminal Functions

#### clock pins

TERMINAL NAME	NO.	TYPE	DESCRIPTION
REFCLKP, REFCLKN	94 95	LVDS/PECL compatible input	Differential reference input clock. There is an on-chip 100-Ω termination resistor differentially placed between REFCLKP and REFCLKN. The dc bias is also provided on-chip for ac-coupled case.
TXCLKP, TXCLKN	79 80	LVDS input	Transmit data clock. The data on TXDATA(0:3) is latched on the rising edge of TXCLKP.
TXCLKSRCP, TXCLKSRCN	70 71	LVDS output	Transmit clock source. A clock source generated from the SLK2501 to the downstream device (i.e., framer) that could be used by the downstream device to transmit data back to the SLK2501. This clock is frequency-locked to the local reference clock.
RXCLKP, RXCLKN	67 68	LVDS output	Receive data clock. The data on RXDATA(0:3) is on the falling edges of RXCLKP. The interface of RXDATA(0:3) and RXCLKP is source synchronous (refer to Figure 7).

#### serial side data pins

TERMINAL NAME	NO.	TYPE	DESCRIPTION
STXDOP, STXDON	9 8	PECL compatible output	Transmit differential pairs; high speed serial outputs.
SRXDIP, SRXDIN	14 15	PECL compatible input	Receive differential pairs; high speed serial inputs.

#### parallel side data pins

TERMINAL NAME	NO.	TYPE	DESCRIPTION
TXDATA[0:3] P/N	88–81	LVDS input	Transmit data pins. Parallel data on this bus is clocked on the rising edge of TXCLKP. TXDATA0 is the first bit transmitted in time.
TXPARP, TXPARN	99 98	LVDS input	Transmit data parity input
RXDATA[0:3] P/N	66–63, 60–57	LVDS output	Receive data pins. Parallel data on this bus is valid on the falling edge of RXCLKP (refer to Figure 7). RXDATA0 is the first bit received in time.
RXPARP, RXPARN	56 55	LVDS output	Receive data parity output
FSYNCP, FSYNCN	73 74	LVDS output	Frame sync pulse. This signal indicates the frame boundaries of the incoming data stream. If the frame-detect circuit is enabled, FSYNC pulses for four RXCLKP and RXCLKN clock cycles, when it detects the framing patterns.



**Terminal Functions(Continued)**

**control/status pins**

TERMINAL NAME	NO.	TYPE	DESCRIPTION
RSEL0, RSEL1	39 38	TTL input (with pulldown)	Data rate configuration pins. Put the device under one of the four data rate operations: OC-48, OC-24, OC-12 or OC-3.
CONFIG0, CONFIG1	17 18	TTL input (with pulldown)	Configuration pins. Put the device under one of the four operation modes: TX only, RX only, transceiver, or repeater mode.
PRE1, PRE2	4 5	TTL input (with pulldown)	Programmable preemphasis control. Combinations of these two bits can be used to optimize serial data transmission.
$\overline{\text{RESET}}$	48	TTL input	TXFIFO and LOL reset pin. Low is reset and high is normal operation.
AUTO_DETECT	34	TTL input (with pulldown)	Data rate autodetect enable. Enable the autodetection function for different data rates.
LLOOP	53	TTL input (with pulldown)	Local loopback enable. When high, the serial output is internally looped back to its serial input
RLOOP	54	TTL input (with pulldown)	Remote loopback enable. When high, the serial input is internally looped back to its serial output with the timing extracted from the serial data.
ENABLE	44	TTL input (with pullup)	Standby enable. When this pin is held low, the device is disabled for IDDQ testing. When high, the device operates normally.
FRAME_EN	27	TTL input (with pullup)	Frame sync enable. When this pin is asserted high, the frame synchronization circuit for byte alignment is turned on.
PRBSEN	41	TTL input (with pulldown)	PRBS testing enable. When this pin is asserted high, the device is put into the PRBS testing mode.
SIGDET	20	TTL input (with pulldown)	Signal detect. This pin is generally connected to the output of an optical receiver. This signal may be active high or active low depending on the optical receiver. The SIGDET input is XORed with the PS pin to select the active state. When SIGDET is in the inactive state, data is processed normally. When activated, indicating a loss of signal event, the transmitter transmits all zeroes and force the LOS signal to go high.
PS	21	TTL input (with pulldown)	Polarity select. This pin, used with the SIGDET pin, sets the polarity of SIGDET. When high, SIGDET is an active low signal. When low, SIGDET is an active high signal.
RX_MONITOR	47	TTL input (with pulldown)	RX parallel data monitor in repeater mode. This pin is only used when the device is put under repeater mode. When high, the RX demux circuit is enabled and the parallel data is presented. When low, the demux is shut down to save power.
LCKREFN	24	TTL input (with pullup)	Lock to reference. When low, RXCLKP/N output is forced to lock to REFCLK. When high, RXCLKP/N is the divided down clock extracted from the receive serial data.
LOOPTIME	51	TTL input (with pulldown)	Loop timing mode. When high, the PLL for clock synthesizer is bypassed. The recovered clock timing is used to send the transmit data.
TESTEN	43	TTL input (with pulldown)	Production test mode enable. This pin should be left unconnected or tied low.
RATEOUT0, RATEOUT1	37 36	TTL output	Autorate detection outputs. When AUTO_DETECT is high, the autodetection circuit generates these two bits to indicate the data rates for the downstream device.
LOL	45	TTL output	Loss of lock. When the clock recovery loop has locked to the input data stream and the phase differs by less than 100 ppm from REFCLK then LOL is high. When the phase of the input data stream differs by more than 100 ppm from REFCLK, then LOL is low. If the difference is too big (> 500 ppm), the LOL output is not valid.
LOS	46	TTL output	Loss of signal. When no transitions appear on the input data stream for more than 2.3 $\mu$ s, a loss of signal occurs and LOS goes high. The device also transmits all zeroes downstream using REFCLK as its clock source. When a valid SONET signal is received the LOS signal goes low.

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### Terminal Functions(Continued)

#### control/status pins (continued)

TERMINAL NAME	NO.	TYPE	DESCRIPTION
PRBSPASS	42	TTL output	PRBS test result. This pin reports the status of the PRBS test results (High = pass). When PRBSEN is disabled, the PRBSPASS pin is set low. When PRBSEN is enabled and a valid PRBS is received, then the PRBSPASS pin is set high.
PAR_VALID	2	TTL output	Parity checker output. The internal parity checker on the parallel side of the transmitter checks for even parity. If there is a parity error, the pin is pulsed low for two clock cycles.
SPILL	49	TTL output	TX FIFO collision output

#### voltage supply and reserved pins

TERMINAL NAME	NO.	TYPE	DESCRIPTION
VDDLVD	62, 72, 75, 78, 90, 91, 92, 97	Supply	LVDS supply voltage (2.5 V)
GNDLVDS	61, 69, 76, 77, 89, 93, 96, 100	Ground	LVDS ground
VDD	3, 22, 25, 29, 32, 35, 50	Supply	Digital logic supply voltage (2.5 V)
GND	1, 6, 19, 23, 26, 28, 30, 31, 33, 40	Ground	Digital logic ground
VDDA	7, 16	Supply	Analog voltage supply (2.5 V)
GND A	10, 13	Ground	Analog ground
VDDPLL	11	Supply	PLL voltage supply (2.5 V)
GNDPLL	12	Supply	PLL ground
RSVD	52	Reserved	This pin needs to be tied to ground or left floating for normal operation.



## detailed description

The SLK2501 is designed to support OC-48/24/12/3. The operating data speed can be configured through RSEL0 and RSEL1 pins as indicated in Table 1.

**Table 1. Data Rate Select**

SERIAL DATA RATE	RSEL0	RSEL1	PARALLEL LVDS DATA RATE	TXCLK/RXCLK
OC-48:2.488 Gb/s	0	0	622.08 Mbps	622.08 MHz
OC-24:1.244 Gb/s	1	0	311.04 Mbps	311.04 MHz
OC-12:622 Mb/s	0	1	155.52 Mbps	155.52 MHz
OC-3:155.52 Mb/s	1	1	38.88 Mbps	38.88 MHz

The user can also enable the autorate detection circuitry through the AUTO\_DETECT pin. The device automatically detects the OC-N of the data line rate and generates two bits of output to indicate the data rate to other devices in the system. When using AUTO\_DETECT, RSEL0 and RSEL1 need to be set to 00 or be unconnected.

**Table 2. Data Rate Reporting Under Autorate Detection Mode**

SERIAL DATA RATE	RATEOUT0	RATEOUT1	PARALLEL LVDS DATA RATE	TXCLK/RXCLK
OC-48:2.488 Gb/s	0	0	622.08 Mbps	622.08 MHz
OC-24:1.244 Gb/s	1	0	311.04 Mbps	311.04 MHz
OC-12:622 Mb/s	0	1	155.52 Mbps	155.52 MHz
OC-3:155.52 Mb/s	1	1	38.88 Mbps	38.88 MHz

The SLK2501 has four operational modes controlled by two configuration pins. These operational modes are listed in Table 3. When the device is put in a certain mode, unused circuit blocks are powered down to conserve the system power.

While the transceiver mode, transmit only mode, and receive only mode are straightforward, the repeater mode of operation is shown in Figure 5. The receive serial data is recovered by the extracted clock, and it is then sent back out on the transmit serial outputs. The data eye is open both vertically and horizontally in this process. In the repeater mode, user can select to turn on the RX demux function through RX\_MONITOR pin and allow the parallel data to be presented. This feature enables the repeater device not only to *repeat* but also to *listen in*.

**Table 3. Operational Modes**

MODE	CONFIG0	CONFIG1	DESCRIPTION
1	0	0	Full duplex transceiver mode
2	0	1	Transmit only mode
3	1	0	Receive only mode
4	1	1	Repeater mode

## high-speed electrical interface

The high-speed serial I/O uses a PECL compatible interface. The line could be directly coupled or ac-coupled. Refer to Figures 10 and 11 for configuration details. As shown in the figures, an on-chip 100-Ω termination resistor is placed differentially at the receive end.

The PECL output also provide preemphasis for compensating ac loss when driving a cable or PCB backplane over long distance. The level of the preemphasis is programmable via PRE1 and PRE2 pins. Users can use software to control the strength of the preemphasis to optimize the device for a specific system requirement.

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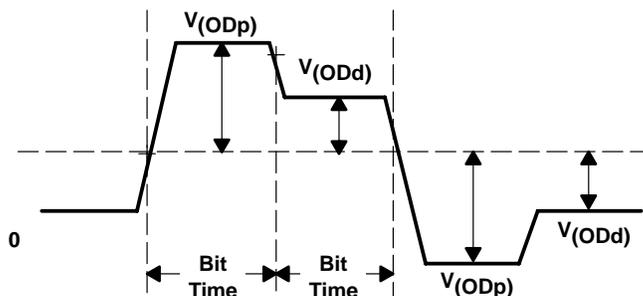
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## detailed description (continued)

**Table 4. Programmable De-emphasis**

PRE1	PRE2	DE-EMPHASIS LEVEL ( $V_{ODp}/V_{ODd}^{\dagger}-1$ )
0	0	De-emphasis disabled
1	0	10%
0	1	20%
1	1	30%

<sup>†</sup>  $V_{ODp}$ : Differential voltage swing when there is a transition in the data stream.  
 $V_{ODd}$ : Differential voltage swing when there is no transition in the data stream.



**Figure 1. Output Differential Voltage Under De-emphasis**

### LVDS parallel data interface

The parallel data interface consists of a 4-bit parallel LVDS data and clock. The device conforms to OIF99.102 specification when operating at the OC-48 rate. When operating at lower serial rates the clock and data frequency are scaled down accordingly, as indicated in Table 1. The parallel data TXDATA[0:3] is latched on the rising edge of the TXCLK and then is sent to a data FIFO to resolve any phase difference between TXCLK and REFCLK. If there is a FIFO overflow condition, the pin SPILL is set high. The FIFO resets itself to realign between two clocks. The internal PLL for the clock synthesizer is locked to the REFCLK, and it is used as the timing to serialize the parallel data (except for the loop timing mode where the recovered clock is used). On the receive side, RXDATA[0:3] is updated on the rising edge of RXCLK. Figures 7 and 8 show the timing diagram for the parallel interface.

The SLK2501 also has a built-in parity checker and generator for error detection of the LVDS interface. On the transmit side, it accepts the parity bit, TXPARP/N, and performs the parity checking function for even parity. If an error is detected, it pulses the PAR\_VALID pin low for two clock cycles. On the receive side, the parity bit, RXPARP/N, is generated for the downstream device for parity error checking.

Differential termination 100-Ω resistors are included on-chip between TXDATAP/N and TXCLKP/N.

### reference clock

The device accepts a 622.08 MHz clock. The REFCLK input is compatible with the LVDS level and also the 3.3-V LVPECL level using ac-coupling. A 100-Ω differential termination resistor is included on-chip, as well as a dc biasing circuit (3 kΩ to VDD and 4.5 kΩ to GND) for the ac-coupled case. A high quality REFCLK must be used on systems required to meet SONET/SDH standards. For non-SONET/SDH compliant systems, loose tolerances may be used.

**detailed description (continued)**

**clock and data recovery**

The CDR unit of SLK2501 recovers the clock and data from the incoming data streams.

In the event of receive data loss, the PLL automatically locks to the local REFCLK to maintain frequency stability. If the frequency of the data differs by more that 100 ppm with respect to the REFCLK frequency, the LOL pin is asserted as a warning. Actual loss of lock occurs if the data frequency differs by more than 170 ppm.

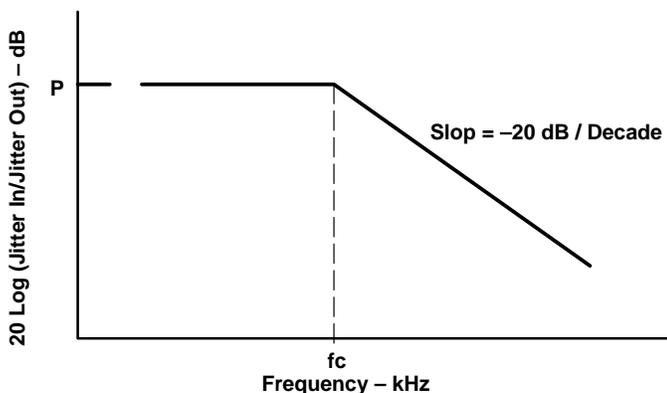
**minimum transition density**

The loop filter transfer function is optimized to enable the CDR to track ppm difference in the clocking and tolerate the minimum transition density that can be received in a SONET data signal ( $\pm 20$  ppm). The transfer function yields a typical capture time of 3500 bit times for random incoming NRZ data after the device is powered up and achieves frequency locking.

The device tolerates up to 72 consecutive digits (CID) without sustaining an error.

**jitter transfer**

The jitter transfer is less than the mask shown in Figure 2 (GR-253 Figure 5-27). Jitter transfer function is defined as the ratio of jitter on the output signal to the jitter applied on the input signal versus frequency. The input sinusoidal jitter amplitude is applied up to the mask level in the jitter tolerance requirement (see Figure 3).



OC-N/STS-N LEVEL	$f_c$ (kHz)	P (dB)
3	130	0.1
12	500	0.1
24	Not Specified	
48	2000	0.1

**Figure 2. Jitter Transfer**

**jitter tolerance**

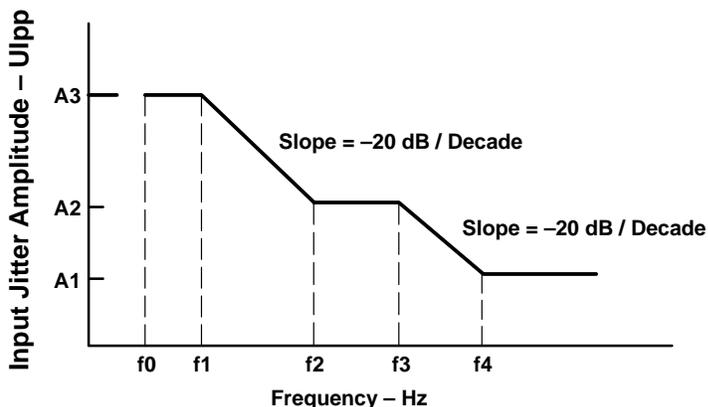
Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes the equivalent 1 dB optical/electrical power penalty. This refers to the ability of the device to withstand input jitter without causing a recovered data error. The device has a jitter tolerance that exceeds the mask shown in Figure 3 (GR-253 Figure 5-28). This jitter tolerance is specified using a pseudorandom data pattern of  $2^{31} - 1$ .

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### jitter tolerance (continued)



OC-N/STS-N LEVEL	f0 (Hz)	F1 (Hz)	F2 (Hz)	F3 (kHz)	F4 (kHz)	A1 (UIpp)	A2 (UIpp)	A3 (UIpp)
3	10	30	300	6.5	65	0.15	1.5	15
12	10	30	300	25	250	0.15	1.5	15
24	Not specified							
48	10	600	6000	100	1000	0.15	1.5	15

Figure 3. Input Jitter Tolerance

### jitter generation

The jitter of a serial clock and serial data outputs must not exceed  $0.01 U_{I_{rms}}/0.1 U_{I_{p-p}}$  when a serial data with no jitter is presented to the inputs. The measurement bandwidth for intrinsic jitter is 12-kHz to 20-MHz.

### loop timing mode

When LOOPTIME is high, the clock synthesizer used to serialize the transmit data is bypassed and the timing is provided by the recovered clock. However, REFCLK is still needed for the recovery loop operation.

### loss of lock indicator

The SLK2501 has a lock detection circuit to monitor the integrity of the data input. When the clock recovery loop is locked to the input serial data stream, the LOL signal goes high. If the recovered clock frequency deviates from the reference clock frequency by more than 100 ppm, LOL goes low. If the data stream clock rate deviates by more than 170 ppm, loss of lock occurs. If the data streams clock rate deviates more than 500 ppm from the local reference clock, the LOL output status might be unstable. Upon power up, the LOL goes low until the PLL is close to phase lock with the local reference clock.

### loss of signal

The loss of signal (LOS) alarm is set high when no transitions appear in the input data path for more than 2.3  $\mu$ s. The LOS signal becomes active when the above condition occurs. If the serial inputs of the device are ac-coupled to its source, the ac-couple cap needs to be big enough to maintain a signal level above the threshold of the receiver for the 2.3  $\mu$ s no transition period. Once activated, the LOS alarm pin is latched high until the receiver detects an A1A2 pattern. The recovered clock (RXCLK) is automatically locked to the local reference when LOS occurs. The parallel data (RXDATAx) may still be processed even when LOS is activated.



## **detailed description (continued)**

### **signal detect**

The SLK2501 has an input SIGDET pin to force the device into the loss of signal state. This pin is generally connected to the signal detect output of the optical receiver. Depending on the optics manufacturer, this signal can be either active high or active low. To accommodate the differences, a polarity select (PS) is used. For an active low, SIGDET input sets the PS pin high. For an active high, SIGDET input sets the PS pin low. When the PS signal pin and SIGDET are of opposite polarities, the loss of signal state is generated and the device transmits all zeroes downstream.

### **multiplexer operation**

The 4-bit parallel LVDS data is clocked into an input buffer by a clock derived from the synthesized clock. The data is then clocked into a 4:1 multiplexer. The D0 bit is the most significant bit and is shifted out first in the serial output stream.

### **demultiplexer operation**

The serial 2.5 Gbps data is clocked into a 1:4 demultiplexer by the recovered clock. The D0 bit is the first bit that is received in time from the input serial stream. The 4-bit parallel data is then sent to the LVDS driver along with the divided down recovered clock.

### **frame synchronization**

The SLK2501 has a SONET/SDH-compatible frame detection circuit that can be enabled or disabled by the user. Frame detection is enabled when the FRAMEN pin is high. When enabled it detects the A1, A2 framing pattern, which is used to locate and align the byte and frame boundaries of the incoming data stream. When FRAMEN is low the frame detection circuitry is disabled and the byte boundary is frozen to the location found when detection was previously enabled.

The frame detect circuit searches the incoming data for three consecutive A1 bytes followed immediately by one A2 byte. The data alignment circuit then aligns the parallel output data to the byte and frame boundaries of the incoming data stream. During the framing process the parallel data bus will not contain valid and aligned data. Upon detecting the third A1, A2 framing patterns that are separated by 125  $\mu$ s from each other, the FSYNC signal goes high for four RXCLK cycles, indicating frame synchronization has been achieved.

The probability that random data in a SONET/SDH data stream will mimic the framing pattern in the data payload is extremely low. However, there is a state machine built in to prevent false reframing if a framing pattern does show up in the data payload.

### **testability**

The SLK2501 has a comprehensive suite of built-in self-tests. The Loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable pin allows for all circuitry to be disabled so that an Iddq test can be performed. The PRBS function allows for a BIST (built-in self-test).

### **IDDQ function**

When held low, the ENABLE pin disables all quiescent power in both the analog and digital circuitry. This allows for Iddq testing on all power supplies and can also be used to conserve power when the link is inactive.

### **local loopback**

The LLOOP signal pin controls the local loopback. When LLOOP is high, the loopback mode is activated and the parallel transmit data is selected and presented on the parallel receive data output pins. The parallel transmit data is also multiplexed and presented on the high-speed serial transmit pins. Local Loopback can only be enabled when the device is under transceiver mode.

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## detailed description (continued)

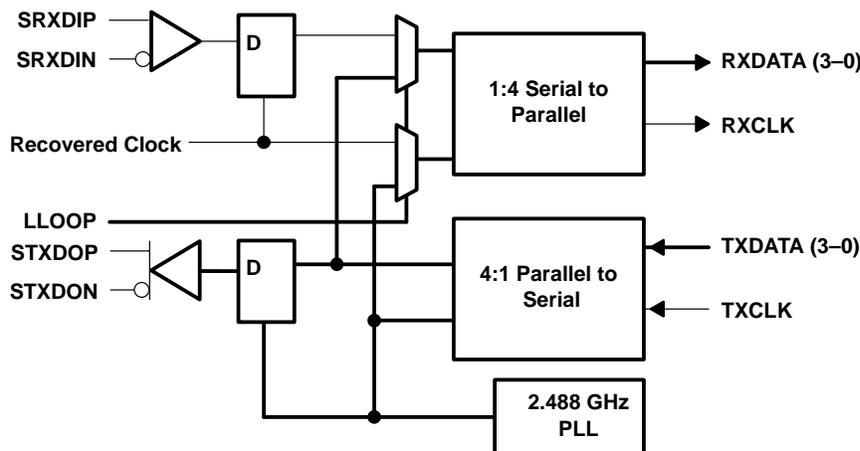


Figure 4. Local Loopback Data Path

## remote loopback

The RLOOP signal pin controls the remote loopback. When RLOOP is high the serial receive data is selected and presented on the serial transmit data output pins. The serial received data is also demultiplexed and presented on the parallel receive data pins. The remote loop can be enabled only when the device is under transceiver mode. When the device is put under the repeater mode with RX\_MONITOR high, it performs the same function as remote loopback.

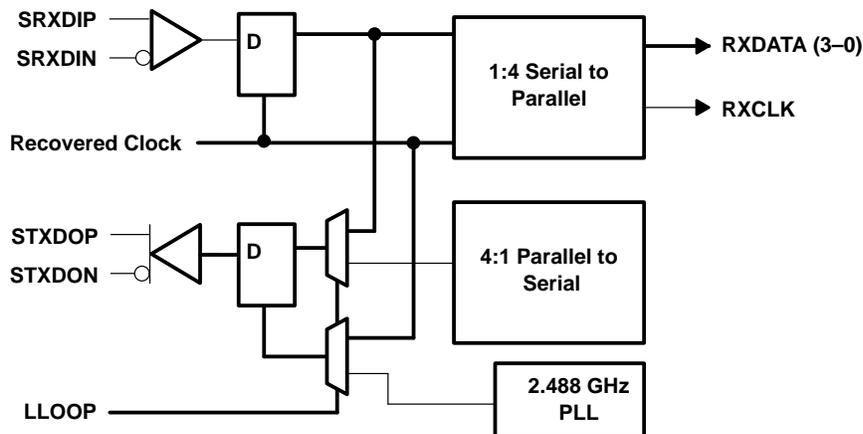


Figure 5. Remote Loopback Data Path/Repeater Mode Operation

## PRBS

The SLK2501 has two built-in pseudorandom bit stream (PRBS) functions. The PRBS generator is used to transmit a PRBS signal. The PRBS verifier is used to check and verify a received PRBS signal.

When the PRBSEN pin is high, the PRBS generator and verifier are both enabled. A PRBS is generated and fed into the parallel transmitter input bus. Data from the normal input source is ignored in PRBS mode. The PRBS pattern is then fed through the transmitter circuitry as if it was normal data and sent out by the transmitter. The output can be sent to a bit error rate tester (BERT) or to the receiver of another SLK2501. If an error occurs in the PRBS pattern, the PRBSPASS pin is set low for two RXCLKP/N cycles.

**detailed description (continued)**

**power-on reset**

Upon application of minimum valid power, the SLK2501 generates a power-on reset. During the power-on reset the PRXDATA[0:3] signal pins goes to 3-state. RXCLKP and RXCLKN are held low. The length of the power-on reset cycle is dependent upon the REFCLKP and REFCLKN frequency but is less than 1- $\mu$ s in duration.

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>**

Supply voltage, $V_{DD}$ .....	–0.3 to 3 V
Voltage range: TTL input terminals .....	–0.3 to 4 V
LVDS terminals .....	–0.3 to 3 V
Any other terminal except above .....	–0.3 to $V_{DD} + 0.3$ V
Package power dissipation, $P_D$ .....	See Dissipation Rating Table
Storage temperature, $T_{stg}$ .....	–65°C to 150°C
Electrostatic discharge .....	HBM: 2 kv
Characterized free-air operating temperature range, $T_A$ .....	–40°C to 85°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds .....	260°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>§</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
PZP <sup>‡</sup>	3.4 W	33.78 mW/°C	1.3 W
PZP <sup>¶</sup>	2.27 W	22.78 mW/°C	0.911 W

<sup>‡</sup> 2 oz trace and copper pad with solder.

<sup>§</sup> This is the inverse of the traditional junction-to-ambient thermal resistance ( $R_{\theta JA}$ ).

<sup>¶</sup> 2 oz trace and copper pad without solder.

**recommended operating conditions**

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}$		2.3	2.5	2.7	V
Power dissipation, $P_D$	Frequency = 2.488 Gb/sec, PRBS pattern		700	900	mW
Shutdown current	Enable = 0, $V_{dda}$ , $V_{dd}$ pins, $V_{dd} = \text{max}$		20		$\mu$ A
Operating free-air temperature, $T_A$		–40		85	°C

**start up sequence**

To ensure proper start up, follow one of the following steps when powering up the SLK2501.

1. Keep ENABLE (pin 44) low until power supplies and reference clock have become stable.
2. Drive ENABLE (pin 44) low for at least 30 ns after power supplies and reference clock have become stable.

The following step is recommended with either of the above two sequences.

3. Drive  $\overline{\text{RESET}}$  low for at least 10 ns after link has become stable to center the TXFIFO.

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### electrical characteristics over recommended operating conditions (unless otherwise noted)

#### TTL

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IH</sub>	High-level input voltage		2		3.6	V
V <sub>IL</sub>	Low-level input voltage				0.80	V
I <sub>IH</sub>	Input high current	V <sub>DD</sub> = MAX, V <sub>IN</sub> = 2 V			40	μA
I <sub>IL</sub>	Input low current	V <sub>DD</sub> = MAX, V <sub>IN</sub> = 4 V	-40			μA
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	2.10	2.3		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OH</sub> = 1 mA		0.25	0.5	V
C <sub>I</sub>	Input capacitance				4	pF

#### LVDS input signals

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>I</sub>	Input voltage		825		1575	mV
V <sub>ID(th)</sub>	Input differential threshold voltage		100			mV
C <sub>I</sub>	Input capacitance				3	pF
R <sub>I</sub>	Input differential impedance	On-chip termination	80	100	120	Ω
t <sub>su</sub>	Input setup time requirement	See Figure 8	300			ps
t <sub>h</sub>	Input hold time requirement	See Figure 8	300			ps
T <sub>(duty)</sub>	Input clock duty cycle		40%		60%	

#### LVDS output signals

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OD</sub>	Output differential voltage	R <sub>L</sub> = 100 ±1%	300		800	mV
V <sub>OS</sub>	Output common mode voltage		1070		1375	
ΔV <sub>OD</sub>	Change V <sub>OD</sub> between 1 and 0				25	
ΔV <sub>OS</sub>	Change V <sub>OS</sub> between 1 and 0				25	
I <sub>(SP)</sub> , I <sub>(SN)</sub> , I <sub>(SPN)</sub>	Output short circuit current	Outputs shorted to ground or shorted together			24	mA
I <sub>off</sub>	Power-off current	V <sub>DD</sub> = 0 V			10	μA
t <sub>(cq_min)</sub>	Clock-output time	See Figure 7			100	ps
t <sub>(cq_max)</sub>					100	
t <sub>r</sub> /t <sub>f</sub>	Output transition time	20%to80%	100		300	ps
	Output clock duty cycle		45%		55%	
	Data output to FRAME_SYNC delay		4		7	Bit times

### timing requirements over recommended operating conditions (unless otherwise noted)

#### reference clock (REFCLK)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency tolerance <sup>†</sup>		-20		20	ppm
	Duty cycle		40%	50%	60%	
	Jitter	12 kHz to 20 MHz			3	ps rms
	Frequency range absolute value			622.08		MHz

<sup>†</sup> The ±20 ppm tolerance is required to meet SONET/SDH requirements. For non-SONET/SDH compliant systems, looser tolerances may apply.



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### PLL performance specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PLL startup lock time	$V_{DD}, V_{DDC} = 2.3\text{ V}$ , After REFCLK is stable			1	ms
Acquisition lock time	Valid SONET signal or PRBS OC-48		2031		Bit Times

### serial transmitter/receiver characteristics

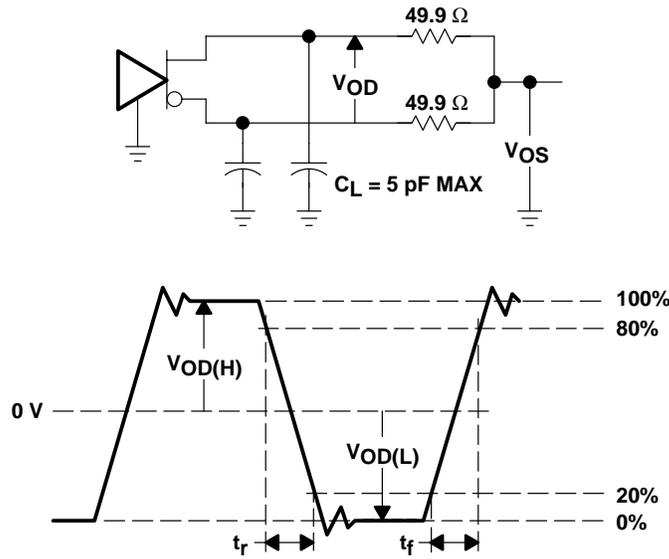
PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{odd} =  STXDOP - STXDON $ , transmit differential output voltage under preemphasis	PRE1 = 0, PRE2 = 0, $R_t = 50$ , See Table 4 and Figure 1	650	850	1000	mV
	PRE1 = 1, PRE2 = 0	550	750	900	
	PRE1 = 0, PRE2 = 1	540	700	860	mV
	PRE1 = 1, PRE2 = 1	500	650	800	
$V_{(CMT)}$ Transmit common mode voltage range	$R_t = 50\ \Omega$	1100	1250	1400	mV
Receiver Input voltage requirement, $V_{id} =  SRXDIP - SRXDIN $		150			mV
$V_{(CMR)}$ Receiver common mode voltage range		1100	1250	2250	mV
$I_l$ Receiver input leakage		-550		550	$\mu\text{A}$
$R_l$ Receiver differential impedance		80	100	120	$\Omega$
$C_l$ Receiver input capacitance				1	pF
$t_d(\text{TX\_Latency})$				50	Bit Times
$t_d(\text{RX\_Latency})$				50	

### serial differential switching characteristics over recommended operating conditions (unless otherwise noted)

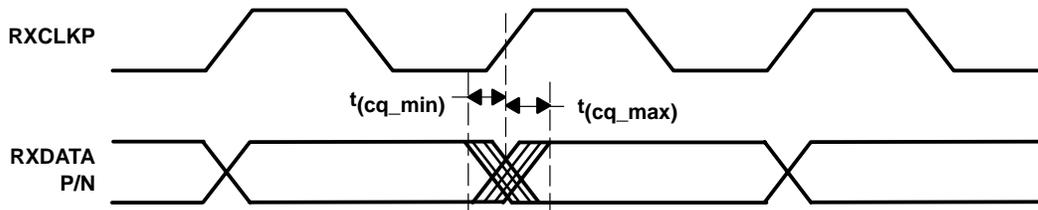
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_t$ Differential signal rise time (20% to 80%)	$R_L = 50\ \Omega$ ,	80	100	140	ps
$t_j$ Output jitter	Jitter-free data, 12 kHz to 20 MHz, RLOOP = 1		0.05	0.1	UI(pp)
Jitter tolerance	RLOOP = 1 See Figure 3				
Jitter transfer	RLOOP = 1 See Figure 2				



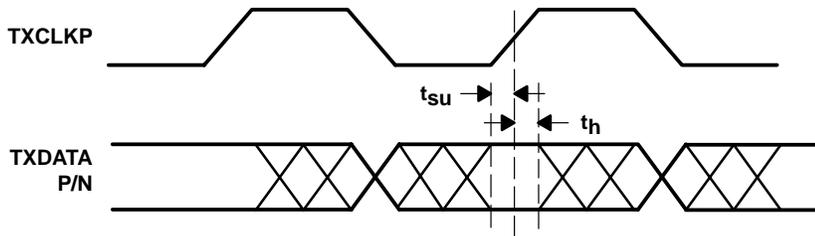
**TYPICAL CHARACTERISTICS**



**Figure 6. Test Load and Voltage Definitions for LVDS Outputs**

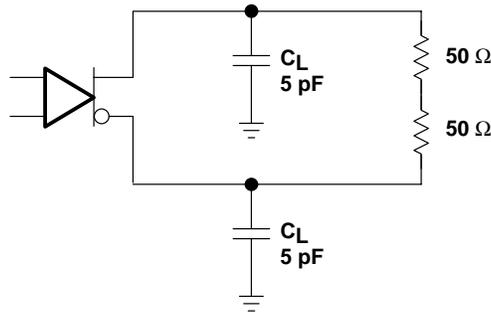


**Figure 7. LVDS Output Waveform**

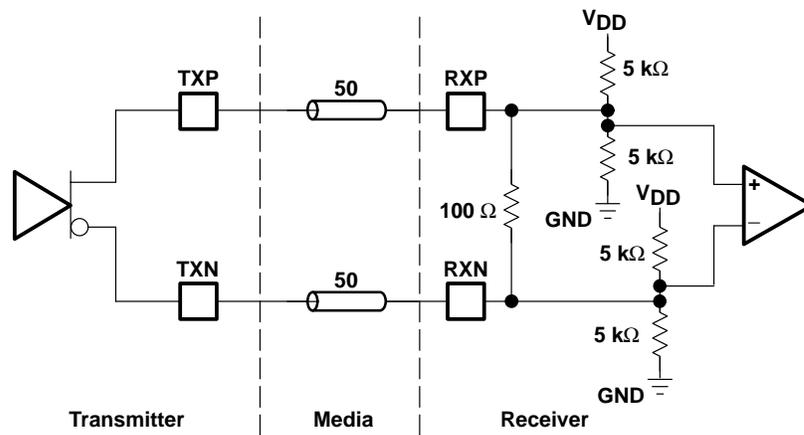


**Figure 8. LVDS Input Waveform**

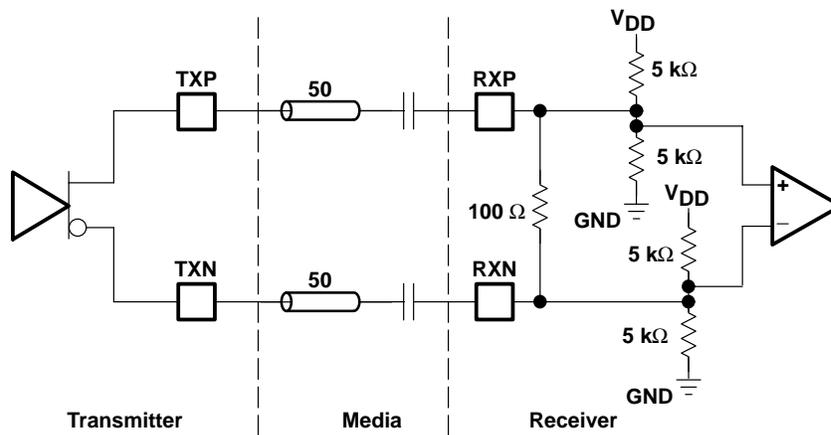
**APPLICATION INFORMATION**



**Figure 9. Transmitter Test Setup**



**Figure 10. High-Speed I/O Directly Coupled Mode**



**Figure 11. High-Speed I/O AC Coupled Mode**

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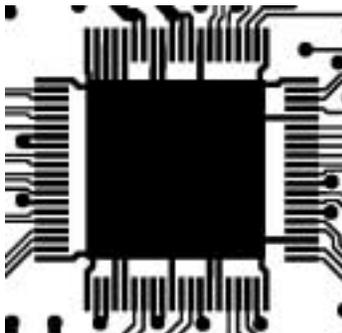
### APPLICATION INFORMATION

#### designing with the PowerPad package

The SLK2501 is housed in high-performance, thermally enhanced, 100-pin PZP PowerPAD packages. Use of a PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Correct device operation requires that the PowerPAD be soldered to the thermal land. Do not run any etches or signal vias under the device, but have only a grounded thermal land, as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keepout area for the 100-pin PZP PowerPAD package is 12 mm × 12 mm.

A thermal land, which is an area of solder-tinned-copper, is required underneath the PowerPAD package. The thermal land varies in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias, depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD™ Thermally Enhanced Package* Application Report, TI literature number SLMA002, available via the TI Web pages beginning at URL <http://www.ti.com>.



**Figure 12. Example of a Thermal Land**

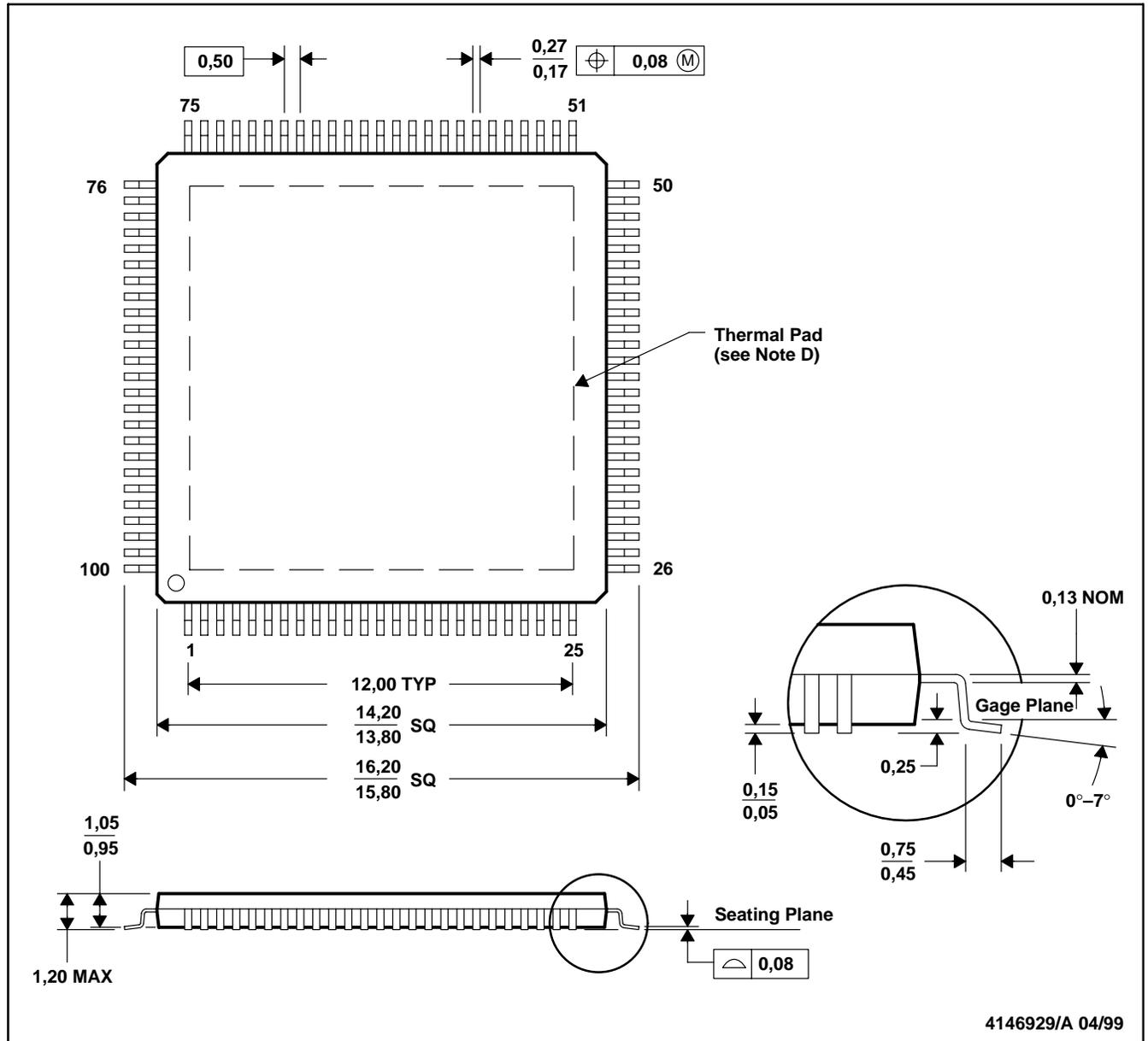
For the SLK2501, this thermal land should be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal terminals. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low-impedance ground plane of the device. More information may be obtained from the TI application note *PHY Layout*, TI literature number SLLA020.

**MECHANICAL DATA**

**PZP (S-PQFP-G100)**

**PowerPAD™ PLASTIC QUAD FLATPACK**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
  - E. Falls within JEDEC MS-026

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)  
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### Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265