

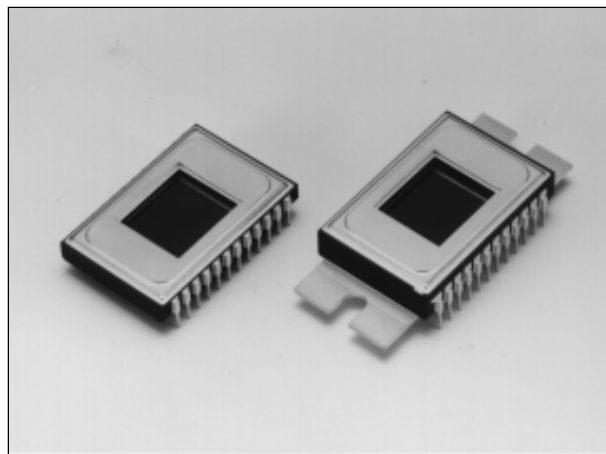
Back-thinned FFT-CCDs

FEATURES

- Greater than 90 % quantum efficiency
- Wide spectrum range
- Low readout noise
- Wide dynamic range
- MPP operation
- Non-cooled types: S7170 series
One-stage TE-cooled types: S7171 series
(Two-stage TE-cooled types are optional.)

APPLICATIONS

- Scientific measuring instrument
- Optical analyzer
- UV imaging
- Bio-photon observation



Hamamatsu Photonics K.K. developed Full-Frame Transfer Charge Coupled Device (FFT-CCD), Multi Pin Phase (MPP) mode back illuminated CCDs S7170-0909, S7171-0909 specifically designed for low-light-level detection in scientific applications. S7170-0909, S7171-0909 have responsivity from the UV to near-IR as well as having low dark current and wide dynamic range. Stability of the spectral response curve is also achieved for high precision measurements.

Either one-stage or two-stage thermoelectric cooler is built into the package. At room temperature operation, the device can be cooled down to -10 °C by one-stage cooler and -30 °C by two-stage cooler, respectively. In addition since both the CCD chip and the thermoelectric cooler are hermetically sealed, no dry air is required, thus allowing easy handling.

■SELECTION GUIDE

Type No.	Cooling	Number of Total Pixels	Number of Active Pixels	Active Area [mm (H) × mm (V)]
S7170-0909	Non-cooled	532 × 520	512 × 512	12.288 × 12.288
S7171-0909	One-stage TE-cooled	532 × 520	512 × 512	12.288 × 12.288

CCD AREA IMAGE SENSORS S7170/S7171 SERIES

■GENERAL RATINGS

Parameter	Specification	
	S7170 series	S7171 series
Pixel Size	24 μm (H) × 24 μm (V)	
Number of Pixels (H × V)	(512 + 20) × (512 + 8)	
Vertical Clock Phase	2 phases	
Horizontal Clock Phase	2 phases	
Output Circuit on Chip	One-stage MOSFET source follower	
Package	24 pin ceramic DIP (refer to Dimensional Outlines)	
Built-in cooler *1	-	One-stage
Window	Sapphire	

*1: Two stage TE-cooler is available upon request.

■ELECTRICAL CHARACTERISTICS (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal Output Frequency	fc	-	-	1	MHz
Charge Transfer Efficiency *2	CTE	-	0.99995	-	-
DC Output Level *3	Vout	-	15	18	V
Output Impedance *3	Zo	-	3	-	kΩ
Power Dissipation *3 *4	P	-	15	-	mW

*2: Measured at half of the full well capacity. CTE is defined per pixel.

*3: The values depend on the load resistance. (Typical, VOD=20 V, Load resistance=22 kΩ)

*4: Power dissipation of the on-chip amplifier.

■ELECTRICAL AND OPTICAL CHARACTERISTICS (Ta=25 °C if not remarked)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation Output Voltage		Vsat	-	Fw × Sv	-	V
Full Well Capacity	Vertical	Fw	-	300,000	-	e ⁻
	Horizontal		-	600,000	-	
CCD Node Sensitivity		Sv	-	3.0	-	μV/e ⁻
Dark Current *5	25 °C	DS	-	3,000	9,000	e ⁻ /pixel/s
MPP Mode (Tentative Data)	0 °C		-	200	600	
Readout Noise *6		Nr	-	6	-	e ⁻ rms
Dynamic Range *7	Line Binning	DR	-	75,000	-	-
	Area Scanning		-	37,500	-	-
Photo Response Non-Uniformity *8		PRNU	-	-	±10	%
Spectral Response Range		λ	-	200 to 1100	-	nm

*5: Dark signal doubles for every 5 to 7 °C.

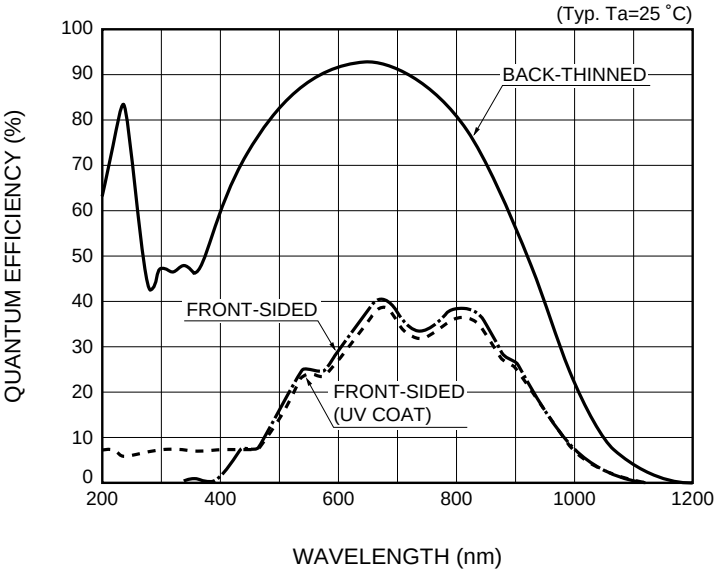
*6: Operating frequency is 150 kHz.

*7: Dynamic Range (DR) = Full Well/Readout Noise

*8: Measured at the half of the full well capacity.

$$\text{Photo Response Non-Uniformity (PRNU) [\%]} = \frac{\text{Fixed Pattern Noise (peak to peak)}}{\text{Signal}} \times 100$$

Figure 1: Spectral Response (Without Window) *9

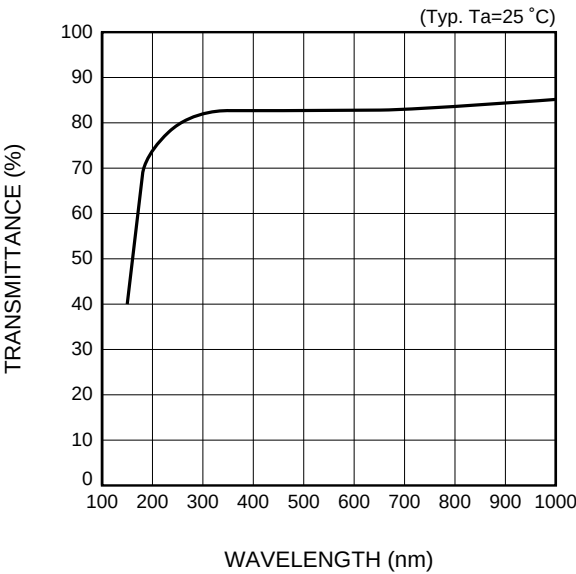


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*9:

- Window-less type is not available now.
- Spectral response with sapphine window is decreased by the transmittance (refer to Fig. 2)

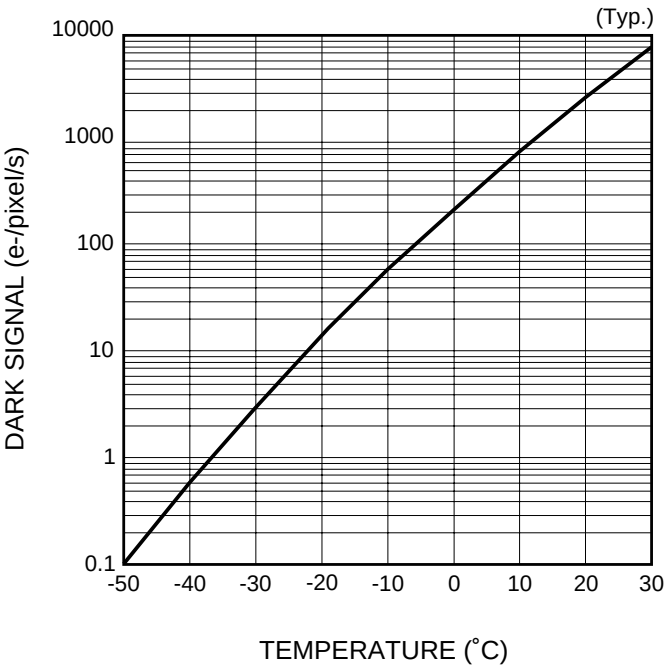
Figure 2: Spectral Transmittance Characteristic of window material



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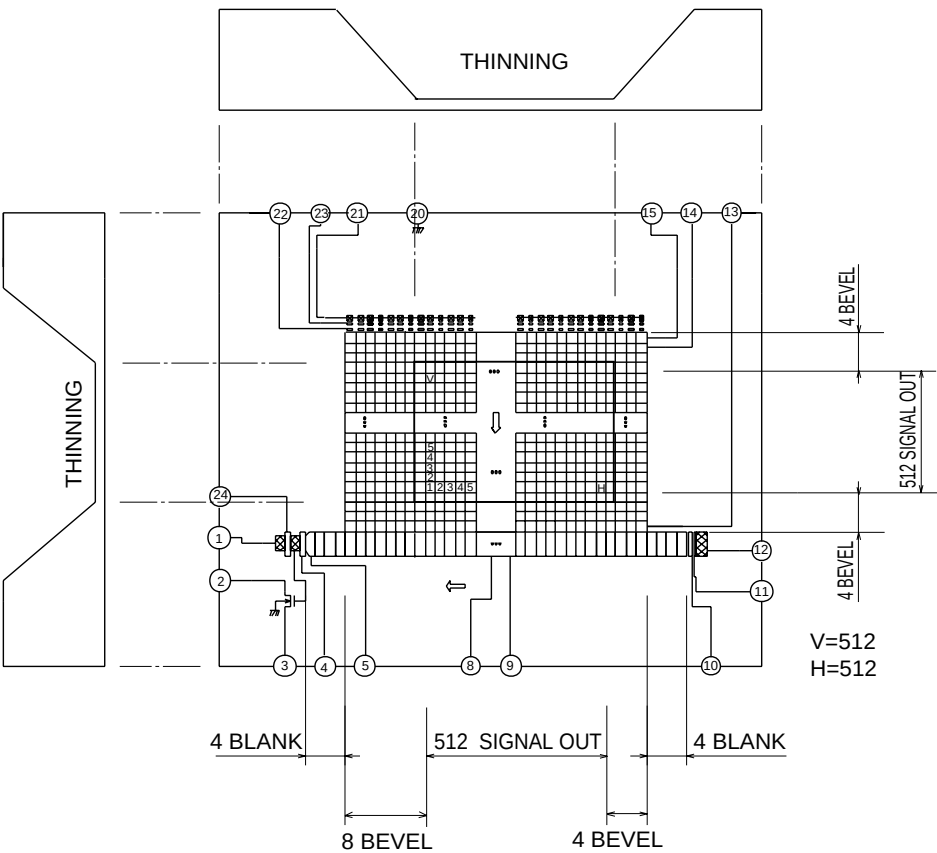
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Figure 3: Dark Signal vs. Temperature



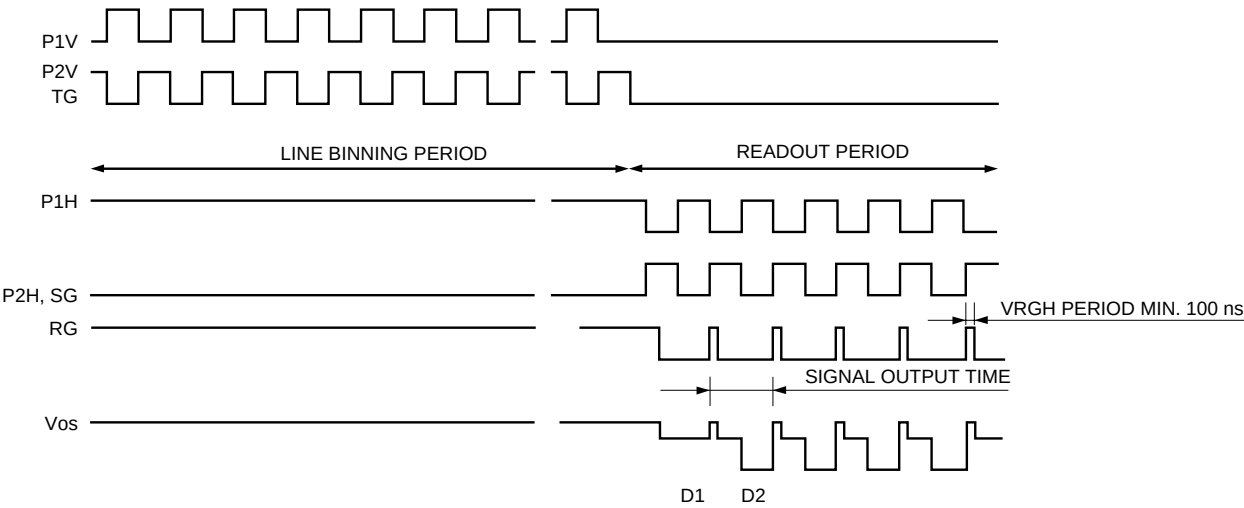
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Figure 4: Device Structure



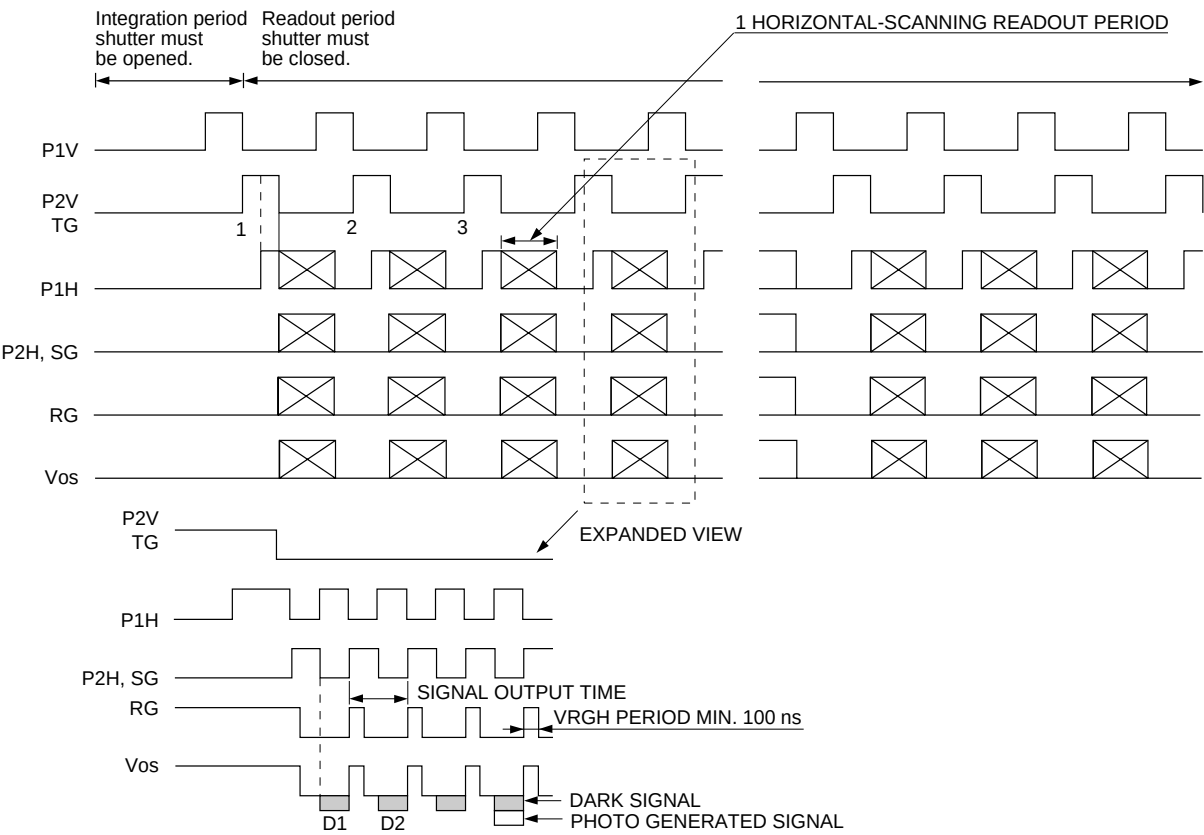
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Figure 5: Pulse Timing Chart (Line Binning)



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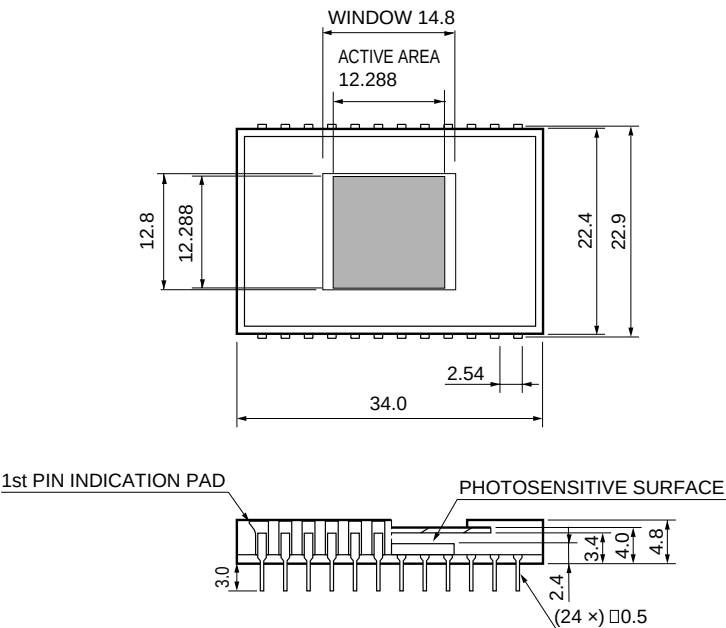
Figure 6: Pulse Timing Chart (Area Scanning)



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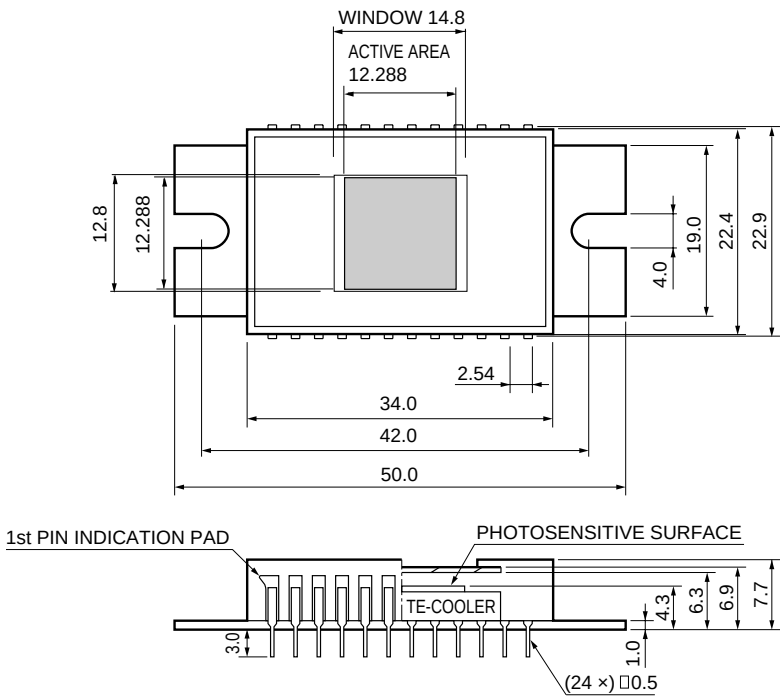
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Figure 7: Dimensional Outlines (Unit: mm)
S7070-0909



KMPDA0084EA

S7071-0909



KMPDA0085EA

PIN CONNECTIONS

Pin No.	S7170 Series		S7171 Series		Remark (Standard Operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset Drain	RD	Reset Drain	+12 V
2	OS	Output Transistor Source	OS	Output Transistor Source	RL: 10 k to 100 kΩ
3	OD	Output Transistor Drain	OD	Output Transistor Drain	+20 V
4	OG	Output Gate	OG	Output Gate	+3 V
5	SG	Summing Gate	SG	Summing Gate	same pulse as P2H
6	-		-		
7	-		-		
8	P2H	CCD Horizontal Register Clock-2	P2H	CCD Horizontal Register Clock-2	
9	P1H	CCD Horizontal Register Clock-1	P1H	CCD Horizontal Register Clock-1	
10	IG2H	Test Point (Horizontal Input Gate-2)	IG2H	Test Point (Horizontal Input Gate-2)	-8 V
11	IG1H	Test Point (Horizontal Input Gate-1)	IG1H	Test Point (Horizontal Input Gate-1)	-8 V
12	ISH	Test Point (Horizontal Input Source)	ISH	Test Point (Horizontal Input Source)	connect to RD
13	TG * ¹⁰	Transfer Gate	TG * ¹⁰	Transfer Gate	same pulse as P2V
14	P2V	CCD Vertical Register Clock-2	P2V	CCD Vertical Register Clock-2	
15	P1V	CCD Vertical Register Clock-1	P1V	CCD Vertical Register Clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	Peltier-	
19	-		P+	Peltier+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	ISV	Test Point (Vertical Input Source)	ISV	Test Point (Vertical Input Source)	connect to RD
22	IG2V	Test Point (Vertical Input Gate-2)	IG2V	Test Point (Vertical Input Gate-2)	-8 V
23	IG1V	Test Point (Vertical Input Gate-1)	IG1V	Test Point (Vertical Input Gate-1)	-8 V
24	RG	Reset Gate	RG	Reset Gate	

*10: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

CCD AREA IMAGE SENSORS S7170/S7171 SERIES

HAMAMATSU

HAMAMATSU PHOTONICS K.K., Solid State Division

1126-1 Ichino-cho, Hamamatsu City, 435-8558 Japan, Telephone: (81) 053-434-3311, Fax: (81) 053-434-5184, <http://www.hamamatsu.com>

U.S.A.: Hamamatsu Corporation: 360 Foothill Road, P.O.Box 6910, Bridgewater, N.J. 08807-0910, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218

Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 08152-3750, Fax: (49) 08152-2658

France: Hamamatsu Photonics France: S.A.R.L.: 8, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10

United Kingdom: Hamamatsu Photonics UK Limited: Lough Point, 2 Gladbeck Way, Windmill Hill, Enfield, Middlesex EN2 7JA, United Kingdom, Telephone: (44) 020-8367-3560, Fax: (44) 020-8367-6384

North Europe: Hamamatsu Photonics Norden AB: Smidesvägen 12, SE-171 41 Solna, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01

Italy: Hamamatsu Photonics Italia S.R.L.: Strada della Moia, 1/E, 20020 Arese, Milano, Italy, Telephone: (39) 02-935-81-733, Fax: (39) 02-935-81-741

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