HAMAMATSU

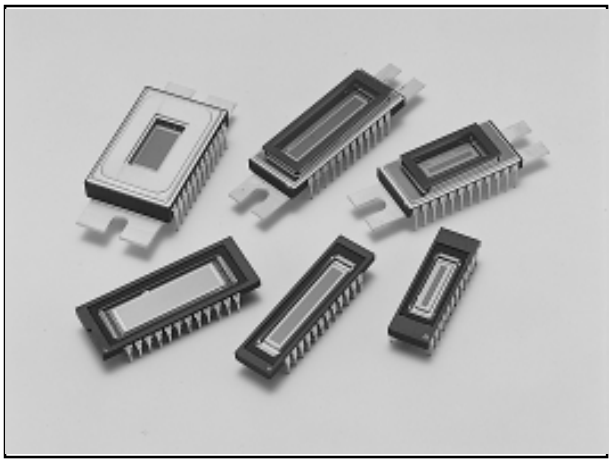
PRELIMINARY DATA Mar. 1998

CCD AREA IMAGE SENSORS S7010/S7011/S7015 SERIES

Front-illuminated FFT-CCDs

FEATURES

- 512 (H) × 60 (V) to 1024 (H) × 252 (V) pixel format
- Pixel size: 24 μm × 24 μm
- Line/pixel binning
- 100 % fill factor
- Wide dynamic range
- Low dark signal
- Low readout noise
- MPP operation



APPLICATIONS

- Fluorescence spectrometer
- Raman spectrophotometer
- Optical and spectrophotometric analyzer
- For low-light-level detection requiring

The S7010/S7011/S7015 series are families of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, the S7010/S7011/S7015 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes the S7010/S7011/S7015 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. The S7010/S7011/S7015 series also feature low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.
The S7010/S7011/S7015 series have an effective pixel size of 24 μm × 24 μm and are available in image areas ranging from 12.288 (H) × 1.44 (V) mm^2 (512 × 60 pixels) up to a large image area of 24.576 (H) × 6.048 (V) mm^2 (1024 × 252 pixels).

■SELECTION GUIDE

Type No.	Cooling	Number of Total Pixels	Number of Active Pixels	Active Area [mm (H) × mm (V)]	Suitable Multichannel Detector Head
S7010-0906	Non-cooled	532 × 64	512 × 60	12.288 × 1.44	C7020
S7010-0907		532 × 128	512 × 124	12.288 × 2.976	
S7010-0908		532 × 256	512 × 252	12.288 × 6.048	
S7010-1006		1044 × 64	1024 × 60	24.576 × 1.44	
S7010-1007		1044 × 128	1024 × 124	24.576 × 2.976	
S7010-1008		1044 × 256	1024 × 252	24.576 × 6.048	
S7011-0906	One-stage TE-cooled	532 × 64	512 × 60	12.288 × 1.44	C7021
S7011-0907		532 × 128	512 × 124	12.288 × 2.976	
S7011-1006		1044 × 64	1024 × 60	24.576 × 1.44	
S7011-1007		1044 × 128	1024 × 124	24.576 × 2.976	
S7015-0908		532 × 256	512 × 252	12.288 × 6.048	C7025
S7015-1008		1044 × 256	1024 × 252	24.576 × 6.048	

■GENERAL RATINGS

Parameter	Specification
Pixel Size	24 μm (H) × 24 μm (V)
Vertical Clock Phase	2 phase
Horizontal Clock Phase	2 phase
Output Circuit	One-stage MOSFET source follower
Package	24 pin ceramic DIP (Refer to DIMENSIONAL OUTLINES)
Window	S7010 series: quartz glass *1 S7011 series: sapphire glass S7015 series: quartz glass *2

*1: Window-less is available upon request.

*2: Sapphire glass is available upon request.

■ELECTRICAL CHARACTERISTICS (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal Output Frequency	fc	-	-	1	MHz
Charge Transfer Efficiency *3	CTE	-	0.99995	-	-
DC Output Level *4	Vout	12	15	18	V
Output Impedance *4	Zo	-	3	-	kΩ
Power Dissipation *4 *5	P	-	15	-	mW

*3: Measured at half of the full well capacity. CTE is defined per pixel.

*4: The values depend on the load resistance. (Typical, VOD=20 V, Load resistance=22 kΩ)

*5: Power dissipation of the on-chip amplifier.

■ELECTRICAL AND OPTICAL CHARACTERISTICS (Ta=25 °C if not remarked)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation Output Voltage		Vsat	-	Fw × Sv	-	V
Full Well Capacity	Vertical	Fw	-	300,000	-	e^-
	Horizontal *6		-	600,000	-	
CCD Node Sensitivity		Sv	1.8	2.2	-	μV/e^-
Dark Current *7 MPP Mode (Tentative Data)	25 °C	DS	-	1000	3000	e^-/pixel/s
	0 °C		-	50	150	
Readout Noise *8		Nr	-	8	-	e^- rms
Dynamic Range *9	Line Binnng	DR	-	75,000	-	-
	Area Scanning		-	37,500	-	-
Photo Response Non-Uniformity *10		PRNU	-	-	±10	%
Spectral Response Range		λ	-	400 to 1,100	-	nm

*6: Large horizontal full well for vertical binning operation.

*7: Dark signal doubles for every 5 to 7 °C.

*8: Operating frequency is 150 kHz, Ta= -40 °C

*9: Dynamic Range: DR = Full Well/Readout Noise

*10: Measured at the half of the full well capacity.

Photo Response Non-Uniformity:

$$\text{PRNU (\%)} = \frac{\text{Fixed Pattern Noise (peak to peak)}}{\text{Signal}} \times 100$$

Figure 1: Spectral Response

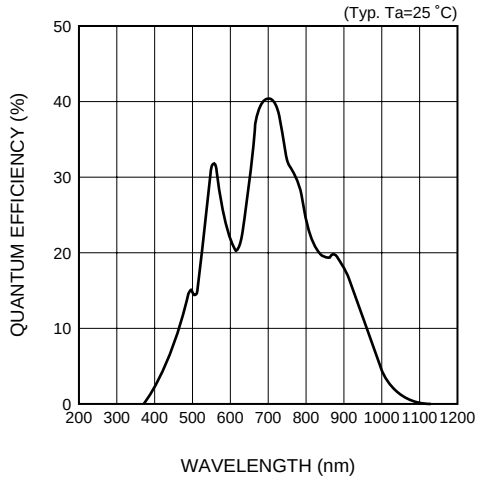


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Figure 2: Device Structure

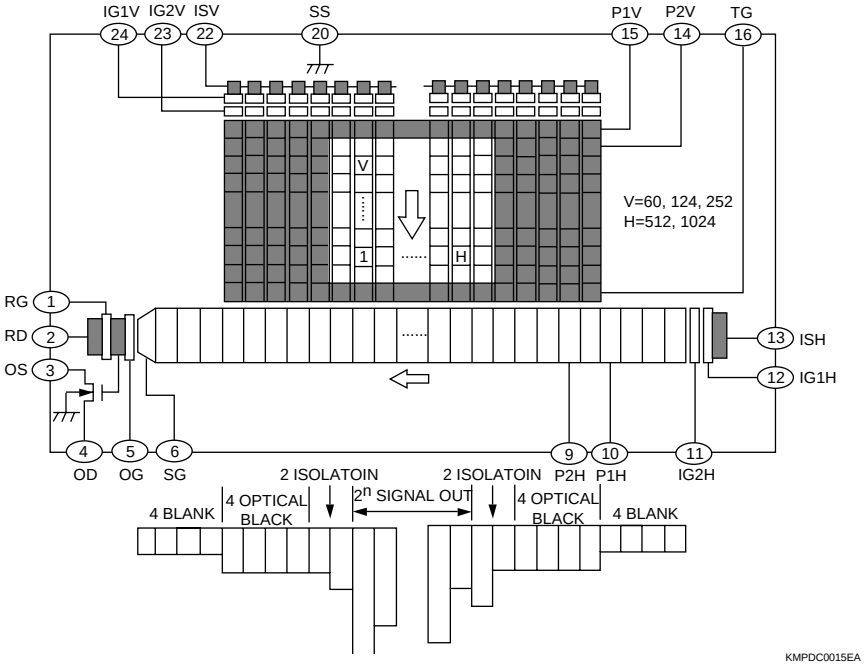


Figure 3: Timing Chart (Line Binning)

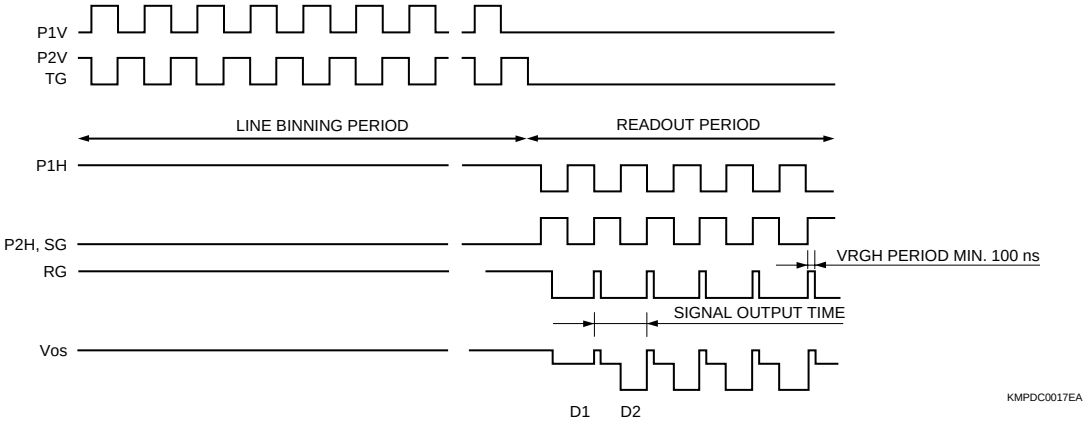


Figure 4: Timing Chart (Area Scanning)

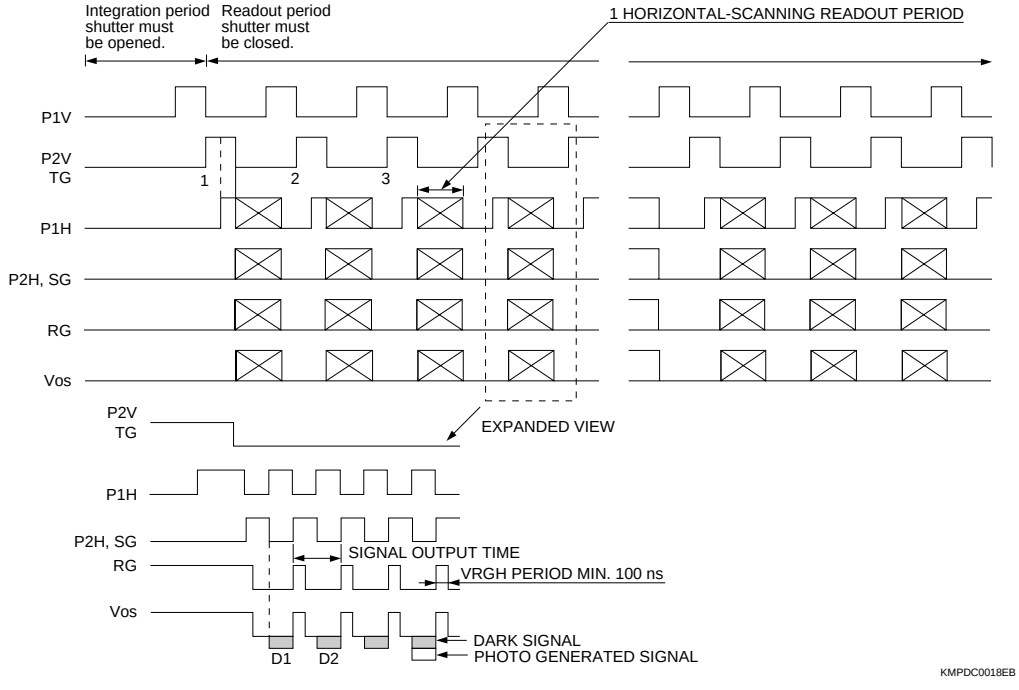
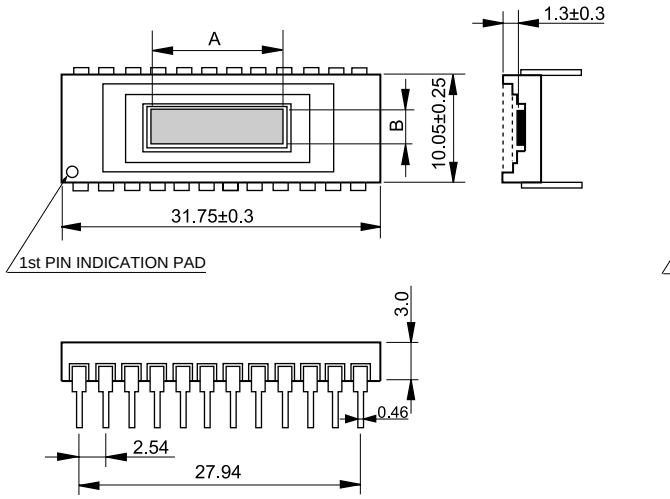
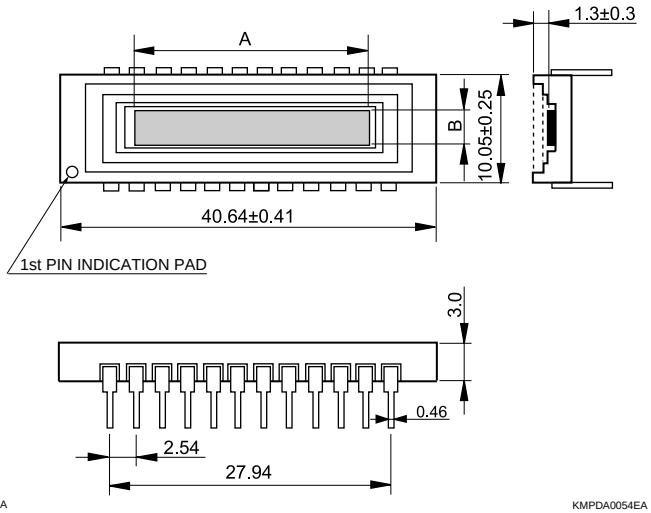


Figure 5: Dimensional Outlines (Unit: mm)

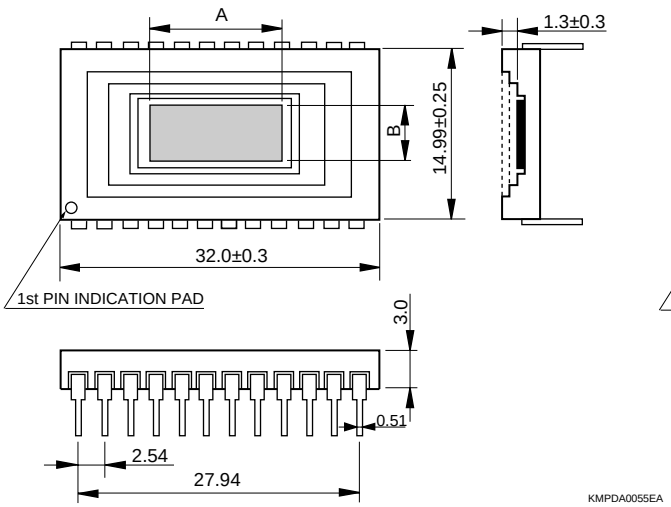
S7010-0906/-0907



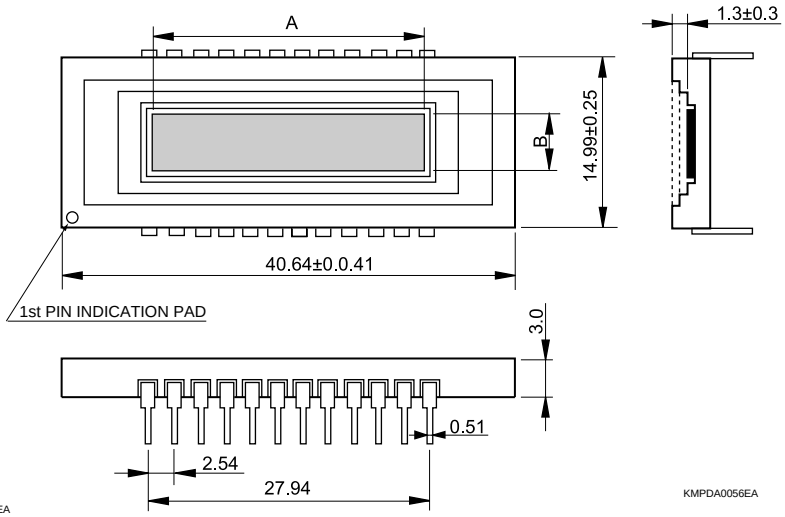
S7010-1006/-1007



S7010-0908

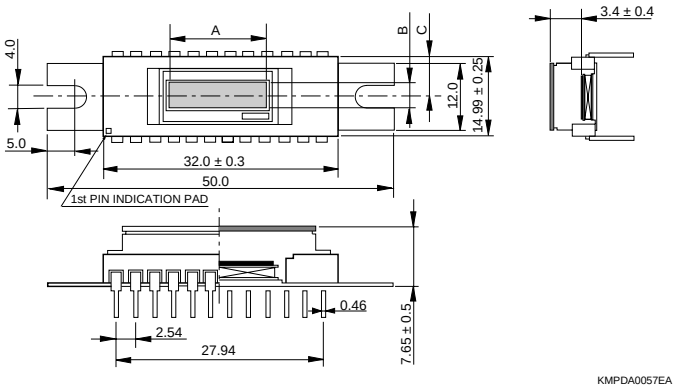


S7010-1008

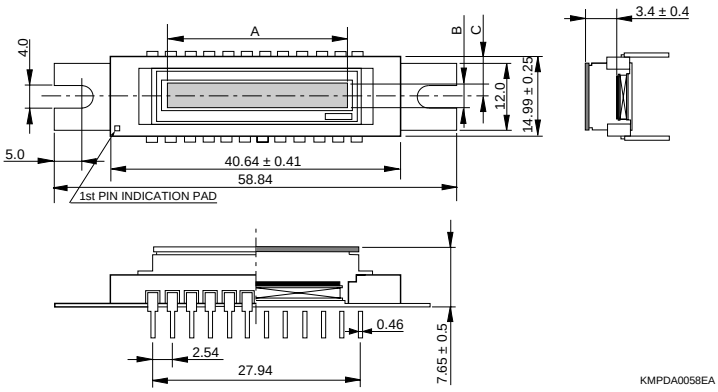


Type No.	Active Area	
	A	B
S7010-0906	12.288 (H)	1.44 (V)
S7010-0907	12.288 (H)	2.976 (V)
S7010-0908	12.288 (H)	6.048 (V)
S7010-1006	24.576 (H)	1.44 (V)
S7010-1007	24.576 (H)	2.976 (V)
S7010-1008	24.576 (H)	6.048 (V)

S7011-0906/-0907

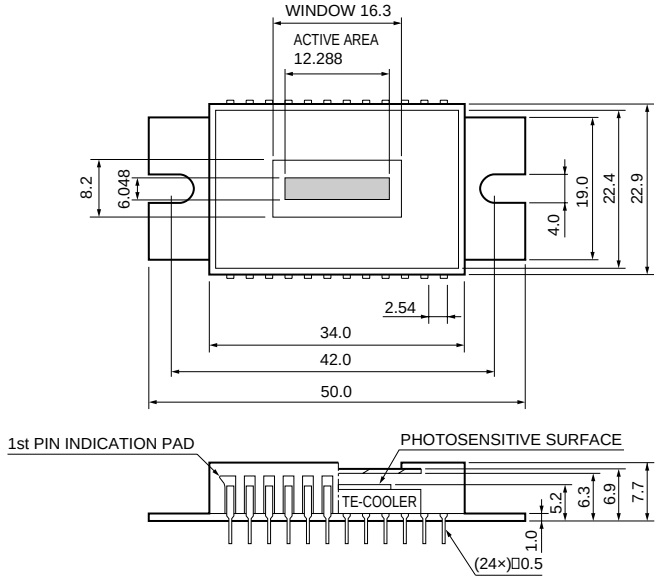


S7011-1006/-1007

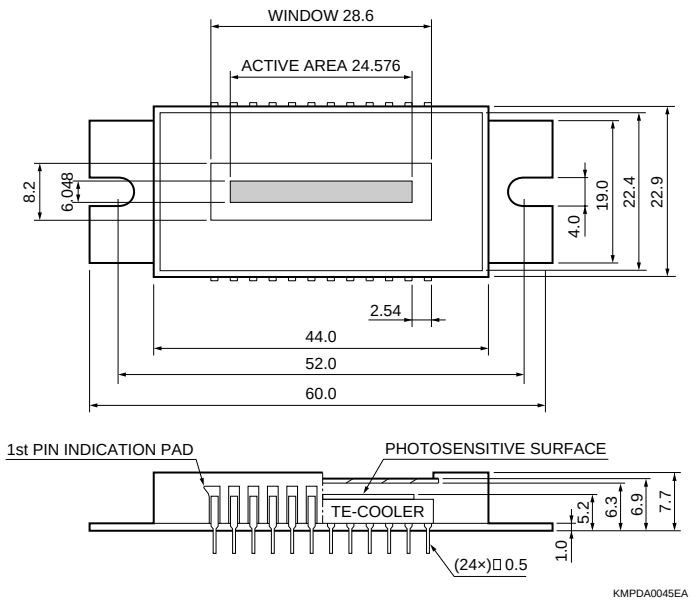


Type No.	Active Area		
	A	B	C
S7011-0906	12.288 (H)	1.44 (V)	7.5
S7011-0907	12.288 (H)	2.976 (V)	7.1
S7011-1006	24.576 (H)	1.44 (V)	7.5
S7011-1007	24.576 (H)	2.976 (V)	7.1

S7015-0908



S7015-1008



■PIN CONNECTIONS

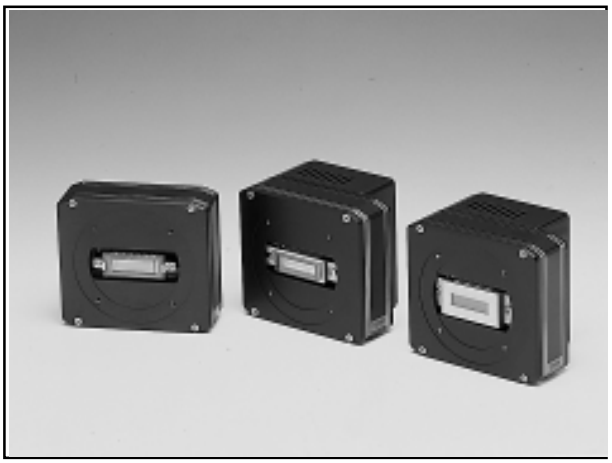
Pin No.	S7010 series		S7011 series		S7015 series		Remark
	Symbol	Description	Symbol	Description	Symbol	Description	
1	RG	Reset Gate	RG	Reset Gate	RG	Reset Gate	
2	RD	Reset Drain	RD	Reset Drain	RD	Reset Drain	
3	OS	Output Transistor Source	OS	Output Transistor Source	OS	Output Transistor Source	
4	OD	Output Transistor Drain	OD	Output Transistor Drain	OD	Output Transistor Drain	
5	OG	Output Gate	OG	Output Gate	OG	Output Gate	
6	SG	Summing Gate	SG	Summing Gate	SG	Summing Gate	=P2H
7	NC		Th1	Thermistor	Th1	Thermistor	
8	NC		Th2	Thermistor	Th2	Thermistor	
9	P2H	CCD Horizontal Register Clock-2	P2H	CCD Horizontal Register Clock-2	P2H	CCD Horizontal Register Clock-2	
10	P1H	CCD Horizontal Register Clock-1	P1H	CCD Horizontal Register Clock-1	P1H	CCD Horizontal Register Clock-1	
11	IG2H	Test Point (Horizontal Input Gate-2)	IG2H	Test Point (Horizontal Input Gate-2)	IG2H	Test Point (Horizontal Input Gate-2)	= -8 V
12	IG1H	Test Point (Horizontal Input Gate-1)	IG1H	Test Point (Horizontal Input Gate-1)	IG1H	Test Point (Horizontal Input Gate-1)	= -8 V
13	ISH	Test Point (Horizontal Input Source)	ISH	Test Point (Horizontal Input Source)	ISH	Test Point (Horizontal Input Source)	=RD
14	P2V	CCD Vertical Register Clock-2	P2V	CCD Vertical Register Clock-2	P2V	CCD Vertical Register Clock-2	
15	P1V	CCD Vertical Register Clock-1	P1V	CCD Vertical Register Clock-1	P1V	CCD Vertical Register Clock-1	
16	TG *1	Transfer Gate	TG *1	Transfer Gate	TG *11	Transfer Gate	=P2V
17	NC		NC		NC		
18	NC		P-	Peltier-	P-	Peltier-	
19	NC		P+	Peltier+	P+	Peltier+	
20	SS	Substrate (GND)	SS	Substrate (GND)	SS	Substrate (GND)	
21	NC		NC		NC		
22	ISV	Test Point (Vertical Input Source)	ISV	Test Point (Vertical Input Source)	ISV	Test Point (Vertical Input Source)	=RD
23	IG2V	Test Point (Vertical Input Gate-2)	IG2V	Test Point (Vertical Input Gate-2)	IG2V	Test Point (Vertical Input Gate-2)	=-8 V
24	IG1V	Test Point (Vertical Input Gate-1)	IG1V	Test Point (Vertical Input Gate-1)	IG1V	Test Point (Vertical Input Gate-1)	=-8 V

*11 TG: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

■MULTICHANNEL DETECTOR HEADS (C7020, C7021, C7025)

FEATURES

- C7020: for S7010 series
  C7021: for S7011-0906/0907/1006/1007
  C7025: for S7015-0908/1008
- Area scanning or full line-binnng operation
- Readout frequency: 250 kHz
- Readout noise: 20 e^-rms
- Radiation method is optional.
  (Finn and fan for air-cooling, water-cooling)
- ΔT=50 °C (ΔT changes by radiation method.)



Input	Symbol	Value
Supply Voltage	$+V_{DI}$	+5 Vdc, 200 mA
	$\pm V_{A1}$	±15 Vdc, ±100 mA
	$+V_{A2}$	+24 Vdc, 10 mA
	$+V_{D2}$	+5 Vdc, 10 mA (C7021, C7025)
	+Vp	+5 Vdc, 3 A (C7021, C7025)
	$+V_F$	+12 Vdc, 200 mA (C7021, C7025)
Master Start	ϕms	HCMOS logic compatible
Master Clock	ϕmc	HCMOS logic compatible, 1MHz

HAMAMATSU

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