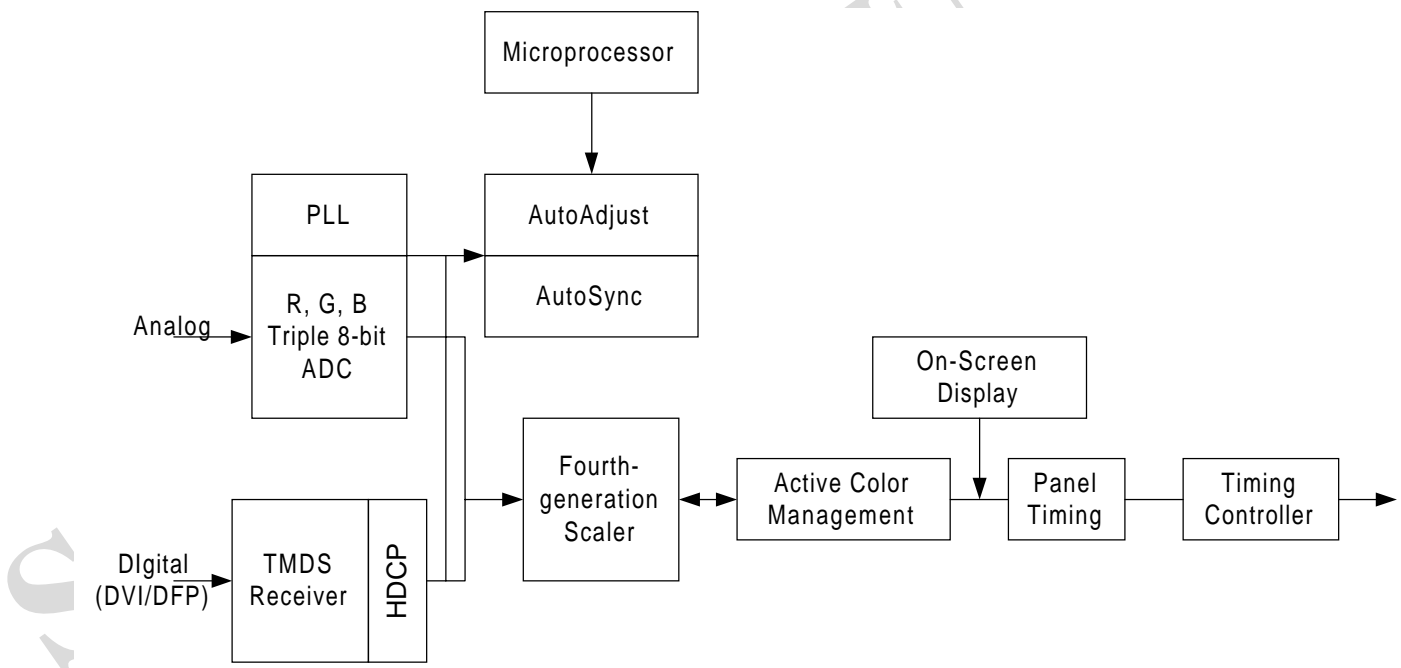# s9330 Display Processor

ssage

Industry's First Dual-interface Display Processor with Integrated Timing Controller and Microprocessor s9330

The s9330-135 and the s9330-100 are both highly-integrated dual-interface display processors. Both have an ADC/PLL block, a TMDS receiver block and a microprocessor integrated on a single chip. The cost-effective s9350-100 is suitable for the XGA and the s9330 for the SXGA market segment with smaller memory requirements. Other features include a brand new high-end scaler, Active Color Management, a flexible OSD, Autoadjust, SureSync™ and independent monitoring of the analog and digital interfaces. A new standalone on-chip pattern generator has been incorporated to simplify the manufacture of monitors.

Features

High-performance ADC and PLL
- Single channel RGB
- 140MHz capture PLL
- Supports Sync-On-Green
  - Sync slicer
  - Capture PLL coasting

TMDS Receiver
- 140MHz operating speed
  - Digital Video Content Protection (HDCP)
  - Supports DE-only mode

Embedded 188 microprocessor
- 8Kbytes data memory
- Address/Data de-multiplex option
- Optional external microprocessor
- Supported speeds up to 80MHz.
- Programmable clock speed for power management.

Integrated PLLs synthesizers for
- Panel Clock
- Micro Clock

Pattern Generation
- Generates horizontal bars, vertical bars and checker patterns
- Color and monochrome supported
- No external input required

Auto Sync
- Dual tandem SureSync™ channels for independent monitoring of ADC and TMDS inputs
- Minimal firmware interaction needed
- Quick and smart synchronization

Autoadjust/AutoColor (For analog input port)
- Detects position, phase and H-size and sets automatically
- Performed in less than two seconds

Scaler
- Advanced third-generation scaler
- Three-tap, 32-phase filters
- Independent expansion/reduction in both horizontal and vertical directions
- Horizontal flipping of images

Active Color Management

Built-in Brightness/contrast Control

Color Look-Up Table
- 8-to-10 look-up
- Static gamma correction
- Auxiliary brightness/contrast control

On-Screen Display
- Supports multi-color fonts
- Translucent OSD supported
- Bitmapped or alphanumeric OSD
- 4Kbytes of embedded OSD Memory

Dithering
- 10-to-8/6 dithering
- Spatial/Temporal (random/sequential)

Flexible Panel Interface
- 1 pixel/2 pixel per shift clock.
- Using both the edges of the shift clock
- 8-bit or 6-bit panels
- Panel datasteering for various panel connectors

Panel Data Transition Minimization
- Number of transitions on panel data is reduced by at least 50%
- No switching on the data lines for a pin-stripe pattern
- Dual-pixel panel minimization is supported on
  - A full two-pixel bus
  - Separately for odd and even buses
- Option to freeze the last active pixel in each line for the succeeding inactive region.

Spread Spectrum
- Supports External Spread Spectrum ICs

Two-Wire Serial Slave and Master available
Support for external I/O expansion
- Uses standard timings
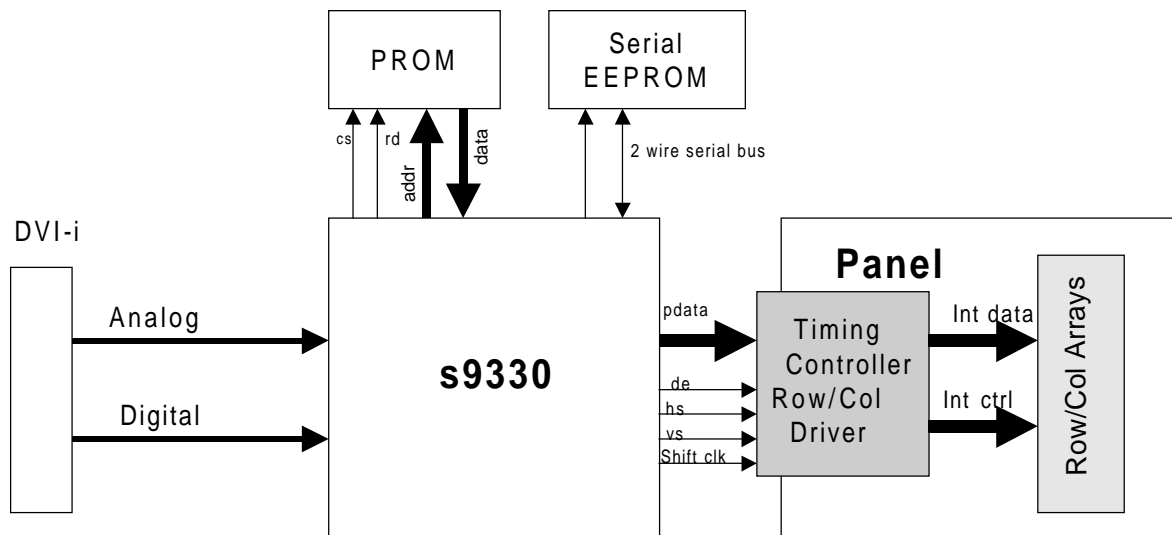- Microcontroller-based

Package
- 208 PQFP

Operating Conditions
- 2.5 volts core
- 3.3 volts I/O

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System Level Interface Diagram Regular Panel Interface

PROM

Serial
EEPROM

cs   rd

addr   data

2 wire serial bus

DVI-i

Analog

Digital

s9330

pdata

de

hs

vs

Shift clk

Panel

Timing
Controller
Row/Col
Driver

Int data

Int ctrl

Row/Col Arrays

Display Modes

Input		Panel Resolution			
Resolution	Refresh	SVGA	XGA	WXGA	SXGA
DOS640	Up to 75Hz	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135
DOS720	Up to 75Hz	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135
VGA	Up to 75Hz	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135
SVGA	Up to 75Hz	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135
XGA	Up to 75Hz	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135
WXGA	Up to 75Hz	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135/s9350-100	s9330-135
SXGA	Up to 75Hz	s9330-135	s9330-135	s9330-135	s9330-135

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