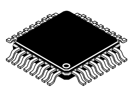
Customer Specific Semiconductor

SC931

Low Voltage PLL Clock Driver

The SC931 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock applications. With output frequencies of up to 140MHz and output skews of 300ps the SC931 is ideal for the most demanding clock distribution designs. The device employs a fully differential PLL design to minimize cycle to cycle and long term jitter. This parameter is of significant importance when the clock driver is providing the reference clock for PLL's on board todays microprocessors and ASiC's. The device offers 6 low skew outputs, and a choice between internal or external feedback. The feedback option adds to the flexibility of the device, providing numerous input to output frequency relationships.



FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

- Differential LVPECL Reference Input
- Fully Integrated PLL
- Output Shut Down Mode
- Output Frequency up to 140MHz
- Compatible with PowerPC™ and Intel Microprocessors
- 32–Lead TQFP Packaging
- Power Down Mode
- ±100ps Typical Cycle–to–Cycle Jitter

The SC931 offers two power saving features for power conscious portable or "green" designs. The power down pin will seemlessly reduce all of the clock rates by one half so that the system will run at half the potential clock rate to extend battery life. The POWER_DN pin is synchronized internally to the slowest output clock rate. This allows the transition in and out of the power–down mode to be output glitch free. In addition, the shut down control pins will turn off various combinations of clock outputs while leaving a subset active to allow for total processor shut down while maintaining system monitors to "wake up" the system when signaled. During shut down, the PLL will remain locked, if internal feedback is used, so that wake up time will be minimized. The shut down and power down pins can be combined for the ultimate in power savings. The Shut_Dn pins are synchronized to the clock internal to the chip to eliminate the possibility of generating runt pulses.

An internal feedback divide by 8 of the VCO frequency is compared with the input reference provided. The internal VCO is running at 8x the input reference clock. The outputs can be configured to run at 4x, 2x, 1.25x or 0.66x the input reference frequency. If the external feedback is selected, one of the SC931's outputs must be connected to the Ext_FB pin. Using the external feedback, numerous input/output frequency relationships can be developed.

The SC931 is fully 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive terminated 50Ω transmission lines. For series terminated applications, each output can drive two 50Ω transmission lines, effectively increasing the fanout to 1:12. The device is packaged in a 32–lead TQFP package to provide the optimum combination of board density and cost.

PowerPC is a trademark of International Business Machines Corporation. Pentium is a trademark of Intel Corporation.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

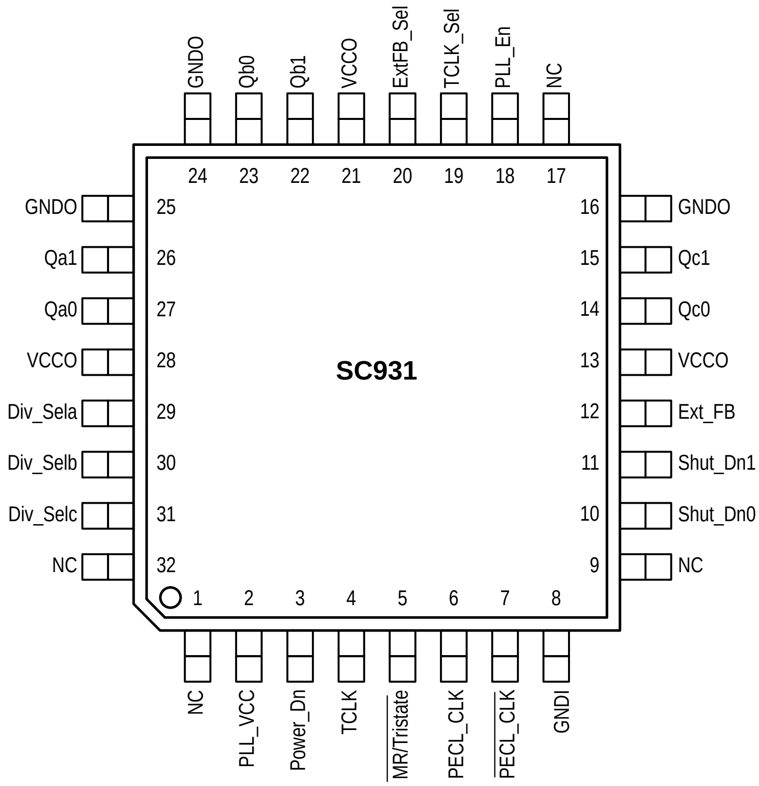


Figure 1. 32–Lead Pinout (Top View)

FUNCTION TABLES

TCLK_Sel	Reference
0	PECL_CLK
1	TCLK

PLL_En	PLL Status
0	Test Mode
1	PLL Enabled

ExtFB_Sel	Reference
0	Int. ÷8
1	Ext_FB

Power_Dn	PLL Status
0	VCO/1
1	VCO/2

Div_Sela,b,c	Qa	Qb	Qc
0	÷2	÷2	÷4
1	÷4	÷4	÷6

MR/Tristate	PLL Status
0	Disabled
1	Enabled

Shut_Dn1	Shut_Dn0	Div_Seln
0	0	Qb & Qc Low, Qa Toggle
0	1	Qa & Qb Low, Qc Toggle
1	0	Qb Low, Qa & Qc Toggle
1	1	All Toggle

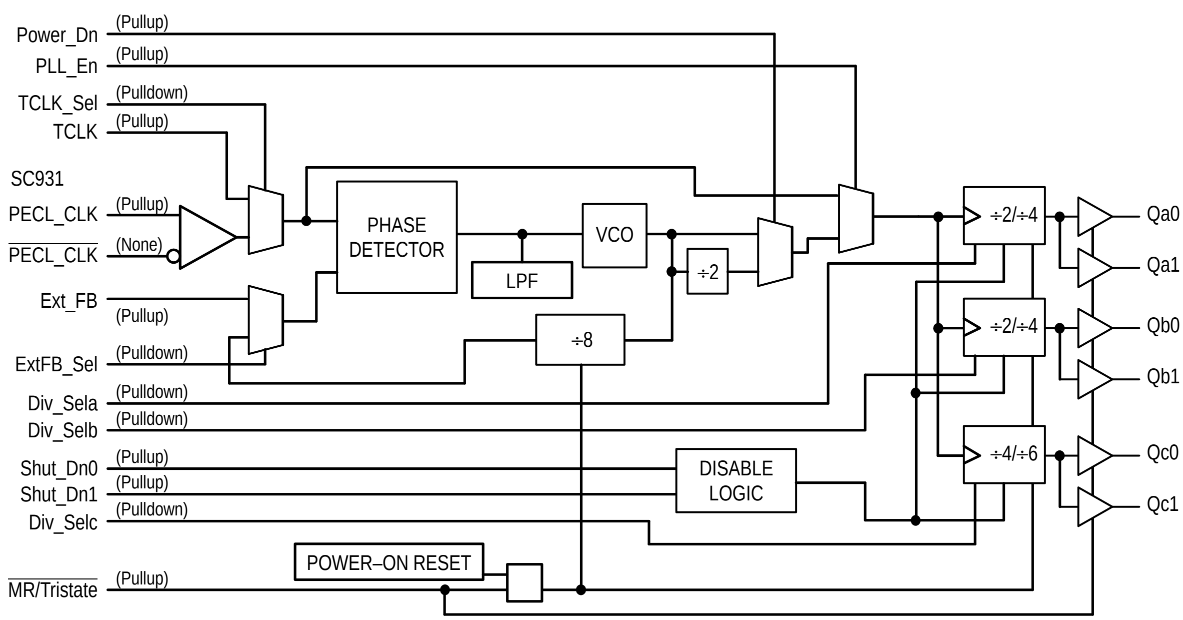


Figure 2. Logic Diagram

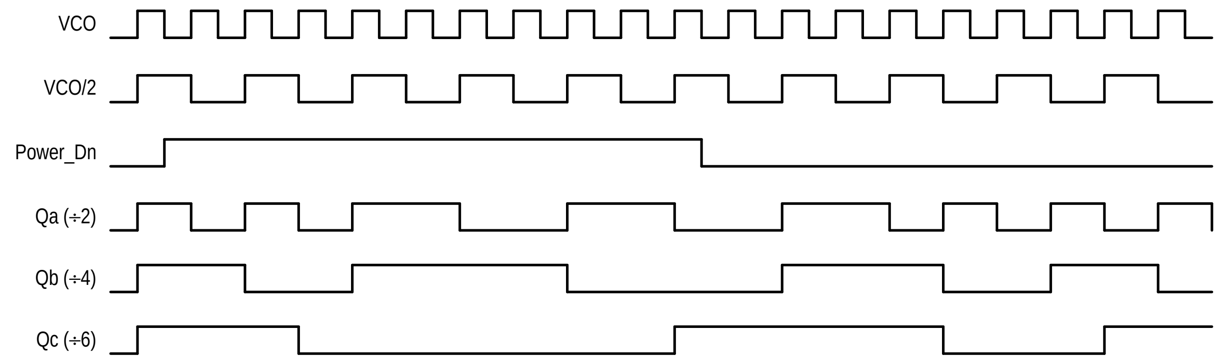


Figure 3. Power_Dn Timing Diagram

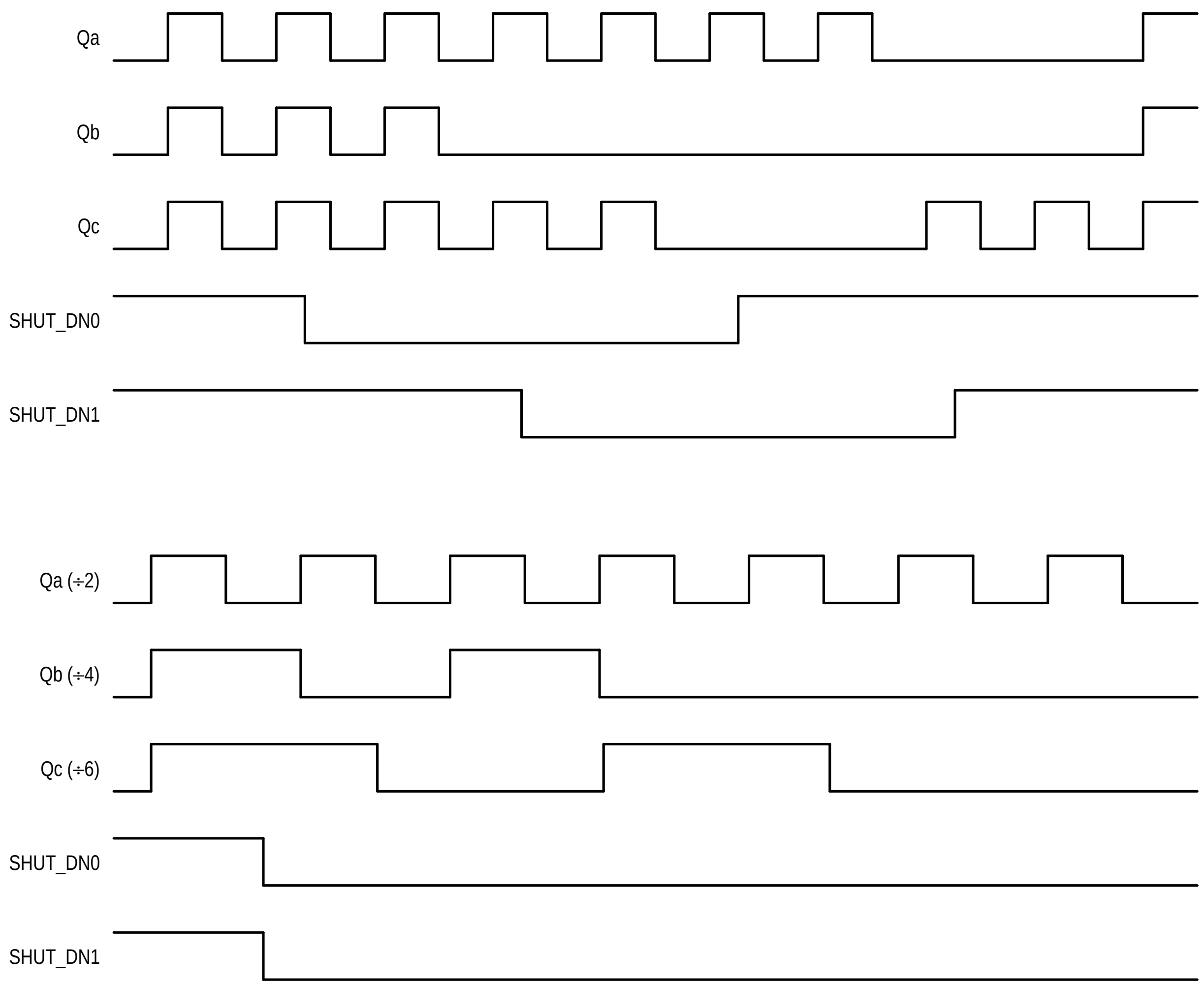


Figure 4. Shut_Dn Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	10	Note 1.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1. Maximum input reference frequency is limited by the VCO lock range and the feedback divider.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA (Note 2.)
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA (Note 2.)
I_{IN}	Input Current			±120	µA	Note 3.
I_{CC}	Maximum Core Supply Current		65	85	mA	
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	
C_{IN}				4	pF	
C_{pd}			25		pF	Per Output

2. The SC931 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up/pull–down resistors which affect input current.

SC931 AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{xtal}	Crystal Oscillator Frequency Range	10		20	MHz	Note NO TAG, Note 6.
f_{ref}	Input Reference Frequency	Note 6.		Note 6.	MHz	Ref = TCLK
t_{os}	Output–to–Output Skew (Note 4.) Same Frequency Diff Frequency Same Frequency Diff Frequency		200 300 300 450	300 400 400 600	ps	f_{max} ≤ 100MHz f_{max} ≤ 100MHz f_{max} > 100MHz f_{max} > 100MHz
f_{VCO}	VCO Lock Range Power_Dn = 0	100		280	MHz	
f_{max}	Maximum Output Frequency Qa, Qb (÷2) Qa, Qb, Qc (÷4) Qc (÷6)			140 80 47	MHz	Note 4.
t_{pd}	TCLK to EXT_FB Delay	–600	–100	400	ps	f_{ref} = 50MHz, FB = ÷4
t_{pw}	Output Duty Cycle (Note 4.)	t_{CYCLE}/2 –750	t_{CYCLE}/2 ±500	t_{CYCLE}/2 +750	ps	
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.1		1.0	ns	0.8 to 2.0V
t_{PLZ}, t_{PHZ}	Output Disable Time	2.0		8.0	ns	50Ω to V_{CC}/2
t_{PZL}	Output Enable Time	2.0		10	ns	50Ω to V_{CC}/2
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±100		ps	Note 5.
t_{lock}	Maximum PLL Lock Time			10	ms	

4. Measured with 50Ω to V_{CC}/2 termination.
5. See Applications Info section for more jitter information.
6. Input reference frequency is bounded by VCO lock range and feedback divide selection.

APPLICATIONS INFORMATION

Programming the SC931

The SC931 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option allows for a great deal of flexibility in establishing unique input to output frequency relationships. The output dividers for the three output groups allows the user to configure the outputs into 1:1, 2:1, 3:1, 3:2 and 3:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 3:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's at VCO/4 and the Qc's at VCO/6. These settings will provide output frequencies with a 3:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The VCO lock range can be found in the specification tables. The feedback frequency and the Power_Dn pin can be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 25 and 140MHz the SC931 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. Table 2 shows the multiplication factors between the inputs and outputs when the internal feedback option is used. For external feedback Table 1 can be used to determine the multiplication factor, there are too many potential combinations to tabularize the external feedback condition. Figure 5 and Figure 6 illustrate some programming possibilities, although not exhaustive it is representative of the potential applications.

Table 1. Programmable Output Frequency Relationships (Power_Dn = '0')

INPUTS			OUTPUTS		
Div_Sela	Div_Selb	Div_Selc	Qa	Qb	Qc
0	0	0	VCO/2	VCO/2	VCO/4
0	0	1	VCO/2	VCO/2	VCO/6
0	1	0	VCO/2	VCO/4	VCO/4
0	1	1	VCO/2	VCO/4	VCO/6
1	0	0	VCO/4	VCO/2	VCO/4
1	0	1	VCO/4	VCO/2	VCO/6
1	1	0	VCO/4	VCO/4	VCO/4
1	1	1	VCO/4	VCO/4	VCO/6

Table 2. Input Reference/Output Frequency Relationships (Internal Feedback Only)

INPUTS			OUTPUTS					
			Qa		Qb		Qc	
Div_Sela	Div_Selb	Div_Selc	Power_Dn=0	Power_Dn=1	Power_Dn=0	Power_Dn=1	Power_Dn=0	Power_Dn=1
0	0	0	4x	2x	4x	2x	2x	x
0	0	1	4x	2x	4x	2x	4/3x	2/3x
0	1	0	4x	2x	2x	x	2x	x
0	1	1	4x	2x	2x	x	4/3x	2/3x
1	0	0	2x	x	4x	2x	2x	x
1	0	1	2x	x	4x	2x	4/3x	2/3x
1	1	0	2x	x	2x	x	2x	x
1	1	1	2x	x	2x	x	4/3x	2/3x

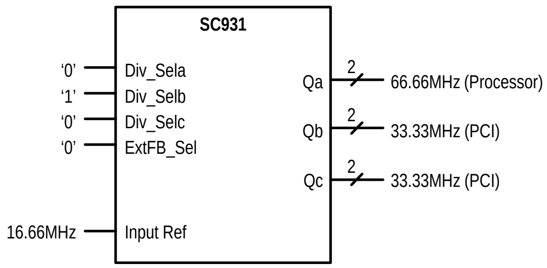


Figure 5. Dual Frequency Configuration

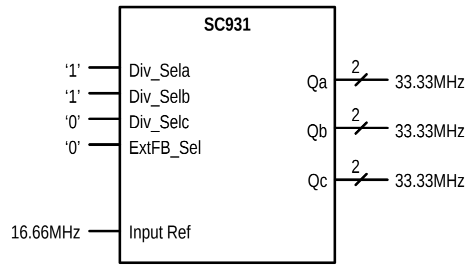
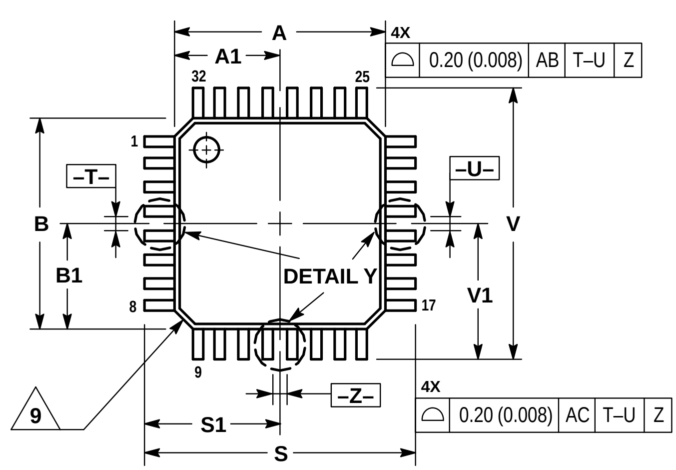
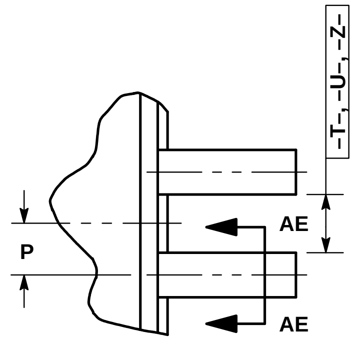


Figure 6. Single Frequency Configuration

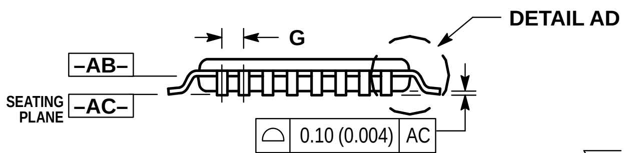
OUTLINE DIMENSIONS

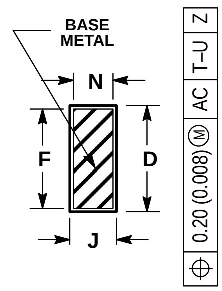
FA SUFFIX
TQFP PACKAGE
CASE 873A–02
ISSUE A



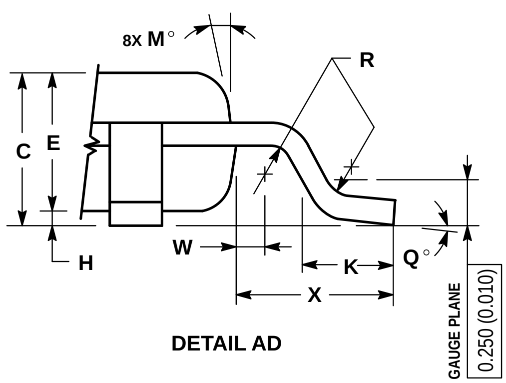


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

Customer Focus Center: 1–800–521–6274

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1–602–244–6609
Motorola Fax Back System – US & Canada ONLY 1–800–774–1848
– http://sps.motorola.com/mfax/

HOME PAGE: http://motorola.com/sps/

JAPAN: Nippon Motorola Ltd.; SPD, Strategic Planning Office, 141,
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan. 81–3–5487–8488

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298