BiCMOS CLOCK SYNTHESIZER S4503

FEATURES

- Multiplies input reference frequency by integers 2–32
- Digitally programmable output clock frequencies from 10 MHz to 300 MHz
- Two (2) groups of independent clock outputs
  - One group consists of differential PECL outputs
  - One group is a pair of TTL outputs
- Proprietary TTL output drivers with:
  - Complementary 24 mA peak outputs, source and sink
  - Source series termination
  - Edge rates less than 1.5 ns
- Low 250 ps reference typ clock jitter (PECL outputs), 400 ps max
- 1.1 mW or less power dissipation, frequency and load dependent
- 150 MHz to 300 MHz phase-locked loop VCO frequency range
- Advanced BiCMOS process technology
- Space saving 28 PLCC package

GENERAL DESCRIPTION

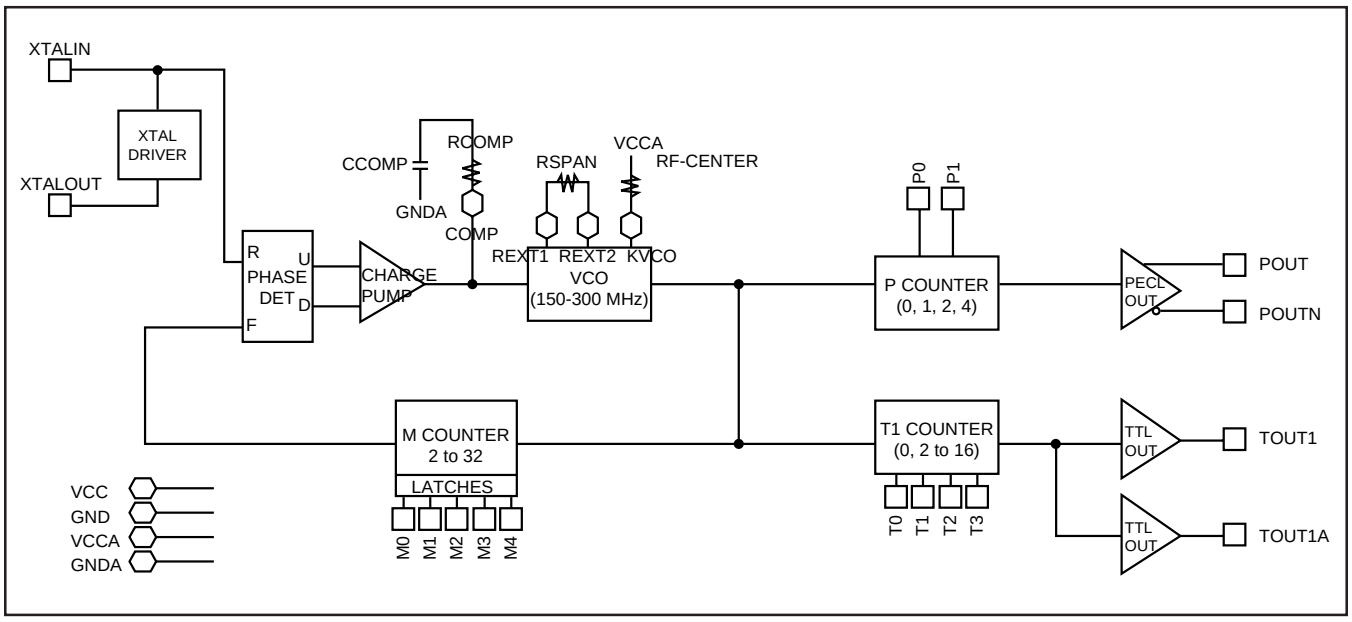
The S4503 is a clock synthesizer which utilizes phase-locked loop technology to provide two (2) independently selectable output frequencies in the 10 MHz to 300 MHz range. A reference input may be provided by either a low cost crystal or a TTL frequency source.

The first of the two (2) output frequency groups consists of a pair of differential PECL (Positive referenced ECL) outputs which will operate up to 300 MHz. The second group (TTL) consist of two outputs with selectable frequency, up to 80 MHz.

The final frequency for each group is digitally selected via three programmable counters. One counter is used to set the internal VCO frequency between 150 MHz to 300 MHz, and the others are used to divide the VCO frequency from 2 thru 16 (TTL) and 1, 2 or 4 (PECL).

All phase-locked loop elements are provided on chip with the exception of the passive components needed for the loop filter function and VCO.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55°C to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +130°C
Latch-up Current ..... >200 mA
Operating ambient temperature ..... 0°C to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF
PECL Output Pins ..... 5.0 pF

AC Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C

Symbol	Description	Conditions	MIN	MAX	Units
F_{VCO}	VCO Frequency		150	300	MHz
F_{XTL}	XTL Frequency, Fundamental	XTLIN to XTLOUT	5	25	MHz
F_{TTL}	TTL Input Frequency	Standard TTL Levels	5	80	MHz
P_{out}	PECL Out Frequency		37	300	MHz
T_{OUTn}	TTL Out Frequency	See Note 4	9	80	MHz
$T_{SKEW\ T\text{-}T}$	TTL to TTL Output Skew	TTL Leading Edges at +1.5V		250	ps
$T_{SYM\text{-}T}$	T_{OUT} Symmetry	Measured at 1.5V		±1.5	ns
$T_{SYM\text{-}P}$	PECL Out Symmetry	Measured at differential crossing points		±250	ps
T_J	PECL Clock Jitter, pk to pk			400	ps

Notes:
1. Max cycle to cycle jitter.
2. Output symmetry is the deviation from a 50% duty cycle.
3. All AC parameters are tested or guaranteed by characterization.
4. VCO frequency is limited to a maximum of 250 MHz when TTL outputs are used.

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Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}(PECL)	Output HIGH Voltage, ECL	50 Ohms to V_{CC}-2V	V_{CC}-1075	V_{CC}-650	mV
V_{OL} (PECL)	Output LOW Voltage, ECL	50 Ohms to V_{CC}-2V	V_{CC}-1980	V_{CC}-1585	mV
V_{OH}(TTL)	Output HIGH Voltage	F_{OUT} = 80 MHz max, C_L = 10pF	2.4		V
V_{OL} (TTL)	Output LOW Voltage, TTL	F_{OUT} = 80 MHz max, C_L = 10pF		0.6	V
V_{IH} (TTL)	Input (TTL) HIGH Voltage	All TTL Inputs	2.0	V	V
I_{IL} (TTL)	Input (TTL) LOW Voltage	All TTL Inputs	-0.5	0.8	V
I_{OH}(PECL)	Output HIGH Current	50 Ohms to V_{CC}-2.0		25	mA
I_{OL}(PECL)	Output LOW Current	50 Ohms to V_{CC}-2.0		8	mA
I_{IH} (TTL)	Input HIGH Current	V_{in} = V_{CC}		200	uA
I_{IL} (TTL)	Input LOW Current	V_{in} ≤ 0.8		50	uA
I_{OHS}[1]	Output HIGH Short Current	Output High, V_{OUT}=0V, Typical	-55		mA
I_{OLS}[1]	Output LOW Peak Current	Output Low, V_{OUT}= V_{CC} , Typical	55		mA
I_{CC}	Supply Current	TTL Outputs to 20 pF @ 50 MHz		210	mA
POWER	Power Dissipation	TTL Outputs to 20 pF @ 50 MHz		1.1	W

1. Maximum test duration one second.
2. All DC parameters are tested or guaranteed by characterization.

The S4503 TTL outputs feature source series termination of approximately 40 Ohms to assist in matching 50–75 ohm P.C. board environments.

DC Characteristics

The S4503 has been designed specifically for clock distribution. In the development of this product, AMCC has made several modifications to the historic “high drive, totem pole outputs” producing AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the S4503 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8 mA	2.4V	
V_{OL}	I_{OL} = 4 mA		0.6V

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

The S4503 synthesizer employs a phase locked loop (PLL) which includes a "multiplying" counter to produce a high frequency internal reference oscillator from a low cost, low frequency crystal. This high frequency internal reference is the output of a votage controlled oscillator or VCO. This single VCO frequency is sub divided down to selectable TTL output frequencies. One positive (+5V) referenced complementary ECL (PECL) output (Pout) pair is also provided.

The M counter is a frequency "multiplying" feedback counter that divides down the VCO frequency, before applying it to the phase detector. Thus the VCO frequency is the product of the input reference (crystal) frequency and the M counter modulus. This divide down counter modulus is externally selected to any integer value from 2 to 32 by a five bit binary coded value, plus 1, entered into input latches via the preset input pins M0 through M4. The M0 to M4 inputs have the binary weight of $M0=2^0$ through $M4=2^4$. The M0-4 inputs are low or 0 if not connected. NOTE: an entry of all binary zeros will not count down and is, therefore, invalid. Designs that will load the M counter inputs from an external register that powers-up with the outputs in a hi-Z state will need to use external resistors to ensure the S4503 M counter inputs are never all zeros.

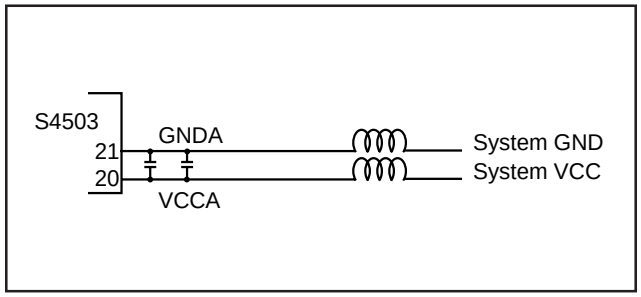
The output frequency divide down counters "P & T" each have individual select input pins which may be actively driven by CMOS/TTL outputs or strapped to +Vcc (as a 1) or non-connected as appropriate. Non-connected inputs are biased low or 0. When the binary coded value of zero is entered into these counter preselect inputs, their outputs are disabled, thereby saving AC output power. Note that the input frequency to the T counter (VCO frequency) is limited to 250 MHz. P counter will operate up to 300 Mhz. Output symmetry is very close to 50% duty cycle with both odd and even division modulus due to an odd division correction employed at the counter's output. Refer to the counter preset tables for the binary coded preselect input values to division modulus.

The TTL output drivers of the T counter are source series terminated by internal resistors of ~40 Ohms to avoid the need for external termination. This series termination was choosen to match 50 to 75 Ohm transmission line traces into end of line load capacitance of ~20 pF. Refer also to the AMCC Clock Driver Application Note #1. The complementary PECL output emitter followers can source 25 mA from +Vcc and should be externally terminated at the end of the transmission line into an equivalent 50 Ohm resistance to +Vcc - 2V.

The analog VCO circuitry requires some external passive loop filter components mounted very close to the required S4503 package pins. A VCO frequency centering resistor, RFcenter, is connected between KVCO and +VCCA, the analog +5V. A frequency span resistor, Rspan, is connected between pins REXT1 and REXT2. A loop filter series resistor-capacitor pair, RCOMP & CCOMP is connected between pin Comp and analog ground GNDA. Note that the analog ground (GNDA) and +5V (+VCCA) are to be isolated (decoupled) from the noisier digital and output power leads VCC and GND.

The input to the XTALIN pin will be a series resonant crystal of fundamental frequency from 5 to 25 Mhz. The external addition of series or shunt capacitance to "pull" the frequency is up to the user's discretion. An external series resistor may be required to limit the drive current from the XTALOUT pin with low ESR crystals.

When the XTALIN pin is driven by an external TTL clock source, the XTALOUT pin is not connected and the peak TTL amplitude should not exceed 3 volts. TTL output signals should be in the range of 5-80 MHz.



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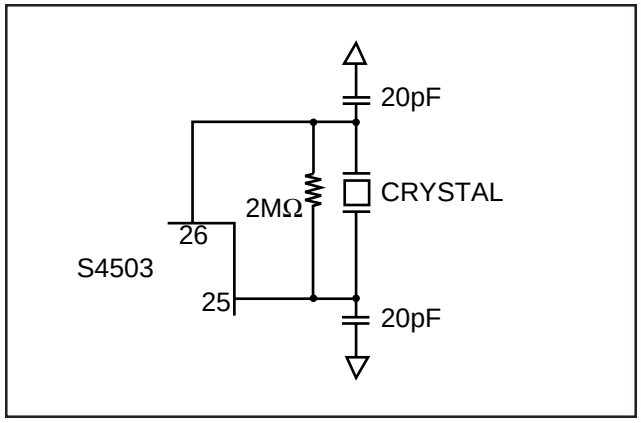
BOARD LAYOUT CONSIDERATIONS

To minimize the impact of board noise on the operation of the S4503, the following guidelines should be followed.

- The analog VCCA and GNDA need to be isolated from the digital supplies. This can be accomplished by creating small analog power and ground planes next to the S4503 under the filter and VCO components. These analog planes can be connected to the digital planes through wire jumpers, small inductors (5-100 uH), or ferrite beads. If the digital supply noise is too large (>100mV), the inductors or ferrite beads will be necessary.
- Decoupling capacitors of 0.1 and 0.01 uF are needed. Three pairs should be placed as close to the S4503 power and ground pins as possible. One pair should be used to decouple the analog VCC and GND, while the others are for the digital supplies. The Vtt supply will also need to be decoupled using 0.1 and 0.01 uF capacitors. These components should be surface mounted chip capacitors, to reduce the parasitic inductance.
- No dynamic signal lines should pass through or beneath the filter circuitry area, to avoid the possibility of noise due to crosstalk.
- The crystal oscillator will need to have a 2 M ohm shunt resistor connected between the terminals of the external crystal, and two 20 pF capacitors connected from each pin of the crystal to VCC (or GND). These components are necessary to ensure the oscillator will operate at the correct frequency.
- The loop filter and VCO components must be surface mounted to reduce the parasitic inductance, and the components are connected to the analog power and ground planes, rather than the digital planes.



FILTER AND VCO COMPONENT SELECTION

The S4503 is designed to operate over a wide range of VCO frequencies. Because of this, it is necessary to modify the values of Rspan and Rfcenter in order to get the best performance at a given frequency.

When operating the S4503 with the VCO in the 150–225 MHz region, the values for the VCO components are:

Rspan = 470 Ohms, Rfcenter = 390 Ohms

When operation the S4503 with the VCO in to 225–300 Mhz, the values for the VCO components are:

Rspan = 390 Ohms, Rfcenter = 820 Ohms

The loop filter components, Rcomp and Ccomp, do not change values at different frequencies. The correct values for these components are:

Rcomp = 2.7K Ohms, Ccomp = 0.1uF

All of the resistor values are 5% and 1/8 watt.

Power Management

The overall goal of managing the power dissipated by the S4503 is to limit its junction (die) temperature to 130°C. A major component of the power dissipated internally by the S4503 is determined by the load that each TTL output drives and the frequency that each output is running. The following table summarizes these dependencies.

FREQUENCY	C_{LOAD} =5pF	C_{LOAD} =10pF	C_{LOAD} =15pF	C_{LOAD} =25pF	C_{LOAD} =40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	65 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	60 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (700 mW) of the S4503 to determine the total power being dissipated by the S4503. This total power is then multiplied by the S4503's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the S4503. For greatest reliability this junction temperature should not exceed 130°C. The thermal resistance for the S4503 soldered to a multi-layer PCB is as follows:

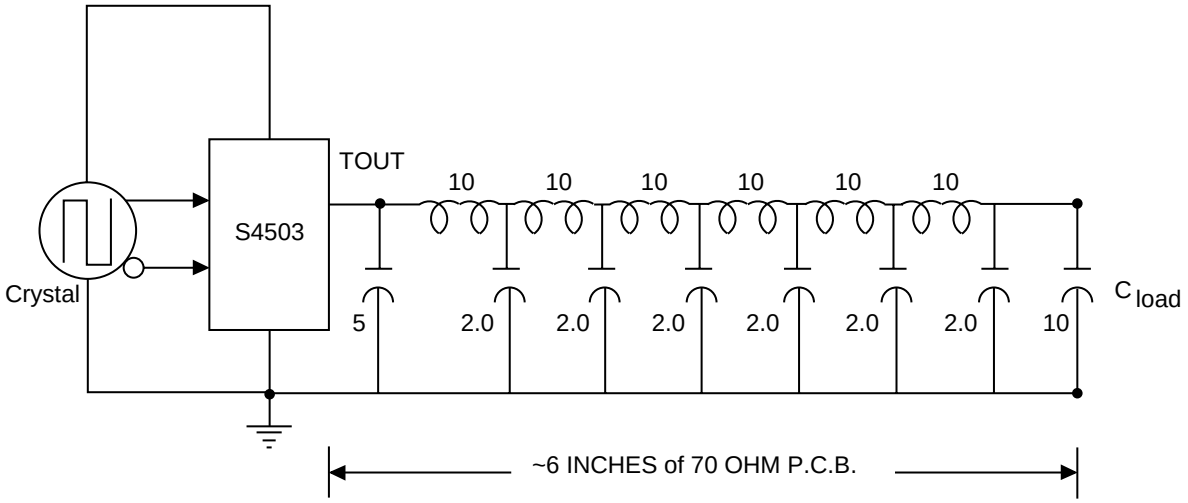
	Still Air	100 Lin Ft/Min	200 Lin Ft/Min
Thermal Resistance	50˚C/Watt	45˚C/Watt	40˚C/Watt

Designing the S4503 for "Real Loads"

The S4503 is designed to provide clean clock transitions when presented with a realistic load. The assumptions are that the S4503 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading can cause overall impedance to drop to under 60 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with capacitive loads ranging up to 20 pF at frequencies up to 80 MHz. Higher capacitive loads (greater than 25 pF) at high frequencies (greater than 50 MHz) may require the like output drivers to be strapped in parallel.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented on the following page. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in the Application Note.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point destination is recommended

S4503 M- Counter Division Table

M0	M1	M2	M3	M4	MODULUS
0	0	0	0	0	INVALID
1	0	0	0	0	2
0	1	0	0	0	3
1	1	0	0	0	4
0	0	1	0	0	5
1	0	1	0	0	6
0	1	1	0	0	7
1	1	1	0	0	8
0	0	0	1	0	9
1	0	0	1	0	10
0	1	0	1	0	11
1	1	0	1	0	12
0	0	1	1	0	13
1	0	1	1	0	14
0	1	1	1	0	15
1	1	1	1	0	16

M0	M1	M2	M3	M4	MODULUS
0	0	0	0	1	17
1	0	0	0	1	18
0	1	0	0	1	19
1	1	0	0	1	20
0	0	1	0	1	21
1	0	1	0	1	22
0	1	1	0	1	23
1	1	1	0	1	24
0	0	0	1	1	25
1	0	0	1	1	26
0	1	0	1	1	27
1	1	0	1	1	28
0	0	1	1	1	29
1	0	1	1	1	30
0	1	1	1	1	31
1	1	1	1	1	32

[Where: M(0:4) + 1 = MODULUS and M0 and M0 = 2^0, M1 = 2^1, M2 =2^2, M3 = 2^3, M4 = 2^4]

S4503 Output Counter Division Table

P0	P1	P-MODULUS
0	0	DISABLED
1	0	1
0	1	2
1	1	4

T0	T1	T2	T3	T-1 MODULUS
0	0	0	0	DISABLED
1	0	0	0	2
0	1	0	0	3
1	1	0	0	4
0	0	1	0	5
1	0	1	0	6
0	1	1	0	7
1	1	1	0	8
0	0	0	1	9
1	0	0	1	10
0	1	0	1	11
1	1	0	1	12
0	0	1	1	13
1	0	1	1	14
0	1	1	1	15
1	1	1	1	16

VCO frequency is limited to a maximum of 250 MHz when TTL outputs are used.

Where T1 (0:3) + 1 = MODULUS and

$T0 = 2^0$

$T1 = 2^1$

$T2 = 2^2$

$T3 = 2^3$

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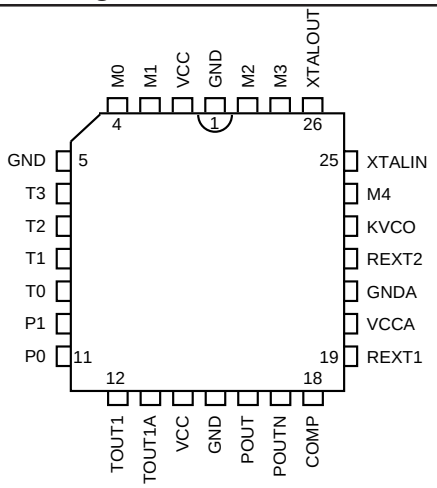
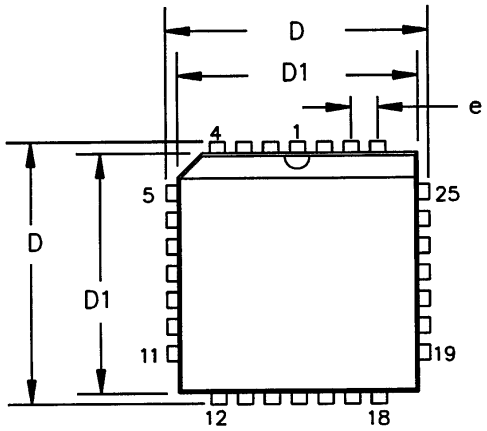
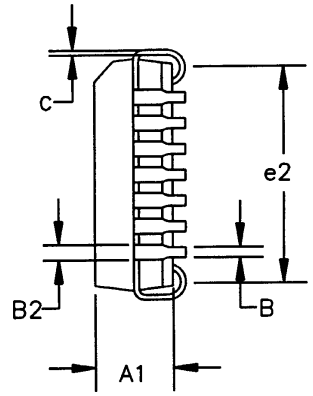
28 PLCC Package and Pinout



SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.487	.497
D1	.444	.459
e	.048	.052
e2	.410	.430



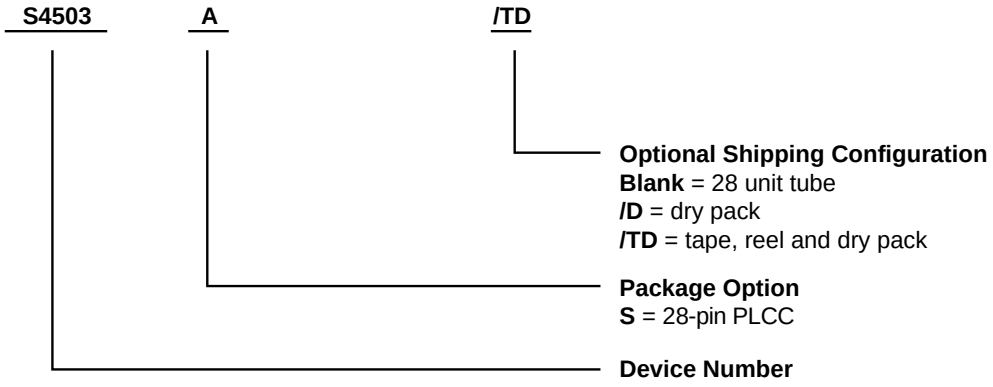


All dimensions nominal in inches.

Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Optional Shipping Configuration**



Example: S4503A/D
28-pin PLCC package, shipped dry packed in the standard tube.

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