

FEATURES

- Generates six clock outputs from 20 MHz to 80 MHz (HFOUT operates from 10 MHz to 40 MHz)
- Allows PECL or TTL reference input
- Provides differential PECL output at up to 160 MHz
- 21 selectable phase/frequency relationships for the clock outputs
- Compensates for clock skew by allowing output delay adjustment down to 3.125 ns increments
- TTL outputs have less than 400 ps maximum skew
- Lock Detect output indicates loop status
- Internal PLL with VCO operating at 160 to 320 MHz
- Test Enable input allows VCO bypass for open-loop operation
- Maximum 1.0 ns of phase error (750 ps from part to part)
- Proven 1.0 micron BiCMOS technology
- Single +5V power supply operation
- 44 PLCC package

APPLICATIONS

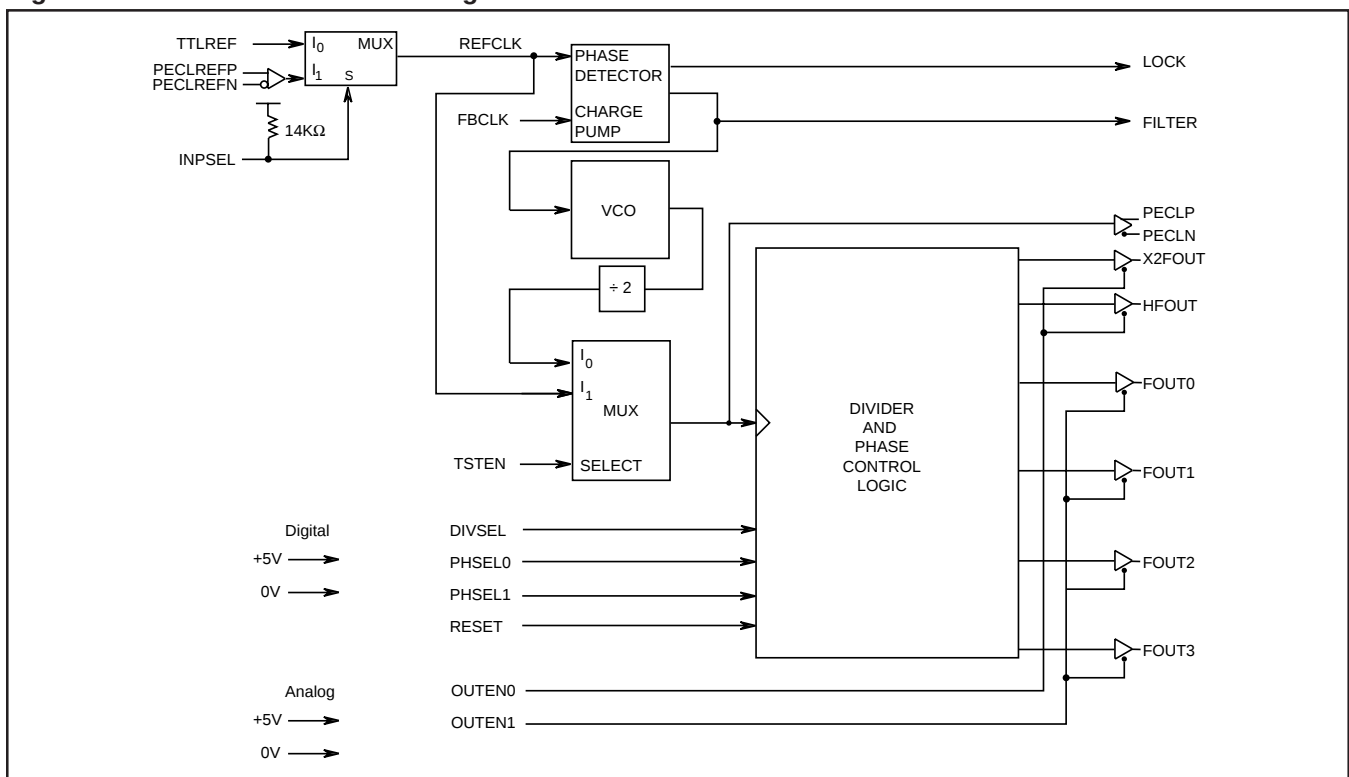
- CMOS ASIC Systems
- High-speed Microprocessor Systems
- Backplane Clock Deskew and Distribution

GENERAL DESCRIPTION

The S4405 BiCMOS clock generators allow the user to generate multiphase TTL clocks in the 10–80 MHz range with less than 400 ps of skew. Use of a simple off-chip filter allows an entire 160–320 MHz phase-locked loop (PLL) to be implemented on-chip. Divide-by-two and times-two outputs allow the ability to generate output clocks at half, equal to, or twice the reference clock input frequency. The reference is selectable to be either TTL or PECL. By using the programmable divider and phase selector, the user can select from up to 21 different output relationships. The outputs can be phase-adjusted in increments as small as 3.125 ns to tailor the clocks to exact system requirements.

Implemented in AMCC's proven 1.0 micron BiCMOS technology, the S4405 generates six TTL outputs and one differential PECL output. Output enables are provided for the various TTL banks, allowing clock control for board and system tests.

Figure 1. Clock Generator Block Diagram



FUNCTIONAL DESCRIPTION

This BiCMOS clock generator is designed to allow the user to generate TTL clocks, in the 10–80 MHz range, with less than 400 ps of skew. Implemented in AMCC's 1.0 μ BiCMOS technology, the internal VCO, phase detector, and programmable divider and phase selector allow the user to tailor the TTL output clocks for his/her system needs. The internal VCO can operate between 160 to 320 MHz, and the programmability allows the user to generate TTL output clocks in the 10–80 MHz range, and a differential +5V referenced ECL output at 80–160 MHz.

The clock generator offers the user the ability to select the appropriate phase relationship among the four FOUT0–3 TTL clock outputs. The phase selection choices are shown in Table 2.

The clock generator also allows the user to choose the divide-by ratio between the VCO frequency and the frequency of the FOUT0–3 signals. The VCO frequency can be divided by 4 when DIVSEL is low, and divided by 8 when DIVSEL is high. The divide ratio between the VCO and the pseudo ECL outputs, PECLP and PECLN, is a fixed divide-by-2.

The clock generator also has two output enable inputs which can be used to control which outputs toggle. OUTEN0 controls the HFOUT and X2FOUT outputs, and OUTEN1 controls the FOUT0–3 outputs. When the output enables are high, the outputs are disabled, and held in a high state.

REFCLK can be driven by either the TTLREF or PECLREF inputs. The reference clock source is selected with the INPSEL input. When INPSEL is low, the TTLREF input is selected as the reference clock.

The FOUT0–3 outputs are the main TTL output clocks that the generator supplies. The frequency of these outputs is determined by the REFCLK clock frequency and the output clock that is tied to the FBCLK input. FOUT0–3 will be equal to REFCLK, half of REFCLK, or twice the frequency of REFCLK. The X2FOUT TTL output provides a clock signal that is identical to the FOUT0 output in the divide-by-4

mode, but twice the FOUT0 frequency (max. freq. of 66 MHz) in the divide-by-8 mode. The HFOUT TTL output provides a clock signal that is also in phase with the FOUT0 output, but at half the FOUT0 frequency.

FILTER is the analog signal from the phase detector going into the VCO. This pin is provided so a simple external filter (a single resistor and one capacitor) can be included in the phase-locked loop of the clock generator.

The LOCK output goes high when the reference clock and FBCLK are within 2–4 ns of each other. This output tells the user that the PLL is in lock.

Three pins are included for test purposes. TESTEN allows the chip to use the REFCLK signal instead of the VCO output to clock the chip. This is used during chip test to allow the counters and control logic to be tested independently of the VCO. The RESET pin initializes the internal counter flip-flops to zeros, but several clock cycles are necessary before the outputs go to a zero state.

The minimum phase delay between FOUT0–3 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the output frequency by the divide-by ratio of four or eight. The minimum phase delay is equal to the period of the VCO frequency: $M_p = 1/\text{VCO freq.}$ Since the VCO can operate in the 160 MHz to 320 MHz range, the range of minimum phase delay values is 6.25 ns to 3.125 ns. Table 1 shows various FOUT/VCO frequencies and the associated phase resolution.

The charge pump and VCO portion of the chip use a separate analog power supply. This supply is brought onto the chip through a distinct set of power and ground pins. This supply should be free of digital switching noise.

Example:

In a typical system, designers may need several low-skew outputs, one early clock, one late clock, a clock at half the input clock frequency, and one at twice the input clock frequency. This system requirement

Table 1. Example Phase Resolution

FOUT0–3 Freq	Divider Select	VCO Freq	Min Phase Resolution
80 MHz	4	320 MHz	3.125 ns
66 MHz	4	266 MHz	3.75 ns
50 MHz	4	200 MHz	5.0 ns
40 MHz	4	160 MHz	6.25 ns
40 MHz	8	320 MHz	3.125 ns
33 MHz	8	266 MHz	3.75 ns
25 MHz	8	200 MHz	5.0 ns
20 MHz	8	160 MHz	6.25 ns

Table 2. Phase Selections

PHSEL1	PHSEL0	Phase Relationship
0	0	All at same phase
0	1	Outputs skewed by 90 degrees from each other
1	0	FOUT1 leads FOUT0 by minimum phase, FOUT2 lags FOUT0 by minimum phase, and FOUT3 lags FOUT0 by 90 degrees
1	1	Outputs skewed by minimum phase (determined by the divider selection, and the VCO frequency) from each other.

Note: The PECL output is not affected by the phase select inputs.

can be met by setting PHSEL1 to 1, PHSEL0 to 0, and feeding back FOUT0 to the FBCLK input (Row 10 of Table 3). The result is that FOUT0 will be phase-aligned to the reference clock, FOUT1 will lead the reference clock by a minimum phase delay, FOUT2 will lag the reference clock by a minimum phase delay, FOUT3 will phase-lag the reference clock by 90°, HFOUT will be phase-aligned with the reference clock but at half the frequency, and X2FOUT will be either phase-aligned at the same frequency as the reference clock if DIVSEL = 0, or at twice the frequency if DIVSEL = 1.

Enabling Outputs

The S4405 has two output-enable inputs that control which outputs toggle. When held LOW, OUTEN0 controls the frequency doubler output X2FOUT and the half-frequency output HFOUT. OUTEN1 controls the FOUT0–3 outputs. When an output enable pin is held High, its associated outputs are disabled and held in a High state.

Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 2) to be included in the PLL. AMCC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter and filter out noise on the reference clock input.

Reset

When the RESET pin is pulled low, all the internal states go to zero, but the outputs will not go low until one clock cycle later (VCO/2 or period of the reference clock). After the chip is reset, the PLL requires a resynchronization time before lock is again achieved.

Lock Detect

A lock detect function is provided by the LOCK output. When the selected reference clock and FBCLK

are within 2–4 ns of each other, the PLL is in lock, and the LOCK output goes High.

Power Supply Considerations

Power for the analog portion of the S4405 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 3). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise. The ferrite beads should exhibit 75Ω impedance at 10 MHz.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

BOARD LAYOUT CONSIDERATIONS

- The S4405 is sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4405 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 4) to avoid the possibility of noise due to crosstalk.

Figure 2. External PLL Filter

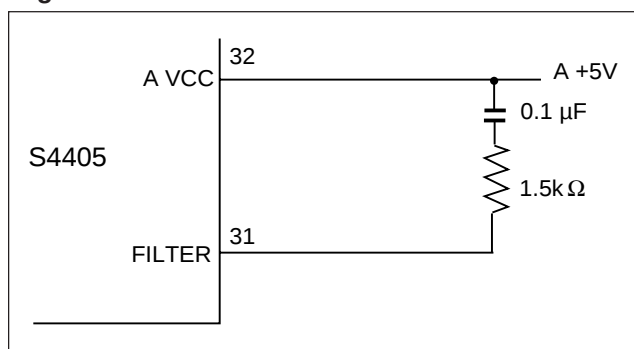
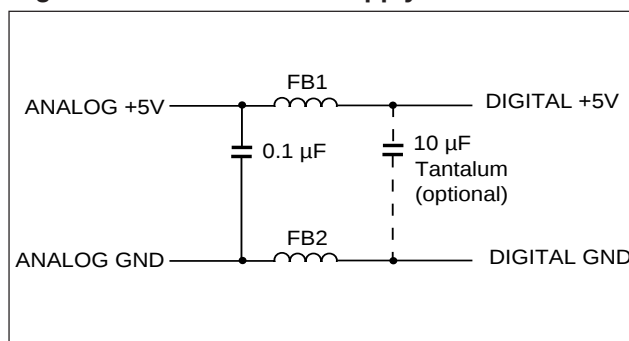
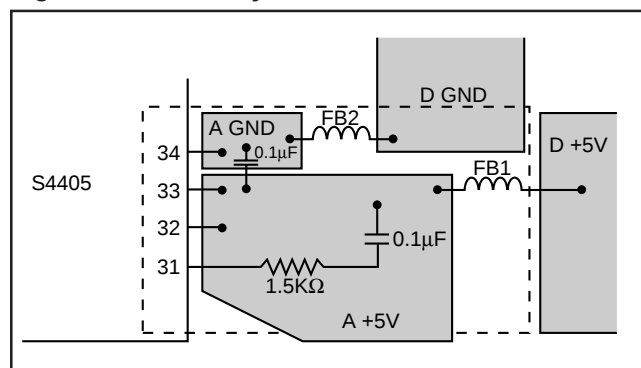


Figure 3. External Power Supply Filter



- The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.
- The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 4. Board Layout



Test Capabilities

The TSTEN input allows users to bypass the VCO and provide their own clock through the selected reference clock input. When TSTEN is High, the VCO is turned off and the REFCLK signal drives the divider/phase adjust circuitry, directly sequencing the outputs. The TSTEN and REFCLK inputs join the divider circuitry after the initial divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode and divided by four in the divide-by-eight mode.

PIN DESCRIPTIONS

Input Signals

TTLREF. TTL. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the FOUT0–FOUT3 outputs. INPSEL is used to select between this reference and the PECL reference PECLREFP/N.

PECLREFP/N. Differential PECL. Frequency reference supplied by the user. Selectable by the INPSEL input.

FBCLK. Feedback clock that, along with the reference clock input, determines the frequency of the FOUT0–FOUT3 outputs. One output is selected to feed back to this input. (See Table 3.)

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by four. When DIVSEL is high, the VCO frequency is divided by eight. (See Tables 1 and 3.)

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

OUTEN0. Active Low. Output enable signal that controls which outputs toggle. Controls the frequency doubler output (X2FOUT) and the half-frequency output (HFOUT).

OUTEN1. Active Low. Output enable signal that controls which outputs toggle. Controls the FOUT0–FOUT3 outputs.

RESET. Active Low. Initializes internal states for test purposes.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Therefore, REFCLK can be divided by two in the divide-by-four mode, and divided by four in the divide-by-eight mode, and used to directly sequence the outputs.

INPSEL. Allows user to select between TTLREF and PECLREF reference frequencies. When INPSEL is High, the PECLREF input is selected.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and capacitor) to be included in the PLL.

X2FOUT. Provides a clock signal identical to the FOUT0 output in the divide-by-four mode and twice the FOUT0 frequency (maximum of 80 MHz) in the divide-by-eight mode.

FOUT0. Clock output.

FOUT1. Clock output.

FOUT2. Clock output.

FOUT3. Clock output.

HFOUT. Provides a clock signal in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes.

PECLP/N. Differential PECL output, always one-half the VCO frequency.

LOCK. Goes high when the reference clock and FBCLK are within 2–4 ns of each other, demonstrating that the PLL is in lock.

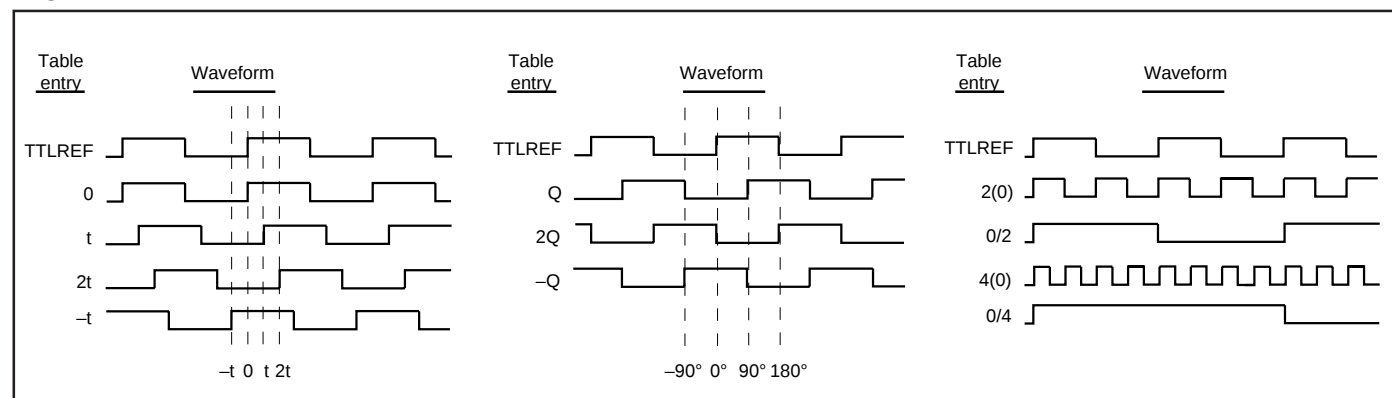
Table 3. Output Select Matrix

Configuration Number	Select Pins		Output Fed to FBCLK	Output Phase Relationships					÷4	÷8
	PHSEL1	PHSEL0		FOUT0	FOUT1	FOUT2	FOUT3	HFOUT	X2FOUT	
1	0	0	FOUT0–FOUT3	0	0	0	0	0/2	0	2(0)
2	0	0	HFOUT	2(0)	2(0)	2(0)	2(0)	0	2(0)	4(0)
3	0	0	X2FOUT (÷8)	0/2	0/2	0/2	0/2	0/4		0
4	0	1	FOUT0	0	Q	2Q	3Q	0/2	0	2(0)
5	0	1	FOUT1	–Q	0	Q	2Q	–Q/2	–Q	2(–Q)
6	0	1	FOUT2	–2Q	–Q	0	Q	–2Q/2	–2Q	2(–2Q)
7	0	1	FOUT3	–3Q	–2Q	–Q	0	–3Q/2	–3Q	2(–3Q)
8	0	1	HFOUT	2(0)	2(Q)	2(2Q)	2(3Q)	0	2(0)	4(0)
9	0	1	X2FOUT (÷8)	0/2	Q/2	2Q/2	3Q/2	0/4		0
10	1	0	FOUT0	0	–t	t	Q	0/2	0	2(0)
11	1	0	FOUT1	t	0	2t	Q+t	t/2	t	2(t)
12	1	0	FOUT2	–t	–2t	0	Q–t	–t/2	–t	2(–t)
13	1	0	FOUT3	–Q	–Q–t	–Q+t	0	–Q/2	–Q	2(–Q)
14	1	0	HFOUT	2(0)	2(–t)	2(t)	2(Q)	0	2(0)	4(0)
15	1	0	X2FOUT (÷8)	0/2	–t/2	t/2	Q/2	0/4		0
16	1	1	FOUT0	0	t	2t	3t	0/2	0	2(0)
17	1	1	FOUT1	–t	0	t	2t	–t/2	–t	2(–t)
18	1	1	FOUT2	–2t	–t	0	t	–2t/2	–2t	2(–2t)
19	1	1	FOUT3	–3t	–2t	–t	0	–3t/2	–3t	2(–3t)
20	1	1	HFOUT	2(0)	2(t)	2(2t)	2(3t)	0	2(0)	4(0)
21	1	1	X2FOUT (÷8)	0/2	t/2	2t/2	3t/2	0/4		0

Notes:

1. “0” implies the output is aligned with the reference clock.
2. “t” implies the output lags the reference clock by a minimum phase delay.
3. “Q” implies the output lags the reference clock by 90° of phase.
4. “–t” implies the output leads the reference clock by a minimum phase delay.
5. “–Q” implies the output leads the reference clock by 90° of phase.
6. “2()” implies the output is at twice the frequency of the reference clock.
7. “/2” implies the output is at half the frequency of the reference clock.
8. The PECLN/P Differential PECL output is not affected by the PHSEL inputs.

Legend



ABSOLUTE MAXIMUM RATINGS

TTL Supply Voltage VCC (GND = 0)	7.0 V
TTL Input Voltage (GND = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC CHARACTERISTICS (TTL I/O)

Symbol	Parameter	DC Test Conditions	Min	Typ ¹	Max	Units
V _{IH} ²	Input HIGH Voltage (TTL)	Guaranteed input HIGH voltage for all inputs	2.0			V
V _{IL} ²	Input LOW Voltage (TTL)	Guaranteed input LOW voltage for all inputs			0.8	V
V _{IK}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18mA		-0.8	-1.2	V
V _{OH}	Output HIGH Voltage	V _{CC} = Min, I _{OH} = -12mA ³	2.4			V
		I _{OH} = -24mA ³	2.0			V
V _{OL}	Output LOW Voltage	V _{CC} = Min, I _{OL} = 24mA ³			0.5	V
I _{IH}	Input HIGH Current	V _{CC} = Min, V _{IN} = 2.7V			10	μA
I _I	Input HIGH Current at Max	V _{CC} = Max, V _{IN} = V _{CC}			1.0	mA
I _{IL}	Input LOW Current	V _{CC} = Min, V _{IN} = 0.5V, INPSEL			-300	μA
		Others			-50	μA
I _{OS} ⁴	Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-25		-100	mA
I _{CC}	Static	V _{CC} = Max			95	mA
I _{CCT}	Total I _{CC} (Dynamic and Static)	C _{LOAD} = 25pF at 50 MHz			200	mA

DC CHARACTERISTICS (PECL I/O)

Symbol	Parameter	DC Test Conditions	Min	Typ ¹	Max	Units
V _{IH} ²	Input HIGH Voltage (PECL)	Guaranteed input HIGH voltage for all inputs	V _{CC} -1145		V _{CC} -600	V
V _{IL} ²	Input LOW Voltage (PECL)	Guaranteed input LOW voltage for all inputs	V _{CC} -2000		V _{CC} -1450	V
V _{OH}	Output HIGH voltage	V _{CC} = 5.0 V, Load = 50Ω to V _{CC} -2V	V _{CC} -1075		V _{CC} -650	V
V _{OL}	Output LOW voltage		V _{CC} -1980		V _{CC} -1585	V

1. Typical limits are at 25°C, V_{CC} = 5.0V.

2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher and are optimized to balance rise and fall times.

4. Maximum test duration one second.

Table 4. AC Specifications

Symbol	Description	S4405B-66		S4405B-80		Units
		Min	Max	Min	Max	
f_{VCO}	VCO Frequency	160	266	160	320	MHz
f_{REF}	REFCLK Frequency	10	66	10	80	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	5.0		5.0		ns
t_{PE}	Phase Error between TTLREF and FBCLK	-1	0	-1	0	ns
t_{PEP}	Phase Error between PECLREF and FBCLK	-3	-1	-3	-1	ns
t_{PED}	Phase Error Difference from Part to Part ¹	0	750	0	750	ps
t_{SKEW}	Output Skew ² (TTL)	0	400	0	400	ps
t_{DC}	Output Duty Cycle	45	55	45	55	%
f_{PECL}	PECLP/N Frequency	80	132	80	160	MHz
f_{FOUT}	FOUT Frequency ³ (TTL)	20	66	20	80	MHz
f_{HFOUT}	HFOUT Frequency ³	10	33	10	40	MHz
f_{2XFOUT}	2XFOUT Frequency ³	40	66	40	80	MHz
t_{PS}	Nominal Phase Shift Increment	3.75	6.25	3.125	6.25	ns
t_{OFD}	Tpd OUTEN0–2 to FOUTs, Disable	2	7	2	7	ns
t_{OFE}	Tpd OUTEN0–2 to FOUTs, Enable	2	7	2	7	ns
t_{IRF}	Input Rise/Fall Time	1	3	1	3	ns
t_{ORF}	FOUT Rise/Fall Time ⁴	0.5	1.5	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time ⁵		5		5	ms

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. $C_{LOAD} = 35$ pF.
4. With 35 pF output loading (0.8 V to 2.0 V transition).
5. Depends on loop filter chosen. (Number given is for example filter.)

Figure 5. Timing Waveforms

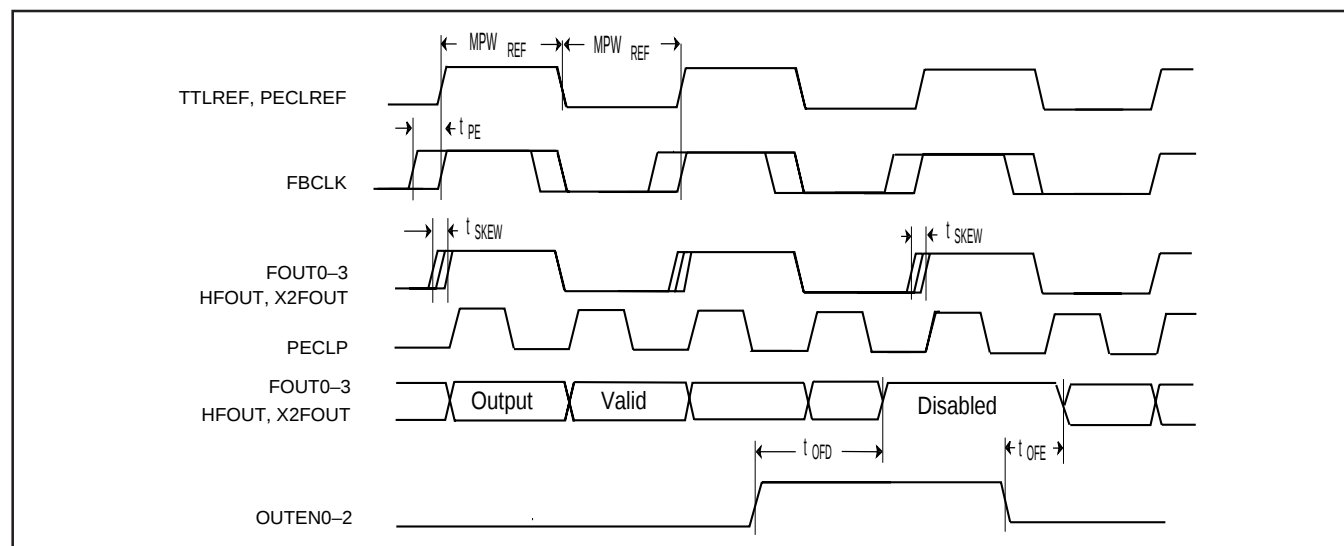
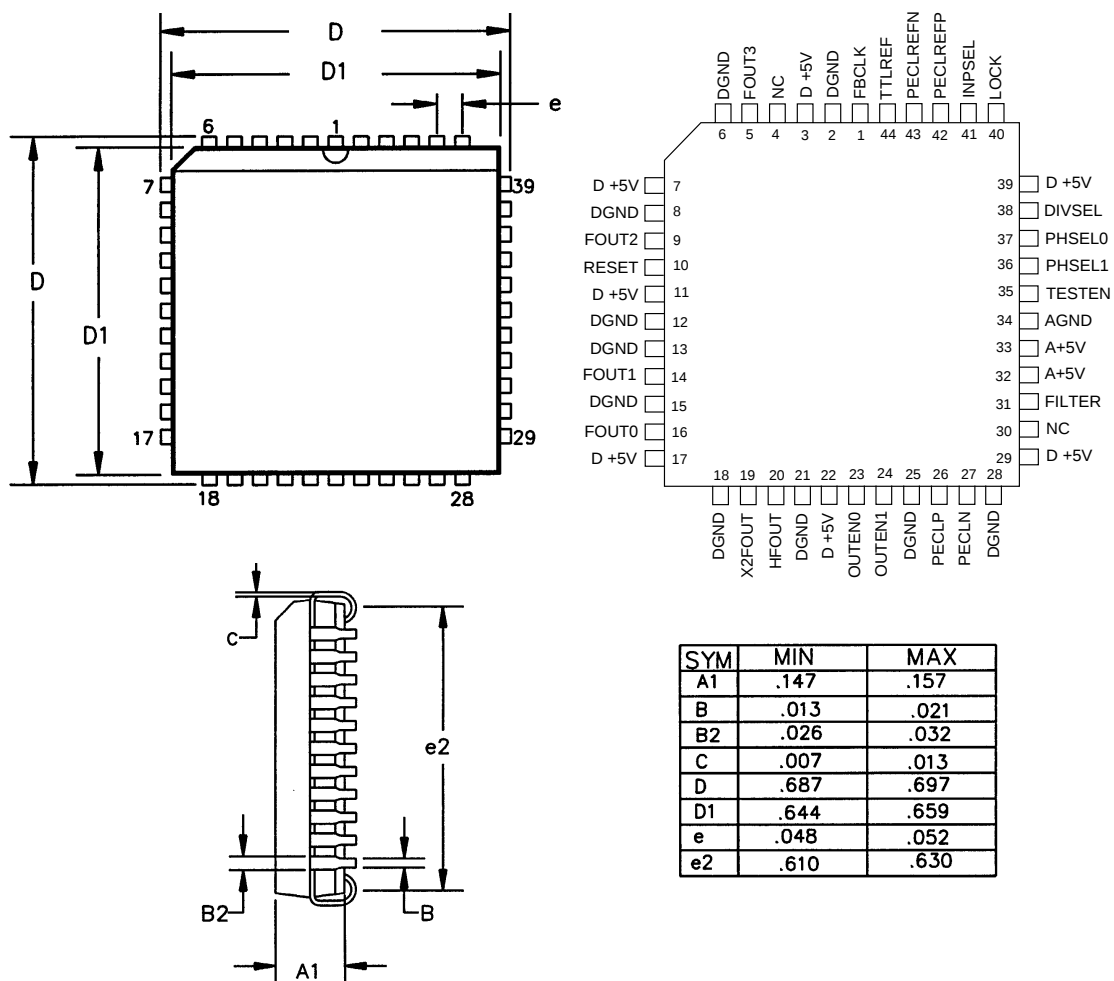


Figure 6. S4405 44 PLCC Package and Pinout

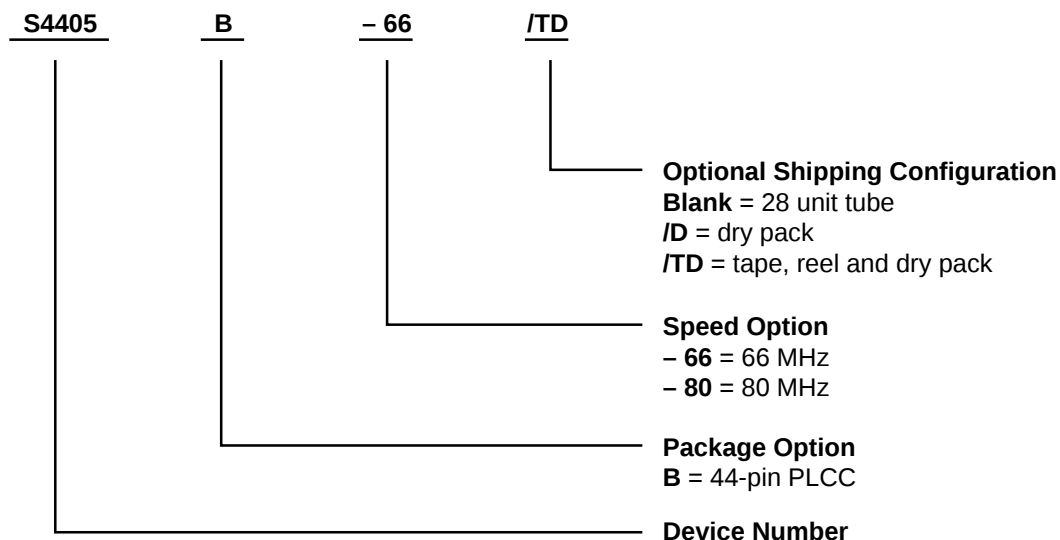


All dimensions nominal in inches.

Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Speed Option (if applicable)**
- **Optional Shipping Configuration**



Example: S4405B-66/D
44-pin PLCC package, 66 MHz, dry packed in the standard tube.

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Printed in U.S.A./12-08-95