SED1335

CMOS GRAPHIC LCD CONTROLLER

- **For Medium-Scale LCD**
- **Low Operating Voltage 2.7 to 5.0V**
- **On-Chip Character Generator ROM**

■ DESCRIPTION

The SED1335 is a CMOS low-power dot matrix liquid crystal graphic display controller. The device stores in external RAM display data sent by an 8-bit microcomputer, and generates all the signals required by the LCD drivers. The LSI incorporates an internal character generator ROM which supports user-defined characters (also an external CGROM can be supported).

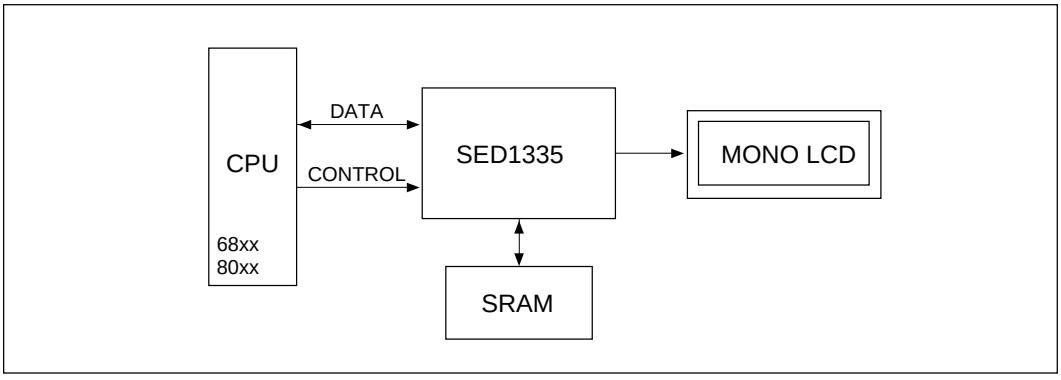
The SED1335 can be interfaced to high-speed microprocessors such as the Intel family or Motorola family. The controller supports a set of rich commands that will allow the user to create a layered display of characters and graphics.

Also, the controller functions as a pipeline buffer between the MPU and display memory so that low-cost, medium-speed SRAM can be used.

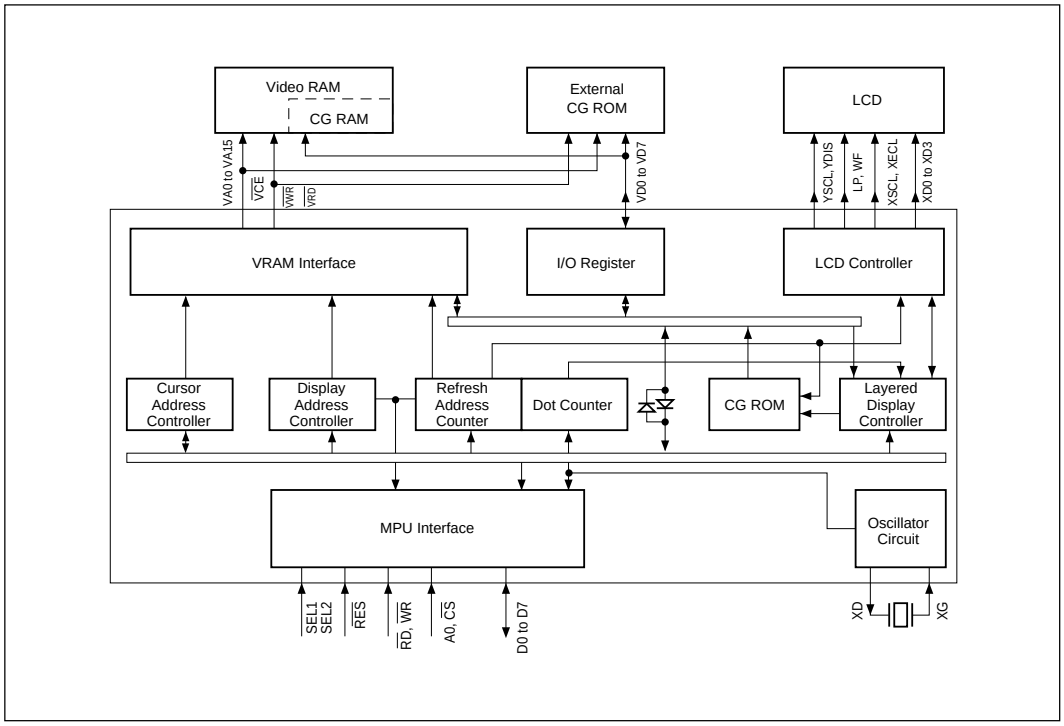
■ FEATURES

- CMOS low-power graphic and character display controller
- Selectable MPU interface is compatible with both the Intel family and the Motorola family
- Smooth scrolling support:
  Horizontal and vertical scroll
  Scrolling of selected areas of the display
- Multimode display:
  2 layers of overlapping characters and graphics
  3 layers of overlapping graphics
- Selectable display synthesis:
  Inverse video
  Flashing display, cursor on/off/blink
  Under and bar cursor, block cursor
  Simple animation
- Programmable cursor
- Internal character generator ROM
- Supports external character generator ROM:
  8×8 or 8×16 pixel characters
  Allowing mixing of ROM and RAM character sets
- Supports 64K bytes of memory:
  4K bytes of user-definable characters
  60K bytes of display memory
  in 2 of 32K $\times$ 8 100ns SRAM
  or in 8 of 8K $\times$ 8 100ns SRAM
- Display duty ..... 1/2 to 1/256
- Low power dissipation
  5mA (typical)
  0.05µA (typical), standby
- Logic power supply ..... 2.7 to 5.5V
- Package: ..... Plastic QFP5-60 pin (F0A)
  Plastic QFP6-60 pin (F0B)

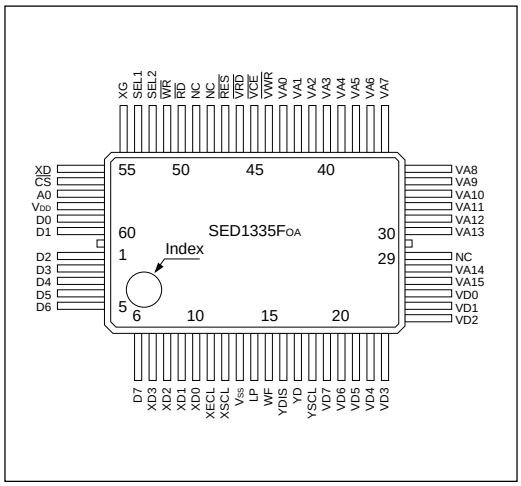
■ SYSTEM BLOCK DIAGRAM

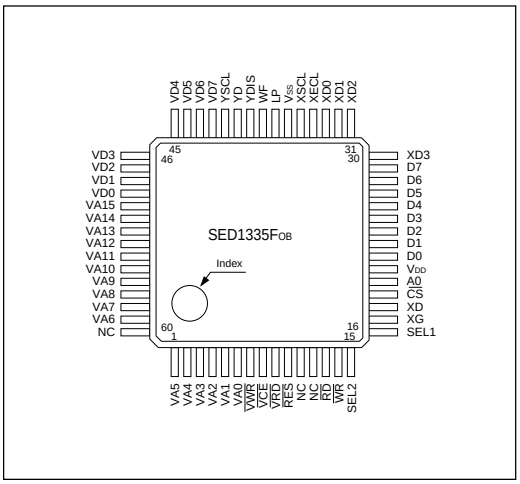


■ BLOCK DIAGRAM



■ PINOUT





■ PIN DESCRIPTION

Pin Name	Pin No.		I/O	Functions
	SED1335F0A	SED1335F0B		
XG	54	17	I	Oscillator terminal
XD	55	18	O	Oscillator terminal
V_{DD}	58	21	+5V	Power supply
V_{SS}	13	36	GND(0V)	Power supply
SEL1,2	53 • 52	16 • 15	I	MPU interface format selection
D0 to D7	59 to 60, 1 to 6	22 to 29	I/O	Data bus
A0	57	20	I	Data type selection
$\overline{RD}$	50	13	I	80 series Read strobe signal 68 series "E" clock
$\overline{WR}$	51	14	I	80 series Write strobe signal 68 series R/W signal
$\overline{CS}$	56	19	I	Chip select
$\overline{RES}$	47	10	I	Reset
VA15 to VA0	27 • 28, 30 to 43	1 to 6, 50 to 59	O	VRAM address bus
VD7 to VD0	19 to 26	42 to 49	I/O	VRAM data bus
$\overline{VWR}$	44	7	O	VRAM write signal
$\overline{VRD}$	46	9	O	VRAM read signal
$\overline{VCE}$	45	8	O	VRAM chip enable
XD3 to XD0	7 to 10	30 to 33	O	Dot data output bus to X driver
XSCL	12	35	O	Dot data shift clock for X driver
XECL	11	34	O	Chip enable shift clock for X driver
LP	14	37	O	Dot data latch pulse
WF	15	38	O	Frame signal
YSCL	18	41	O	Scan data shift clock for Y driver
YD	17	40	O	Scan data output
YDIS	16	39	O	Power down signal when display is OFF

NC: No Connection

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.3 to 7.0	V
Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–60 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

- **DC Electrical Characteristics (1)**

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_a = –20 to 75°C)

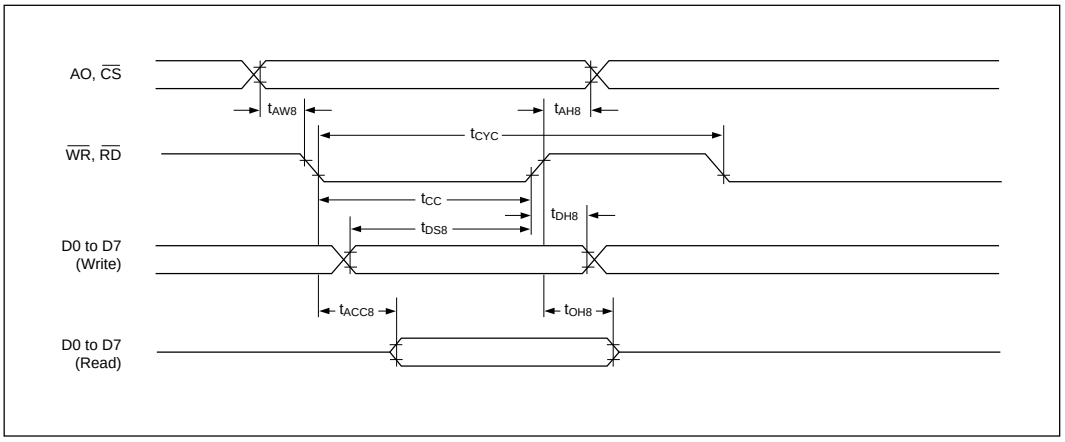
Parameter		Symbol	Condition	Min	Typ	Max	Unit	Terminal
Operating voltage		V_{DD}		4.5	5.0	5.5	V	V_{DD}
Register data retention voltage		V_{OH}		2.0	—	6.0	V	
TTL	High level input voltage	V_{IHT}		0.5xV_{DD}	—	V_{DD}	V	D0 to D7, A0, CS, RD, WR, VD0 to VD7, VA0 to VA15, VCE, VRD, VWR
	Low level input voltage	V_{ILT}		V_{SS}	—	0.2xV_{DD}	V	
	High level output voltage	V_{OHT}	I_{OH} = –5.0mA	2.4	—	—	V	
	Low level output voltage	V_{OLT}	I_{OL} = 5.0mA	—	—	V_{SS}+0.4	V	
CMOS	High level input voltage	V_{IHC}		0.8xV_{DD}	—	V_{DD}	V	SEL1, SEL2, YD, XD0 to XD3, XSCL, YDIS, LP, WF, CL0, XECL, YSCL
	Low level input voltage	V_{ILC}		V_{SS}	—	0.2xV_{DD}	V	
	High level output voltage	V_{OHC}	I_{OH} = –2.0mA	V_{DD}–0.4	—	—	V	
	Low level output voltage	V_{OLC}	I_{OL} = 2.0mA	—	—	V_{SS}+0.4	V	
SCHMITT	Positive trigger threshold voltage	V_{T+}		0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V	$\overline{RES}$
	Negative trigger threshold voltage	V_{T-}		0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V	
Input leakage current		I_{LI}	V_{IN} = V_{DD}/V_{SS}	—	0.05	2.0	µA	
Output leakage current		I_{LO}		—	0.10	5.0	µA	
Average operating current		I_{opr}	f_{osc} = 10MHz, No-load 256 × 200 dot	—	11	15	mA	V_{DD}
Standby current		I_Q	Sleep X_G, $\overline{CS}$, $\overline{RD}$ = V_{DD}	—	0.05	20	µA	V_{DD}
Oscillation frequency		f_{osc}	AT X'tal	1.0	—	10.0	MHz	XG, XD
External clock frequency		f_{CL}	Duty 47.5%	1.0	—	10.0	MHz	
Feed back resistance		R_f		0.5	1.0	3.0	MΩ	

● **DC Electrical Characteristics (2)**

(V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –20 to 75°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Terminal
Operating voltage		V_{DD}		2.7	3.5	4.5	V	V_{DD}
Register data retention voltage		V_{OH}		2.0	—	6.0	V	
TTL	High level input voltage	V_{IHT}		0.8xV_{DD}	—	V_{DD}	V	D0 to D7, A0, CS, RD, WR, VD0 to VD7, VA0 to VA15, VCE, VRD, VWR
	Low level input voltage	V_{ILT}		V_{SS}	—	0.2xV_{DD}	V	
	High level output voltage	V_{OHT}	I_{OH} = –3.0mA	V_{DD}–0.4	—	—	V	
	Low level output voltage	V_{OLT}	I_{OL} = 3.0mA	—	—	V_{SS}+0.4	V	
CMOS	High level input voltage	V_{IHC}		0.8xV_{DD}	—	V_{DD}	V	SEL1, SEL2, YD, XD0 to XD3, XSCL, YDIS, LP, WF, CL0, XECL, YSCL
	Low level input voltage	V_{ILC}		V_{SS}	—	0.2xV_{DD}	V	
	High level output voltage	V_{OHC}	I_{OH} = –1.0mA	V_{DD}–0.4	—	—	V	
	Low level output voltage	V_{OLC}	I_{OL} = 1.0mA	—	—	V_{SS}+0.4	V	
SCHMITT	Positive trigger threshold voltage	V_{T+}		0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V	$\overline{RES}$
	Negative trigger threshold voltage	V_{T-}		0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V	
Input leakage current		I_{LI}	V_{IN} = V_{DD}/V_{SS}	—	0.05	2.0	µA	
Output leakage current		I_{LO}		—	0.10	5.0	µA	
Average operating current		I_{opr}	f_{osc} = 6.1MHz, No-load 256 × 200 dot	—	3.5 (V_{DD}=3.5V)	7.0	mA	V_{DD}
Standby current		I_Q	Sleep X_G, $\overline{CS}$, $\overline{RD}$ = V_{DD}	—	0.05	20	µA	V_{DD}
Oscillation frequency		f_{osc}	AT X'tal	1.0	—	8.0	MHz	XG, XD
External clock frequency		f_{CL}	Duty 47.5%	1.0	—	8.0	MHz	
Feed back resistance		R_f		0.7	—	4.0	MΩ	

- **Timing Diagrams**
  - **8080-Family Interface Timing**



T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{CS}$	t_{AH8}	Address hold time	10	—	10	—	ns	CL = 100 pF
	t_{AW8}	Address setup time	0	—	0	—	ns	
WR, $\overline{RD}$	t_{CYC}	System cycle time	See note	—	See note	—	ns	
	t_{CC}	Strobe pulsewidth	120	—	150	—	ns	
D0 to D7	t_{DS8}	Data setup time	120	—	120	—	ns	
	t_{DH8}	Data hold time	5	—	5	—	ns	
	t_{ACC8}	$\overline{RD}$ access time	—	50	—	80	ns	
	t_{OH8}	Output disable time	10	50	10	55	ns	

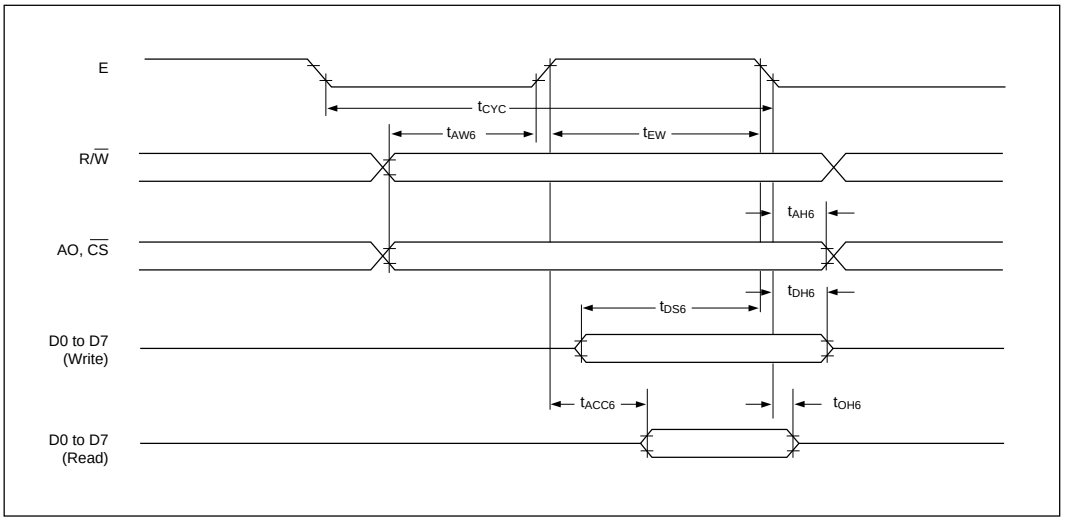
Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

○ **6800-Family Interface Timing**



Note: tCYC6 indicates the interval during which $\overline{CS}$ is LOW and E is HIGH.

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{CS}$, R/$\overline{W}$	t_{CYC6}	System cycle time	See note	—	See note	—	ns	CL = 100 pF
	t_{AW6}	Address setup time	0	—	10	—	ns	
	t_{AH6}	Address hold time	0	—	0	—	ns	
D0 to D7	t_{DS6}	Data setup time	100	—	120	—	ns	
	t_{DH6}	Data hold time	0	—	0	—	ns	
	t_{OH6}	Output disable time	10	50	10	75	ns	
	t_{ACC6}	Access time	—	85	—	130	ns	
E	t_{EW}	Enable pulsewidth	120	—	150	—	ns	

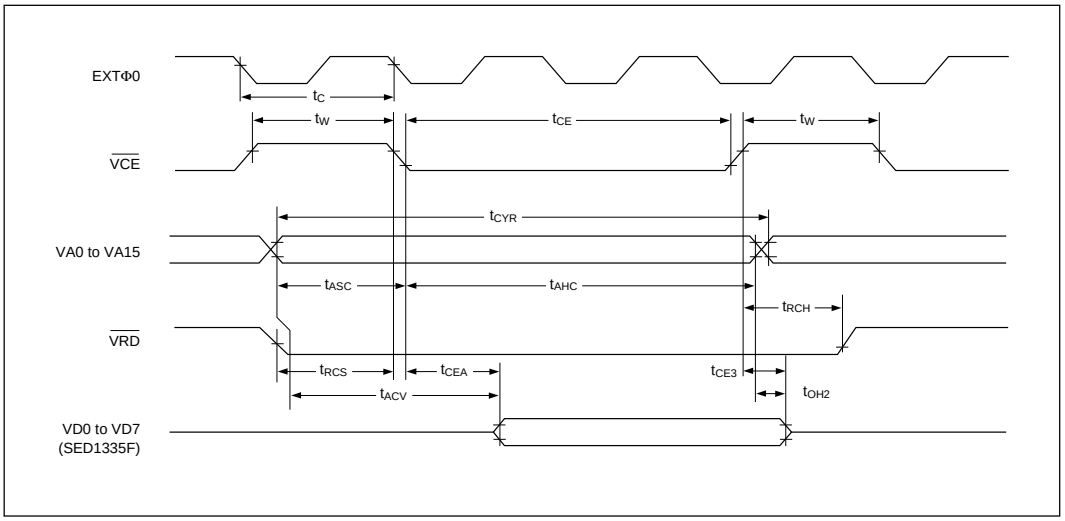
Note: For memory control and system control commands:

$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

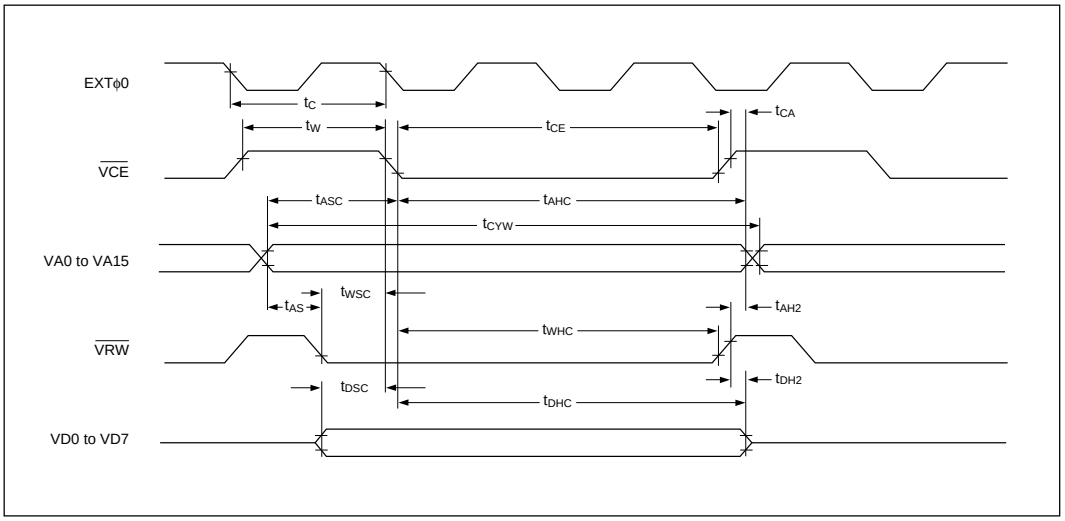
○ **Display Memory Read Timing**



T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulsewidth	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulsewidth	2t_C – 30	—	2t_C – 30	—	ns	
VA0 to VA15	t_{CYR}	Read cycle time	3t_C	—	3t_C	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 100	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	2t_C – 30	—	2t_C – 40	—	ns	
$\overline{VRD}$	t_{RCS}	Read cycle setup time to falling edge of $\overline{VCE}$	t_C – 45	—	t_C – 60	—	ns	
	t_{RCH}	Read cycle hold time from rising edge of $\overline{VCE}$	0.5t_C	—	0.5t_C	—	ns	
VD0 to VD7	t_{ACV}	Address access time	—	3t_C – 100	—	3t_C – 115	ns	
	t_{CEA}	$\overline{VCE}$ access time	—	2t_C – 80	—	2t_C – 90	ns	
	t_{OH2}	Output data hold time	0	—	0	—	ns	
	t_{CE3}	$\overline{VCE}$ to data off time	0	—	0	—	ns	

○ **Display Memory Write Timing**

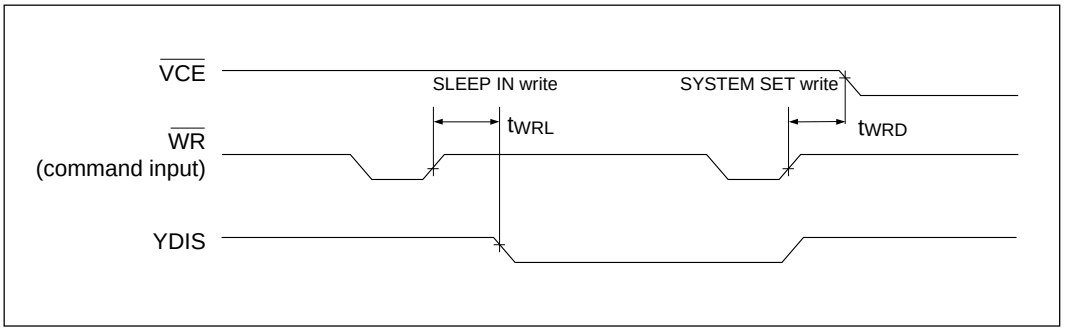


T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	tW	$\overline{VCE}$ HIGH-level pulse-width	tC – 50	—	tC – 50	—	ns	
	tCE	$\overline{VCE}$ LOW-level pulse-width	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYW	Write cycle time	3tC	—	3tC	—	ns	
	tAHC	Address hold time from falling edge of $\overline{VCE}$	2tC – 30	—	2tC – 40	—	ns	
	tASC	Address setup time to falling edge of $\overline{VCE}$	tC – 70	—	tC – 110	—	ns	
	tCA	Address hold time from rising edge of $\overline{VCE}$	0	—	0	—	ns	
	tAS	Address setup time to falling edge of $\overline{VWR}$	0	—	0	—	ns	
	tAH2	Address hold time from rising edge of $\overline{VWR}$	10	—	10	—	ns	
$\overline{VWR}$	tWSC	Write setup time to falling edge of $\overline{VCE}$	tC – 80	—	tC – 115	—	ns	
	tWHC	Write hold time from falling edge of $\overline{VCE}$	2tC – 20	—	2tC – 20	—	ns	
VD0 to VD7	tDSC	Data input setup time to falling edge of $\overline{VCE}$	tC – 85	—	tC – 125	—	ns	
	tDHC	Data input hold time from falling edge of $\overline{VCE}$	2tC – 30	—	2tC – 30	—	ns	
	tDH2	Data hold time from rising edge of $\overline{VWR}$	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

○ **SLEEP IN Command Timing**



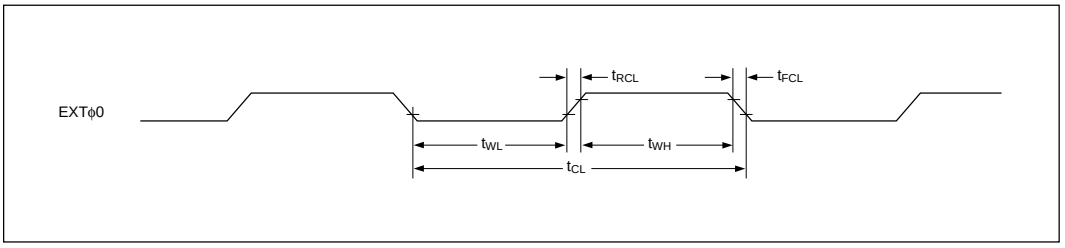
T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
$\overline{WR}$	t_{WRD}	$\overline{VCE}$ falling-edge delay time	*1	—	*1	—	ns	CL = 100 pF
	t_{WRL}	YDIS falling-edge delay time	—	*2	—	*2	ns	

Notes:

1. $t_{WRD} = 18t_C + t_{OSS} + 40$ (t_{OSS} is the time delay from the sleep state until stable operation)
2. $t_{WRL} = 36t_C \times [TC/R] \times [L/F] + 70$

● **External Oscillator Signal Timing**



T_a = –20 to 75°C

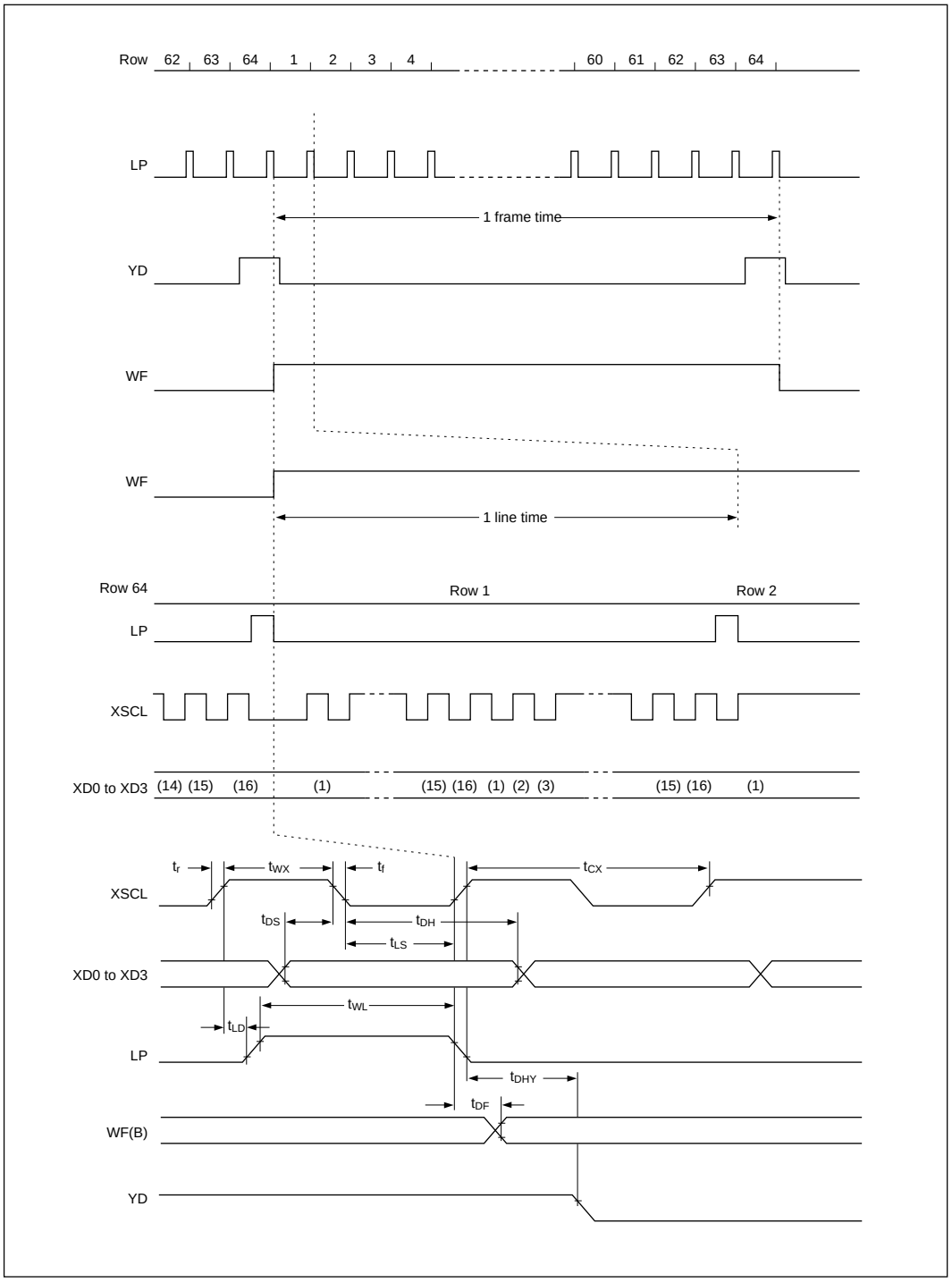
Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	t_{RCL}	External clock rise time	—	15	—	15	ns	
	t_{FCL}	External clock fall time	—	15	—	15	ns	
	t_{WH}	External clock HIGH-level pulsewidth	*1	*2	*1	*2	ns	
	t_{WL}	External clock LOW-level pulsewidth	*1	*2	*1	*2	ns	
	t_C	External clock period	100	—	125	—	ns	

Notes:

1. $(t_C - t_{RCL} - t_{FCL}) \times \frac{475}{1000} < t_{WH}, t_{WL}$
2. $(t_C - t_{RCL} - t_{FCL}) \times \frac{525}{1000} > t_{WH}, t_{WL}$

○ **LCD Output Timing**

The following characteristics are for a 1/64 duty cycle.

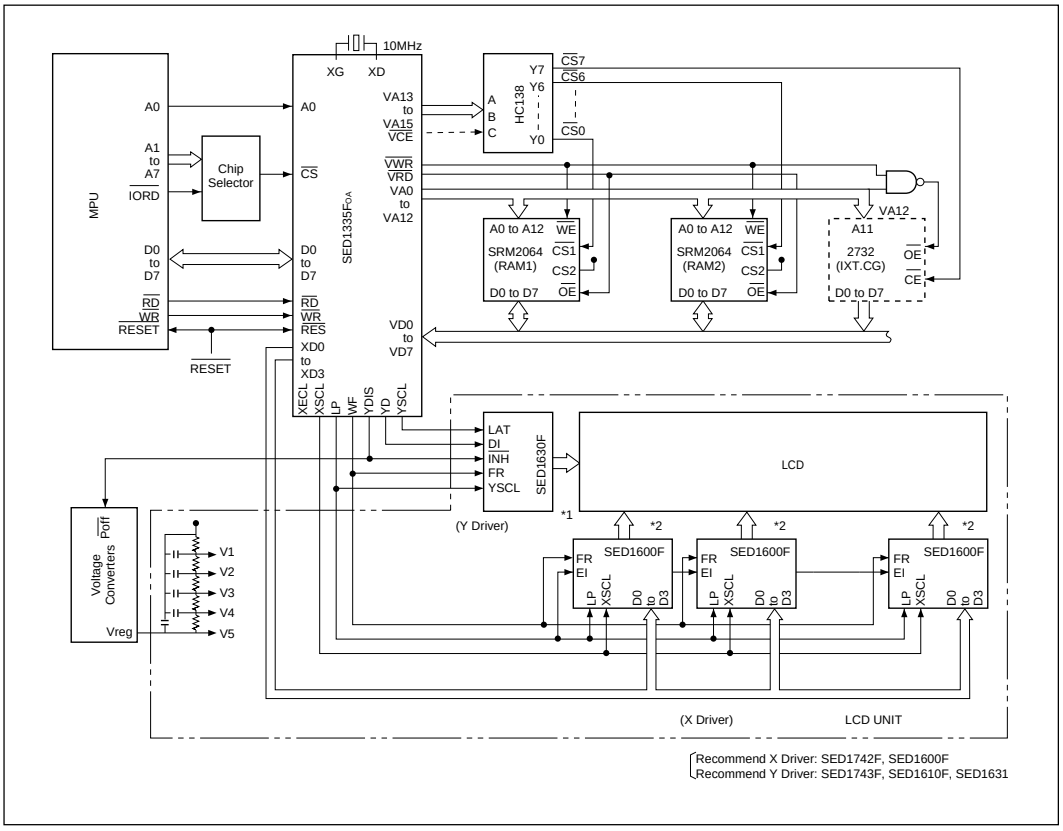


T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
	t_r	Rise time	—	30	—	40	ns	CL = 100pF
	t_f	Fall time	—	30	—	40	ns	
XSCL	t_{CX}	Shift clock cycle time	4t_C	—	4t_C	—	ns	
	t_{WX}	XSCL clock pulsewidth	2t_C – 60	—	2t_C – 60	—	ns	
XD0 to XD3	t_{DH}	X data hold time	2t_C – 50	—	2t_C – 50	—	ns	
	t_{DS}	X data setup time	2t_C – 100	—	2t_C – 105	—	ns	
LP	t_{LS}	Latch data setup time	2t_C – 50	—	2t_C – 50	—	ns	
	t_{WL}	LP pulsewidth	4t_C – 80	—	4t_C – 120	—	ns	
	t_{LD}	LP delay time from XSCL	0	—	0	—	ns	
WF	t_{DF}	Permitted WF delay	—	50	—	50	ns	
YD	t_{DHY}	Y data hold time	2t_C – 20	—	2t_C – 20	—	ns	

Note: The SED1335F reads display memory data from the address of the top left corner of the display screen, then scans horizontally until it reaches the address for the bottom right corner of the display screen. Therefore, each line of X-driver data is sent starting from the left side of the display line.

■ EXAMPLE OF APPLICATION



■ **CHARACTER CODE TABLE (Built-in Character Generator)**