Using TI's CDCVF111 With SLK2501 Serial Gigabit Transceiver for SONET and Gigabit Ethernet Applications

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ABSTRACT

SONET/SDH and gigabit ethernet applications all have stringent timing requirements, which mandate the use of low-skew, low-jitter clock distribution. Texas Instruments has developed two products targeting these systems applications. The first product is the CDCVF111, a 1:9 low-skew, low-jitter differential LVPECL clock driver. The second is the SLK2501, a multirate (OC-48/24/12/3) serial gigabit transceiver. This application note demonstrates that the total jitter transfer at the output of the SLK2501 when driven by the CDCVF111 meets the 20-ps peak-to-peak jitter requirement. Sufficient jitter measurements are included in Tables 1 and 2.

Introduction

This application report discusses various jitter measurements of TI's CDCVF111. The CDCVF111 is 1:9 low-skew, low-jitter differential LVPECL (low-voltage positive-referenced emitter coupled logic) clock driver. The CDCVF111 is characterized for industrial (-40°C to 85°C) temperature with a specified operation frequency of 650 MHz. These features make it ideal for various SONET and gigabit ethernet applications, where skew and jitters are of major concern. Among the many applications, SONET and gigabit ethernet have very stringent jitter and skew requirements and system-timing budgets are normally tight. The need for differential signaling is critical in reducing various noise components. These issues include EMI (electromagnetic interference), signal reflection, power consumption, capacitive and inductive crosstalk, and transient switching noise. All measurements contained in this report were taken at room temperature and a 3.3-V power supply. Figure 1 indicates various jitter measurement points.

Test Summary

The following summarizes worst-case peak-to-peak and RMS jitter measurement points as indicated in Figure 1. The first point (point 1) is the output jitter of the SaRonix or the Raltron VCXO alone. The second point (point 2) indicates the output jitter of the CDCVF111 when driven by either VCXO. The third point (point 3) represents the total output jitter at the end of the chain, where the corresponding VCXO is driving the CDCVF111, which drives the serial gigabit transceiver (SLK2501).

It is evident from the following graph that the CDCVF111 only adds 3 ps of peak-to-peak jitter when driven by either SaRonix's or Raltron's 622.08-MHz VCXO.

Test Setup

Proper termination is critical in high-speed logic since most connections are treated as transmission lines. The proper method of terminating emitter-coupled logic is 50 Ω to V_{CC} – 2 V.

It is important to note that both VCXO's and the CDCVF111 all have an offset of 1.3 V, which means that we need to compensate for this offset and add 1.3 V to the VOH/VOL values in Tables 1 and 2. Moreover, the value of the external coupling capacitors (C_C) used is about 1.5 nF. Additionally, the split 50-Ω, the 3-kΩ pullup resistor, and the 4.5-kΩ pulldown resistors are integrated on-chip of the SLK2501 transceiver; consequently they are not required in an application.

We should reiterate an important point we made earlier, namely, that the supply voltage of the SaRonix, the Raltron VCXO's, and CDCVF111 were all set at V_{CC} = 2 V and V_{SS} = -1.3 V. With that in mind, it is important to remember to add a 1.3-V offset to VOH and VOL in Tables 1 and 2. Notice further that, the 50-Ω termination resistors should be connected to ground, which is the V_{CC} - 2 V point in this setup.

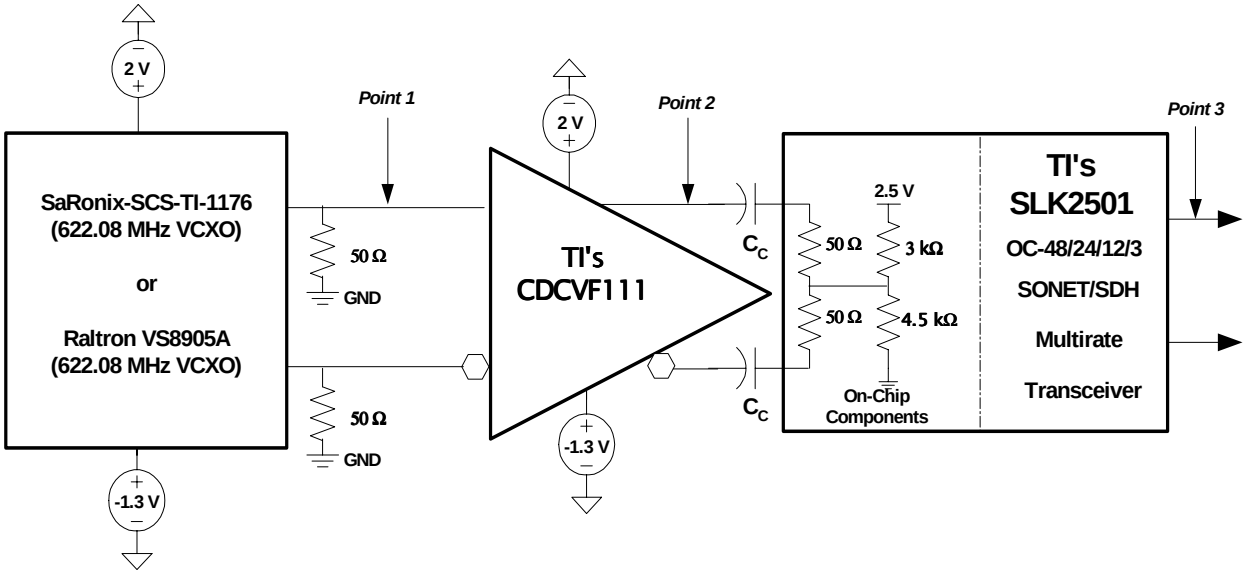

Figure 1. Test Setup: SaRonix's or Raltron's VCXO Driving CDCVF111 Driving SLK2501

Since in real applications a V_{CC} – 2 V supply is not readily available, the 50-Ω termination resistor is normally replaced by a Thevenin equivalent network composed of two resistors R1 and R2 as shown in Figure 3. This Thevenin termination network (R1 and R2) is referred to as dc-coupling. The values of R1 and R2 are chosen such that:

the parallel combination or R1$||$R2 is equal to the characteristic impedance of the transmission line, Zo = 50 Ω, that is: $\frac{R1 \times R2}{R1 + R2} = Zo = 50\ \Omega \rightarrow$ Equation 1

Referring to point B in Figure 3, we can see that the ratio of R2 to the sum of R1 and R2 should equal the ratio of V_{CC} – 2 V to Vcc, that is:

$$\frac{R2}{R1 + R2} = \frac{(Vcc - 2\ V)}{Vcc} \rightarrow \text{Equation 2}$$

Results: For a V_{CC} = 3.3-V supply, the values are: R1 ≅ 130 Ω and R2 ≅ 83 Ω.

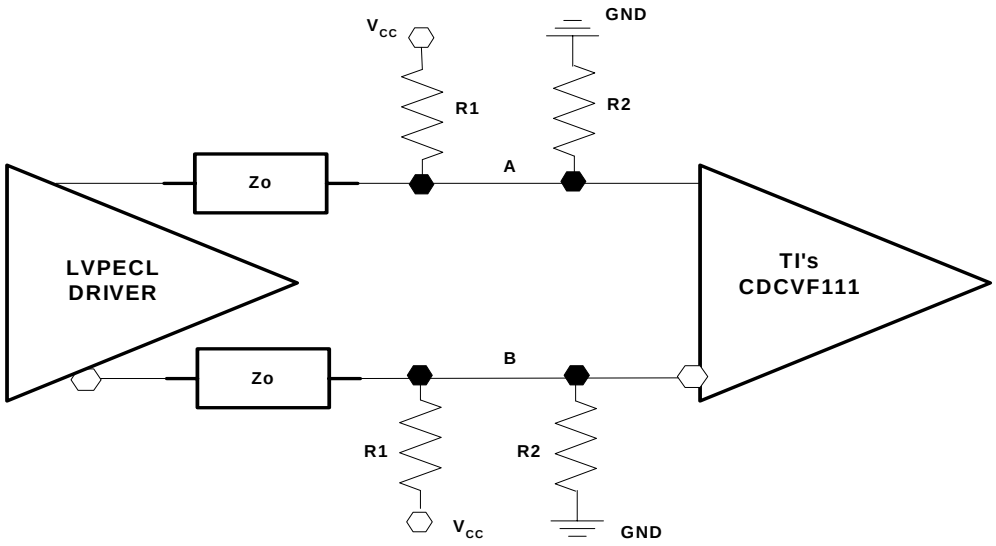

Figure 2. DC-Coupling Between LVPECL and LVPECL

Test Results

The input and output jitter requirement for TI's SLK2501 (serial SONET/SDH multirate transceiver) is ≤20 ps of peak-to peak (0.05 UI to 0.1 UI) for proper operation. It is evident from the following graph that the CDCVF111 transfers a maximum of 3 ps of peak-to-peak jitter, well below the input specification.

It is apparent from the following graph that, the total jitter at the end of the chain (VCXOs + CDCVF111 + SLK2501) is about 14 ps, which is well below the 20-ps specification.

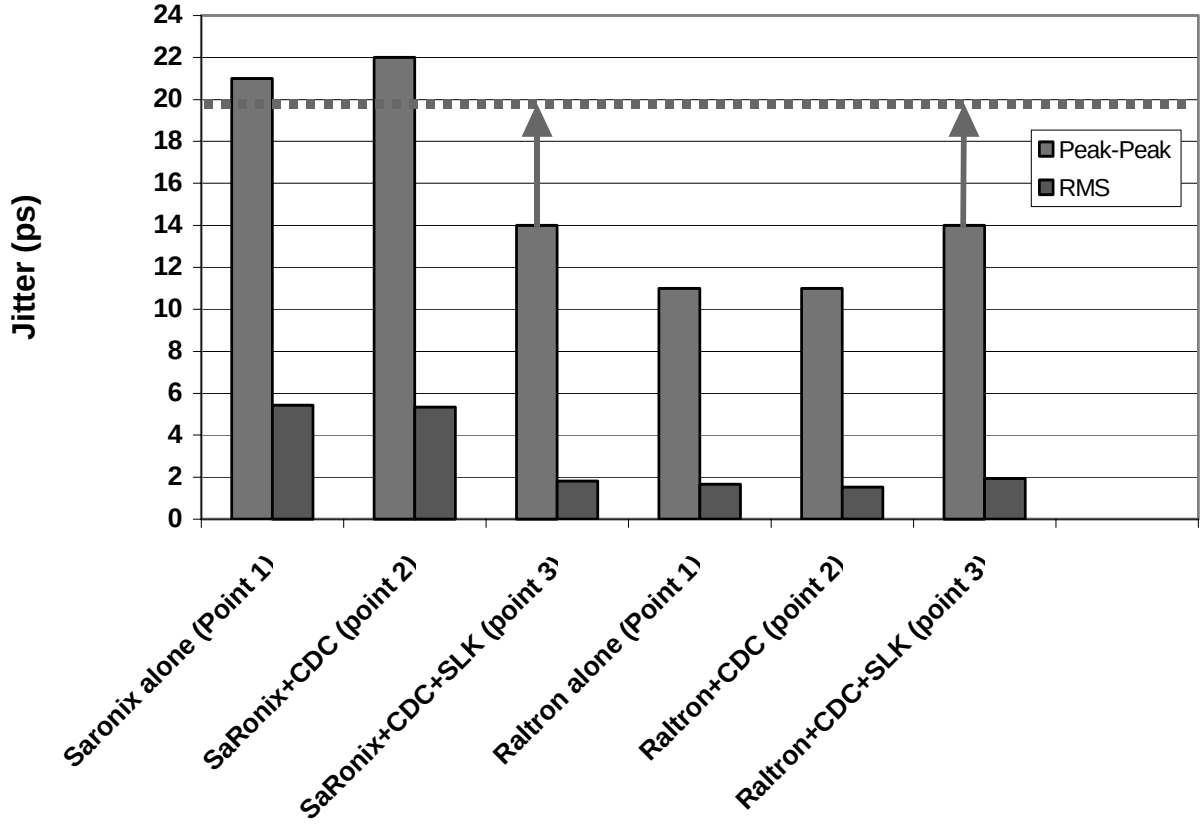

Figure 3. Jitter Comparison of All 3 Points in Figure 1

Output Jitter of SLK2501 Driven by CDCVF111 Driven by Either Raltron or SaRonix's VCXOs (Point 3 in Figure 1)

Tables 1 and 2 list the detail output jitter values of the SLK2501 and CDCVF111 when driven by either SaRonix or Raltron 622.08-MHz VCXO. Table 1 shows the output jitter at point 2 of Figure 1, while Table 2 shows the jitter output at the end of the chain, point 3 of Figure 1.

Table 1. Jitter Output of TI's CDCVF111 (Point 2 in Figure 1)

Reference Clock	Jitter (ps)				Single-Ended Output levels (mV)		
	PP	C-C (+)	C-C (-)	RMS	VOH	VOL	Amplitude
SaRonix VCXO +CDCVF111	22	19	21	5.34	928	368	560
	20	18	19	4.02			
	19	17	19	4.06			
	19	17	19	4.04			
	22	20	21	5.24			
Raltron VCXO +CDC111	10	10	10	1.56	954	402	552
	11	9	9	1.47			
	11	10	10	1.45			
	10	9	10	1.44			
	11	10	10	1.53			

Table 2. Jitter Output of TI's SLK2501 (Point 3 in Figure 1)

Reference Clock	Jitter (ps)				Single-Ended Output levels (mV)		
	PP	C-C (+)	C-C (-)	RMS	VOH	VOL	Amplitude
SaRonix VCXO +CDCVF111 +SLK2501	14	11	13	1.82	413	-381	794
	13	11	12	1.95			
	13	13	11	1.92			
	13	11	12	1.94			
	13	11	12	1.88			
Raltron VCXO +CDCVF111 +SLK2501	13	10	11	1.72	413	-381	794
	13	11	12	1.95			
	14	12	12	1.95			
	14	12	11	1.94			
	13	11	12	1.94			

Table 3. Clock Drivers Supporting Serial Gigabit Transceivers

Serial / Gigabit Transceiver	Recommended Clock Driver
TLK3104SA/SC	CDCVF111 up to 622.08 MHz
	CDC111 up to 500 MHz
SLK2501	CDCVF111
TLK1201/TLK2201	CDCV304 up to 140 MHz
TLK1501/TLK2501/TLK2701/TLK3101	CDV304 up to 140 MHz

References

1. *CDC111 1-Line to 9-Line Differential LVPECL Clock Driver* data sheet, Texas Instruments Literature Number SCAS321
2. *CDC Clock Distribution Circuits Data Book*, Texas Instruments Literature Number SCAD004
3. *Raltron - VS8905A-D3-FREQ-CF-EH FIBER OPTICS-VCSO* data sheet, Raltron Electronic Corp, 2001
4. *SLK2501 OC-48/24/12/3 Sonet/SDH Multirate Transceiver* data sheet, Texas Instruments Literature Number SLLS502
5. *SaRonix – Voltage Controlled Oscillator S1566* data sheet, SaRonix, 2001

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