SED1540

CMOS DOT MATRIX LCD CONTROLLER/DRIVER

S-MOS Systems, Inc.

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Version 1.0 (Preliminary)

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1.0 GENERAL DESCRIPTION

1.1 DESCRIPTION

The SED1540 is an LCD driver-controller intended mainly for segment type liquid crystal displays. The device communicates with a host microprocessor through an 8-bit parallel data. The SED1540 stores the data that is sent from the microcomputer in the built-in data display RAM, and generates a liquid drive signal.

The device is manufactured with a low power consumption CMOS process. These features give the designer a flexible means of implementing a small to medium size LCD display for a compact, low power system.

1.2 FEATURES

- Low-power CMOS technology
- Fast CPU 8-bit data interface (80xx, 68xx)
- 1/4 duty cycle
- Built-in LCD driver circuit . . . . . 73 segments
4 commons
- Built-in display data RAM. . . . . 2560 bits
- Rich display command setting
- On-chip CR oscillation circuit
- Master/slave operation is supported
- Recommended expansion driver . . . SED1521(80-segment driver)
- Low power consumption . . . . . 30μW max
- LCD voltage . . . . . 3.5 to 11V
- Single power supply. . . . . 2.4 to 7.0V
- Package . . . . . QFP5-100 pin (FOA)
Al pad (DOA)
Au bump (DOB)

Clock Source	fCL	Frame frequency
External clock	4 kHz	85/64 Hz
Internal oscillation	18 kHz	375/281 Hz

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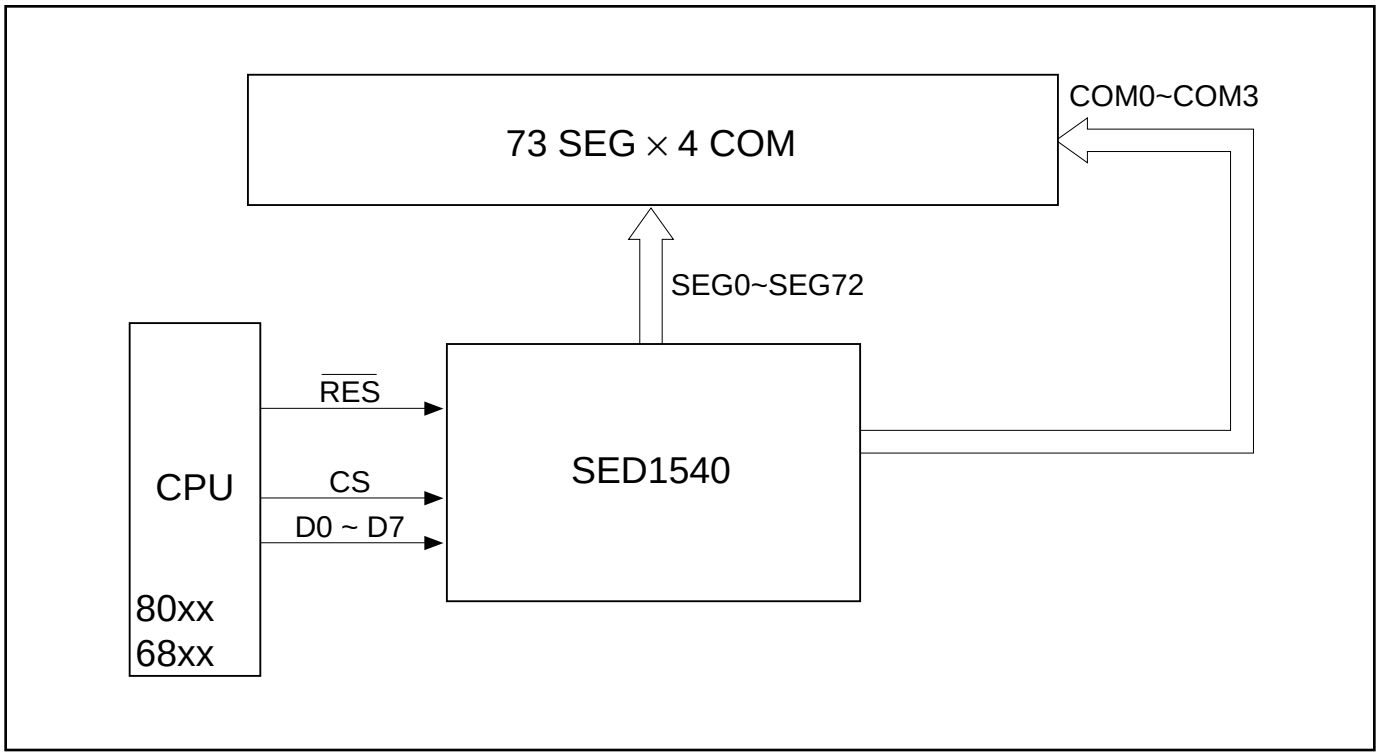
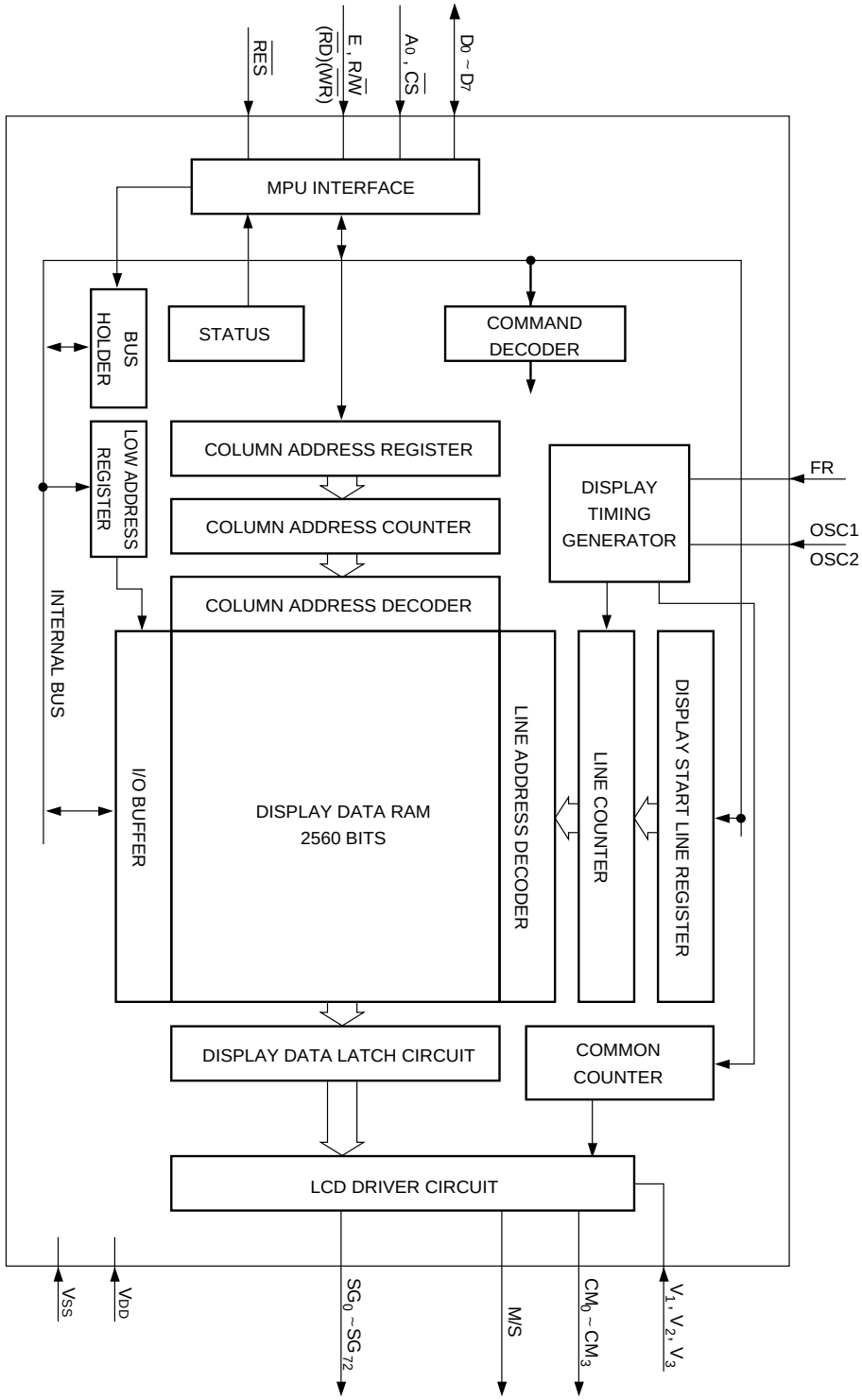
2.0 BLOCK DIAGRAMS

2.1 SYSTEM BLOCK DIAGRAM



2.2 BLOCK DIAGRAM



2.3 DESCRIPTION OF CIRCUIT BLOCKS

2.3.1 MPU Interface

2.3.1.1 Selection of Interface Type

The SED1540 Series uses 8 bits of bi-directional data bus (D_0–D_7) to transfer data. The reset pin is capable of selecting MPU interface; setting the polarity of $\overline{RES}$ to either "H" or "L" can provide direct interface of the SED1540 with a 68 or 80 family MPU (see Table 1 below).

With $\overline{CS}$ at high level, the SED1540 is independent from the MPU bus and stays in standby mode. In this mode, however, the reset signal is input independently of the internal status.

Table 1

Polarity of $\overline{RES}$	Type	A_0	E	R/W	$\overline{CS}$	D0–D7
"L" active	68 MPU	↑	↑	↑	↑	↑
"H" active	80 MPU	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

2.3.1.2 Identification of Data Bus Signals

The SED1540 uses a combination of A0, E, R/W, ($\overline{RD}$, $\overline{WR}$) to identify a data bus signal.

Table 2

Common	68 MPU	80 MPU		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

2.3.1.3 Access to Display Data RAM and Internal Register

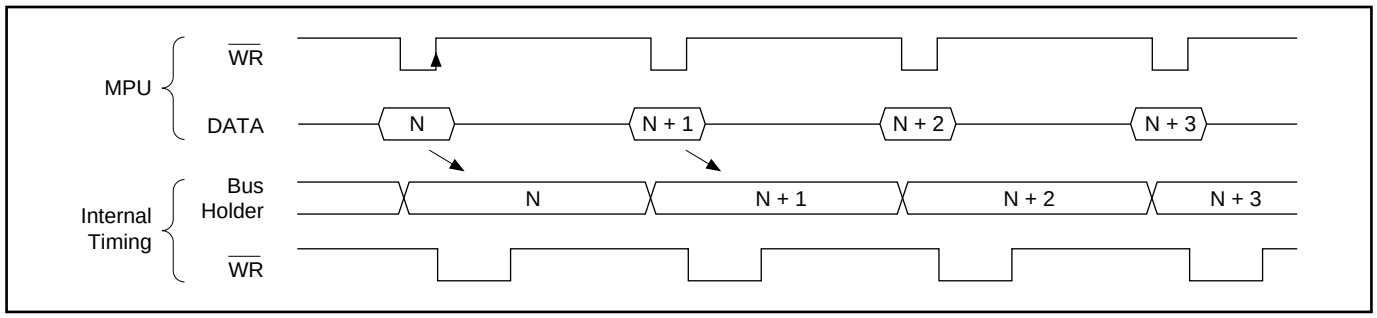
In order to make matching of operating frequencies between the MPU and the display data RAM or internal register, the SED1540 performs a sort of LSI–LSI pipelining via the bus holder attached to the internal data bus.

Consider the case where the MPU reads the content of the display data RAM. In the first data read cycle (dummy), the data is stored on the bus holder. In the next data read cycle, the data is read from the bus holder to the system bus.

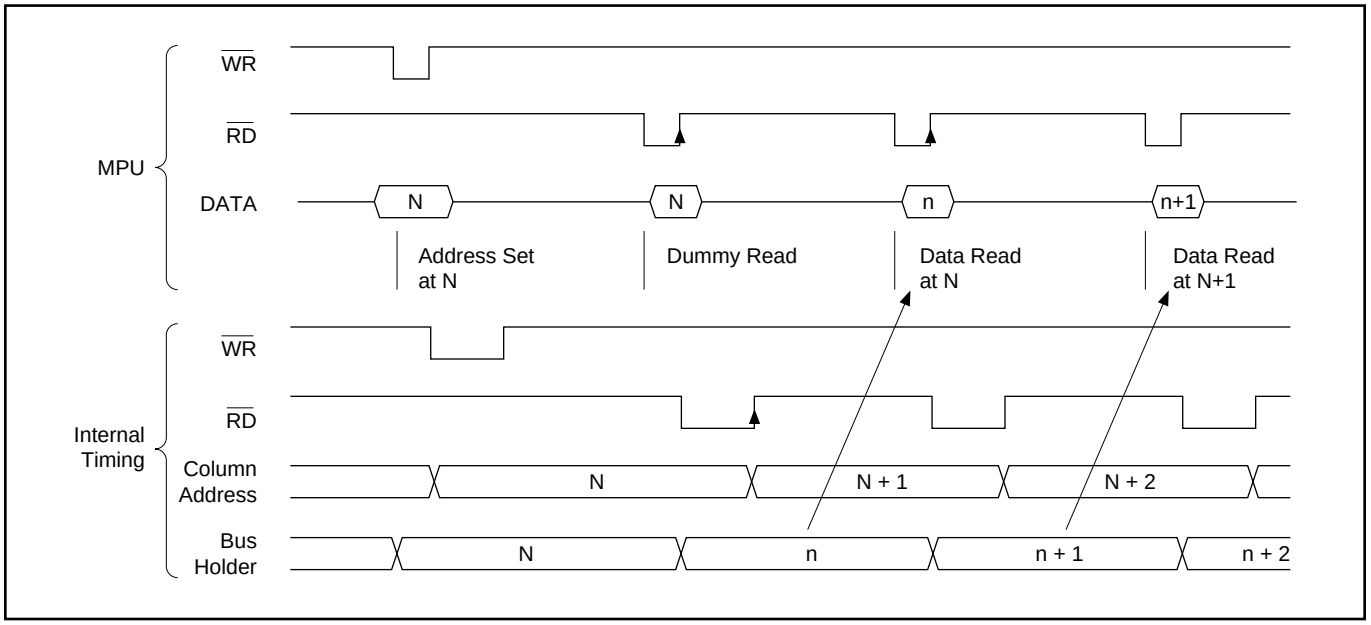
Also, consider the case where the MPU writes data to the display data RAM. In the first data write cycle, the data is held on the bus holder. The data is written to the display data RAM before the next data write cycle begins.

Therefore, MPU's access to the SED1540 is affected not by display data RAM access time (t_{ACC}, t_{DS}) but by cycle time (t_{CYC}). This leads to faster transfer of data to and from the MPU. If the cycle time requirement is not met, the MPU has only to execute the NOP instruction and this is apparently equivalent to execution of a waiting operation. However, there is a restriction on the read sequence of the display data RAM; when an address is set, its data is output not to the first read instruction (immediately following the address setting operation) but to the second read instruction. Thus, one dummy read cycle is necessary after an address set or write cycle. This relation is shown in Figures 2.3.1.4 and 2.3.1.5.

2.3.1.4 Write Timing Diagram



2.3.1.5 Read Timing Diagram



2.3.2 Busy Flag

Busy flag being “1” means that the SED1540 is performing its internal operation and any instruction other than Read Status is disabled. The busy flag is output to pin D7 by a Read Status instruction. As long as the cycle time (t_{CYC}) requirement is met, the flag need not be checked before each command and this dramatically improves the MPU performance.

2.3.3 Display Start Line Register

This register is a pointer which determines the start line corresponding to COM0 (normally, the uppermost line of display) for display of data in the display data RAM. It is used for scrolling the display or changing the page from one to another. Executing the Set Display Start Line command sets 5 bits of display start address in this register. Its content is preset in the line counter at each timing the FR signal changes. The line counter is incremented synchronously to a CL input, thus generating a line address for sequential reading of 80 bits of data from the display data RAM to the LCD driver circuit.

2.3.4 Column Address Counter

The column address counter is a 7–bit presettable counter which gives column addresses of the display data RAM as shown in Fig. 2.3.6.1. When a Read/Write Display Data command comes in, the counter is incremented by 1. For any nonexisting address over 50H, the counter is locked and not incremented.

The column address counter is independent from the page register.

2.3.5 Page Register

This register gives a page address of the display data RAM as shown in Fig. 2.3.6.1. The Set Page Address command permits the MPU to access a new page of the display data RAM.

2.3.6 Display Data RAM

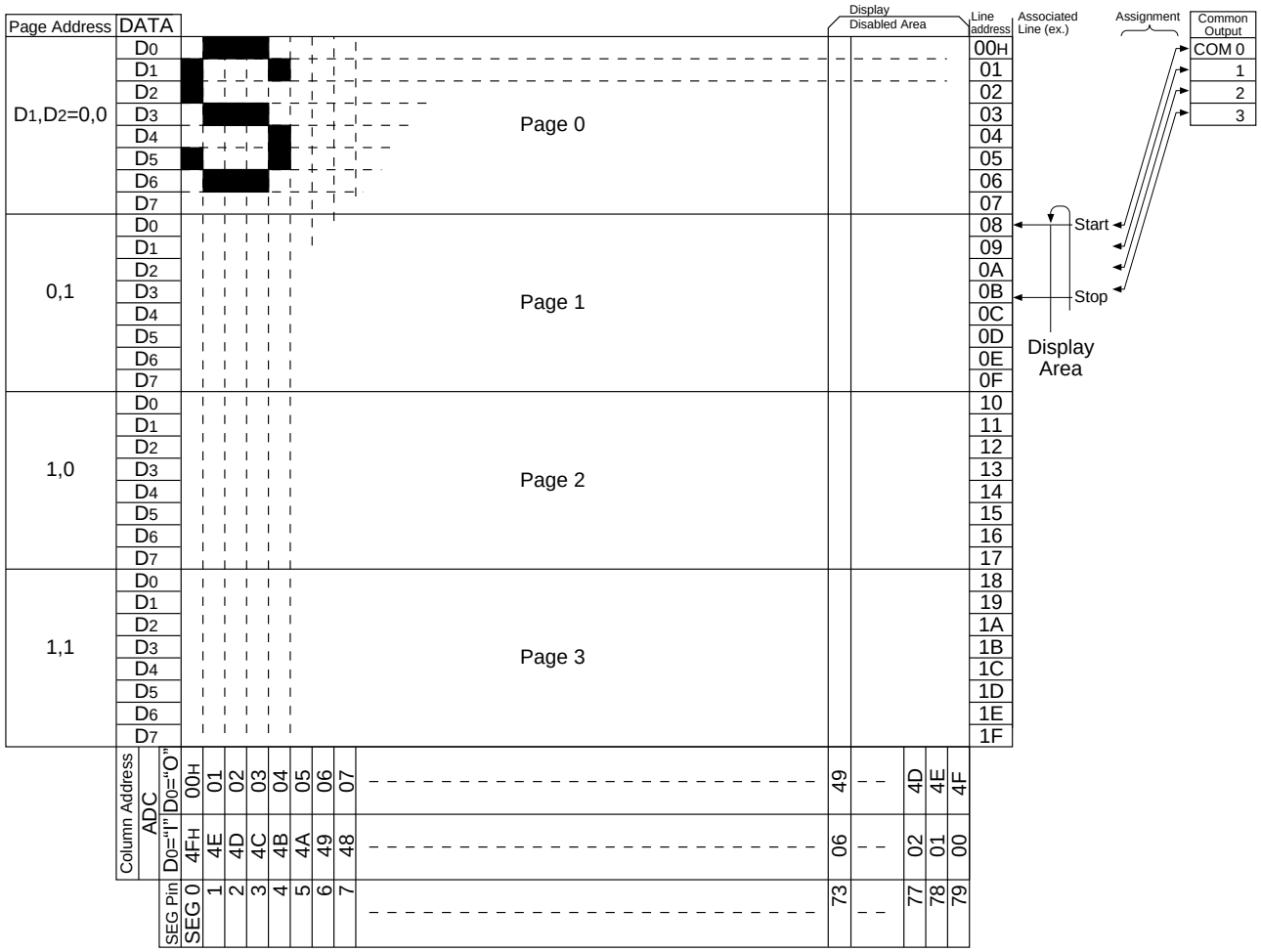
Dot data for display is stored in this RAM. Since the MPU and LCD driver circuit operate independently of each other, data can be changed asynchronously without adverse effect on the display.

One bit of the display data RAM is assigned to one bit of LCD:

LCD on = “1”
LCD off = “0”

The ADC command inverts the assignment relationship between a display data RAM column address and a segment output (see Fig. 2.3.6.1).

2.3.6.1 Relationship Between Display Data RAM Locations and Addresses (Duty = 1/4 and Display Starting Line = 08)



2.3.7 Common Timing Generator

This circuit generates common timing and frame (FR) signals from the basic clock (CL). The Select Duty command selects a duty of 1/3 or 1/4.

2.3.8 Display Data Latch Circuit

The display data latch circuit temporarily stores the data which will be output from the display data RAM to the LCD driver circuit at one-common intervals. The Display ON/OFF and Static Driver ON/OFF commands control the latched data so that the data in the display data RAM remains unchanged.

2.3.9 LCD Driver Circuit

This circuit generates 77 sets of multiplexer that generate quartet levels for LCD driving. Display data in the display data latch, common timing generator output and FR signal are combined to output an LCD driving waveform (Fig. 2.3.12.1).

2.3.10 Display Timing Generator

This circuit generates an internal display timing signal from the basic clock (OSC1) and frame signal (FR).

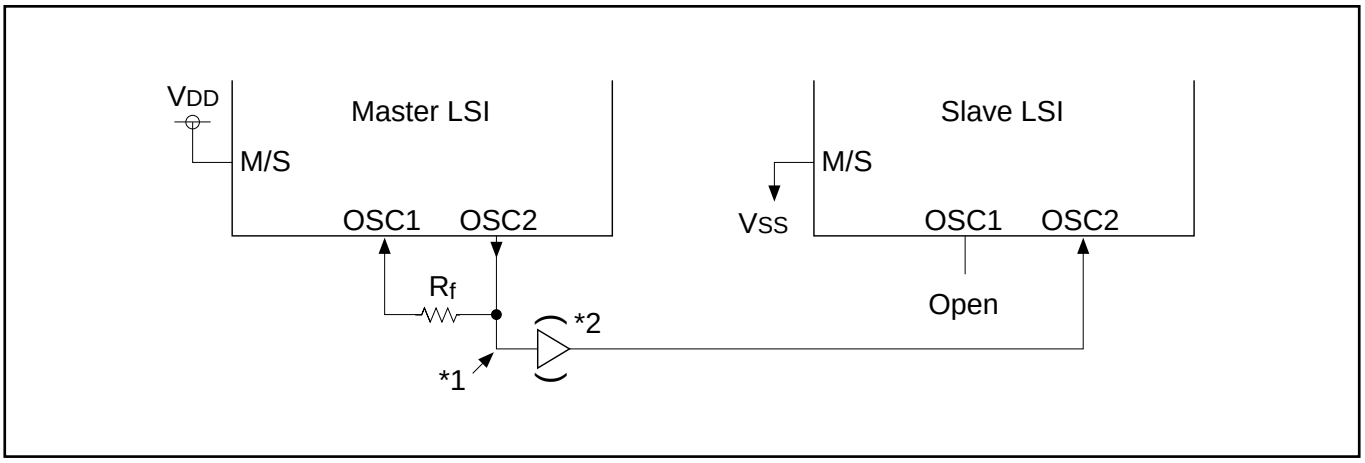
The frame signal FR makes the LCD driver circuit generate a dual frame AC driving waveform (type B) to drive LCD, while making both the line counter and common timing generator synchronized to the FR signal output LSI (dedicated common driver or the SED1540 master LSI). To achieve these functions, the FR signal must be a clock with a duty of 50% which is synchronized to the frame period.

Clock OSC1 is used to operate the line counter. If it is given from outside the LSI, a clock with a duty of 50% is input to OSC1 for the master drive and a clock whose phase is inverted to the clock for the master is input to OSC2 for the slave driver. (Instead, OSC2 for the master driver may be input to OSC2 for the slave driver.)

2.3.11 Oscillation Circuit

This circuit is a low-power CR oscillator which uses an oscillation resistor Rf alone to adjust the oscillation frequency. It generates display timing signals. Fig. 4???? shows the relation between the oscillation resistor and the oscillation frequency that corresponds to the SED1540's frame frequency. When Rf is 1.0MΩ, frame frequency is about 280Hz.

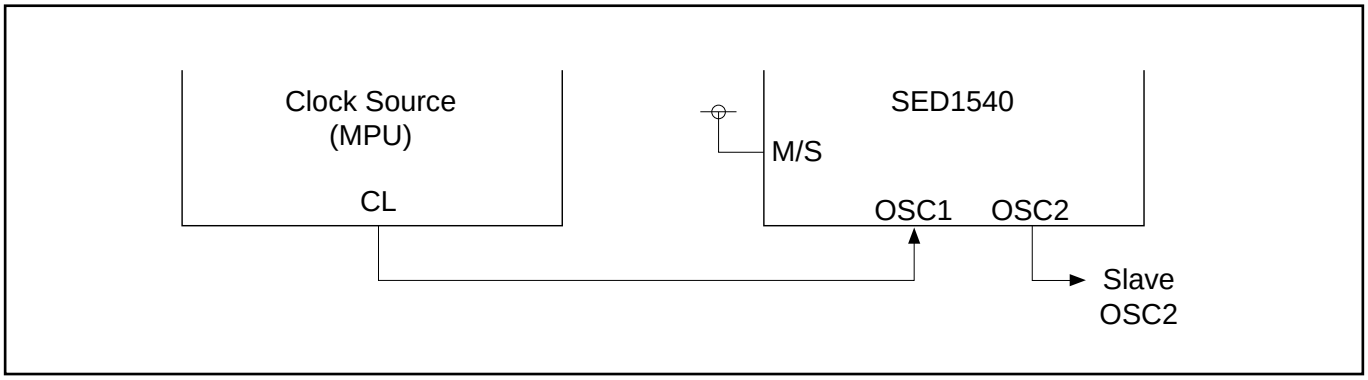
2.3.11.1 LSI Containing Oscillator



* As the parasitic capacitance in this portion increases, the oscillation frequency will shift to a lower level. The Rf must have a smaller value than the specification.

* For a system having two or more slave LSIs, a CMOS buffer is necessary.

2.3.11.2 LSI Operating with External Clock



2.3.12 Reset Circuit

This circuit senses the leading edge or trailing edge of $\overline{RES}$ and initializes the system when its power is switched on.

Initialization:

(a) Display off

(b) Display start line register: First line

(c) Static drive off

(d) Column address counter: Address 0

(e) Page address register: Page 0

(f) Select duty: 1/4

(g) Select ADC: Forward (ADC command D0 = “0”, ADC status flag = “1”)

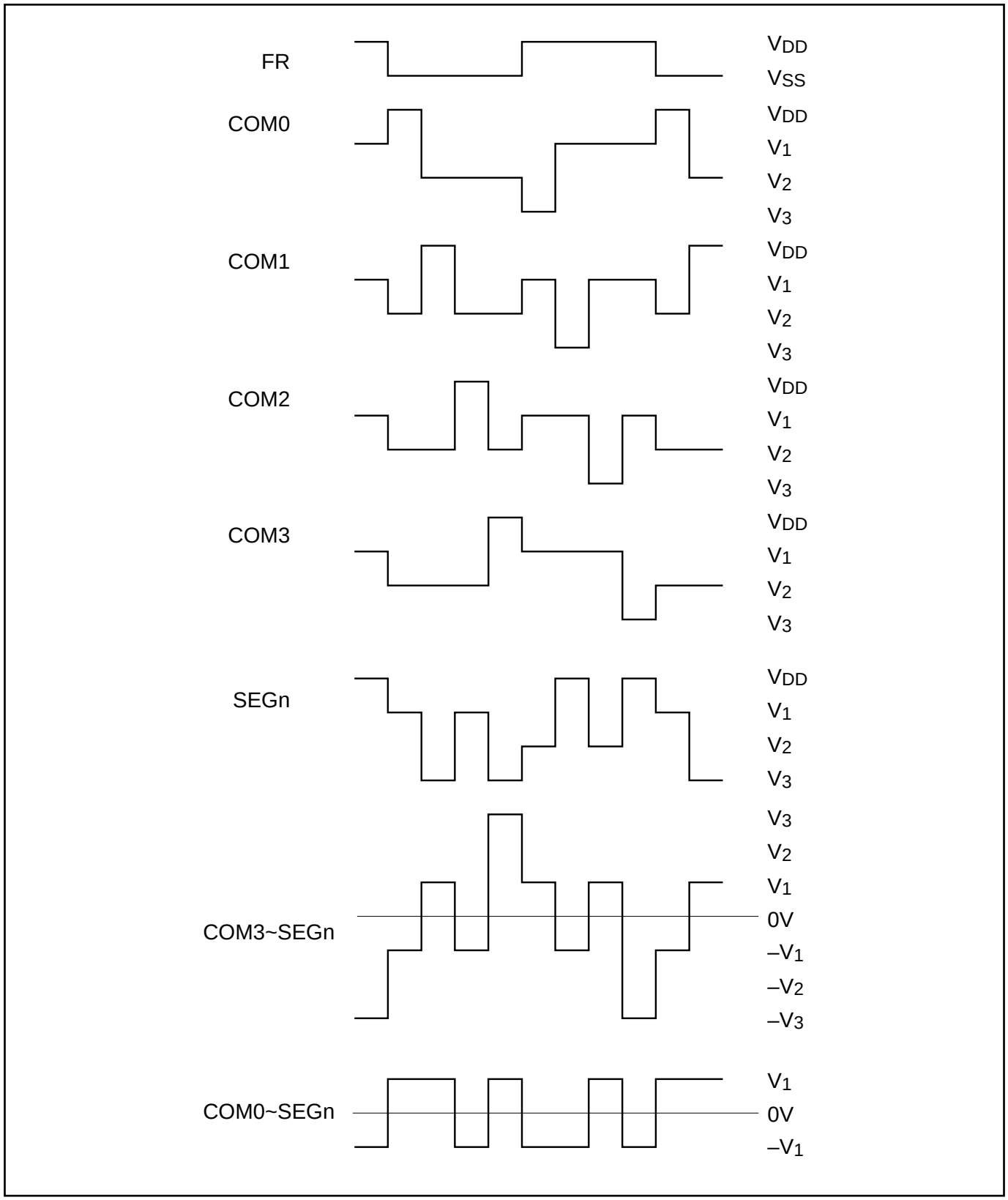
(h) Read modify write off

The input at pin $\overline{RES}$ is level-sensed to select an MPU interface mode as shown in Table 1. For interfacing with an 80 family MPU, an “H” active reset signal is input to pin $\overline{RES}$. For interfacing with a 68 family MPU, an “L” active reset signal is input to the pin. (See Fig.6.)?????

As exemplified in section 6 “MPU Interface”, pin $\overline{RES}$ is connected to the MPU reset pin. Thus the SED1540 and the MPU are initialized at the same time. If system is initialized by pin $\overline{RES}$ at power-on, it may no longer be reset.

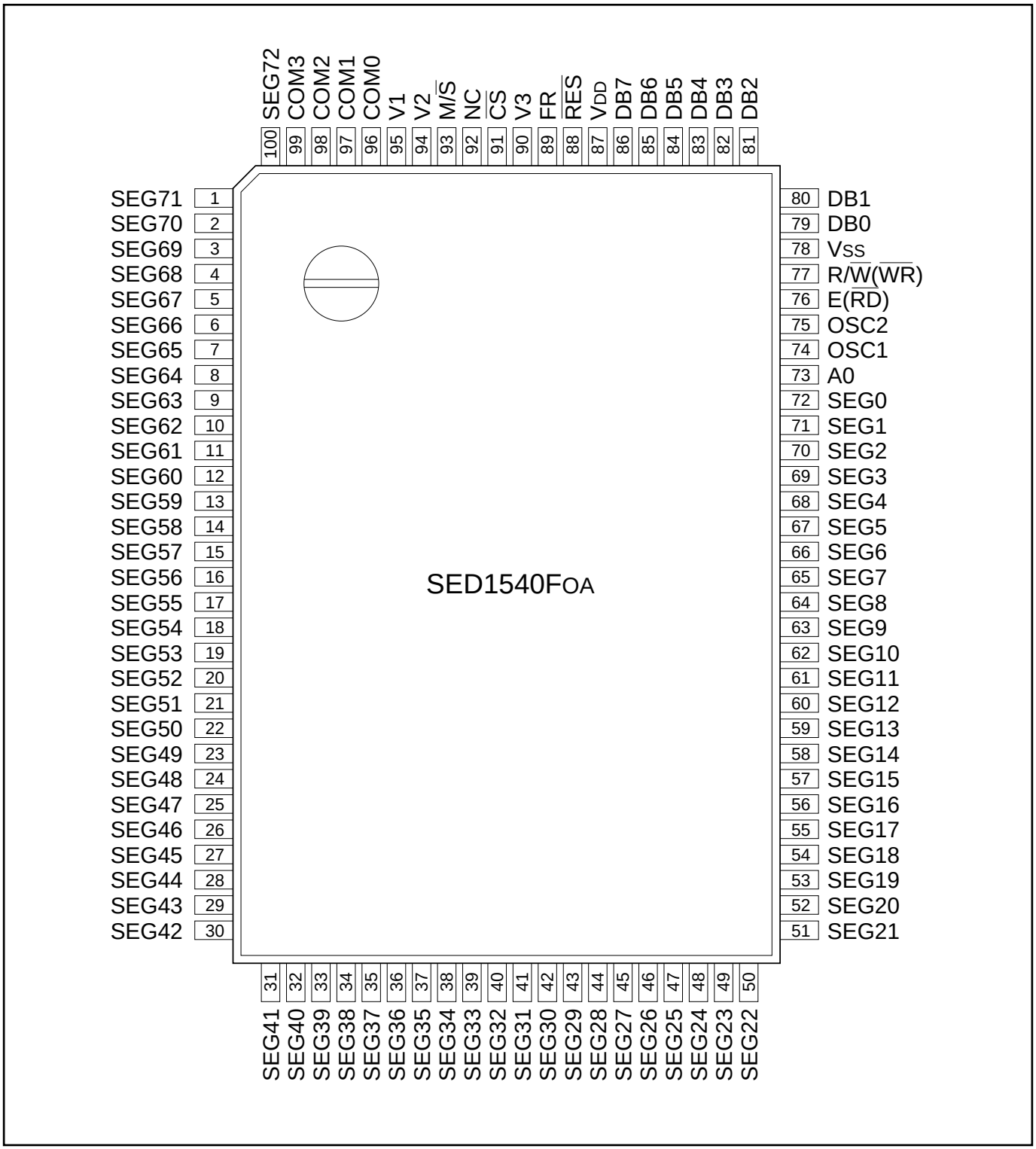
The Reset command causes initialization (b), (d) and (e).

2.3.12.1 Examples of LCD Driving Waveform



3.0 PIN CONFIGURATION

3.1 PIN CONFIGURATION



Number	Name	Number	Name	Number	Name	Number	Name
1	SEG71	26	SEG46	51	SEG21	76	E($\overline{RD}$)
2	SEG70	27	SEG45	52	SEG20	77	R/$\overline{W}$ ($\overline{WR}$)
3	SEG69	28	SEG44	53	SEG19	78	V_{SS}
4	SEG68	29	SEG43	54	SEG18	79	DB0
5	SEG67	30	SEG42	55	SEG17	80	DB1
6	SEG66	31	SEG41	56	SEG16	81	DB2
7	SEG65	32	SEG40	57	SEG15	82	DB3
8	SEG64	33	SEG39	58	SEG14	83	DB4
9	SEG63	34	SEG38	59	SEG13	84	DB5
10	SEG62	35	SEG37	60	SEG12	85	DB6
11	SEG61	36	SEG36	61	SEG11	86	DB7
12	SEG60	37	SEG35	62	SEG10	87	V_{DD}
13	SEG59	38	SEG34	63	SEG9	88	$\overline{RES}$
14	SEG58	39	SEG33	64	SEG8	89	FR
15	SEG57	40	SEG32	65	SEG7	90	V_3
16	SEG56	41	SEG31	66	SEG6	91	$\overline{CS}$
17	SEG55	42	SEG30	67	SEG5	92	NC
18	SEG54	43	SEG29	68	SEG4	93	M/$\overline{S}$
19	SEG53	44	SEG28	69	SEG3	94	V_2
20	SEG52	45	SEG27	70	SEG2	95	V_1
21	SEG51	46	SEG26	71	SEG1	96	COM0
22	SEG50	47	SEG25	72	SEG0	97	COM1
23	SEG49	48	SEG24	73	A_0	98	COM2
24	SEG48	49	SEG23	74	OSC1	99	COM3
25	SEG47	50	SEG22	75	OSC2	100	SEG72

Duty	Pin	
	98	99
1/4	COM2	COM3
1/3	NC	COM2

3.2 PIN DESCRIPTION

3.2.1 Power Signals

V_{DD} Connected to +5V power. Common to MPU power pin V_{CC}.

V_{SS} 0V, connected to system GND.

V_1–V_3 Multi-level power used to drive LCDs. Voltage specified to each LCD cell is divided by resistors or impedance-converted by an operational amplifier before being applied. Each voltage to be applied must be based on V_{DD}, while fulfilling the following conditions:

$$V_{DD} \geq V_1 \geq V_2 \geq V_3$$

3.2.2 System Bus Interface Signals

D_7–D_0 8–bit, tri-state, bi-directional I/O bus. Normally, connected to the data bus of an 8–/16–bit standard microcomputer.

A_0 Input pin. Normally, the LSB of the MPU address bus is connected to this input pin to provide data/command selection.

0: Display control data on D_0–D_7
1: Display data on D_0–D_7

$\overline{RES}$ Input pin. The SED1540 can be reset or initialized by setting $\overline{RES}$ to low level (if it is interfaced with a 68 family MPU) or high level (if with an 80 family MPU). This reset operation occurs when an edge of the $\overline{RES}$ signal is sensed. The level input selects the type of interface with the 68 or 80 family MPU:

High level: Interface with 68 family MPU
Low level: Interface with 80 family MPU

$\overline{CS}$ Chip Select input signal which is normally obtained by decoding an address bus signal. Effective with “L” active and a chip operating with external clocks.

E($\overline{RD}$) Chip interfaced with 68 family MPU:

Enable Clock signal input for the 68 family MPU.

Chip interfaced with 80 family MPU:

“L” active input pin to which the 80 family MPU $\overline{RD}$ signal is connected. With this signal held at “L”, the SED1540 data bus works as output.

R/W ($\overline{WR}$) Chip interface with 68 family MPU:

Read/Write control signal input pin.

R/W = “H” : Read
R/W = “L” : Write

Chip interfaced with 80 family MPU:

“L” active input pin to which the 80 family $\overline{WR}$ is connected. The signal on the data bus is fetched by the leading edge of $\overline{WR}$.

OSC1
OSC2 Connects a resistor for internal oscillation. When M/S = “0”, internal oscillation is disabled and the OSC2 works as an input pin for a clock whose phase is opposite to the clock to the OSC1. With the power-save function active, oscillation or clock input is disabled and the OSC2 turns to high impedance.
(See the description of each block.)

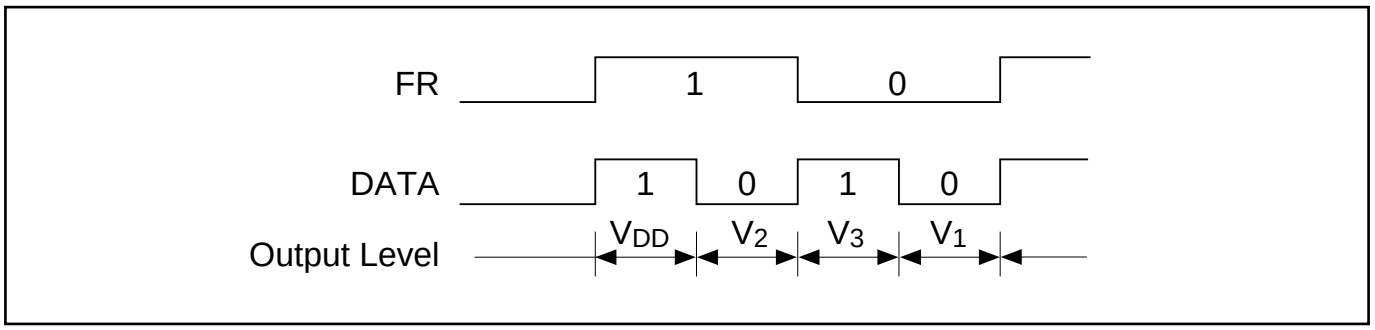
FR LCD AC signal I/O pin.

I/O selection:

M/S = 1: Output
M/S = 0: Input

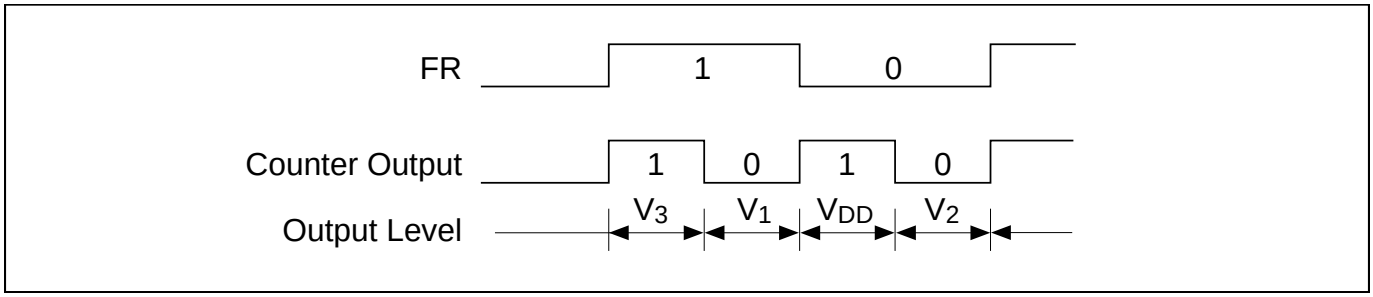
SEG0–
SEG72 LCD segment driving output pins. One of the V_{DD}, V_1, V_2, and V_3 levels is selected by a combination of the content of the display RAM and the FR signal.

3.2.2.1 LCD Segment Driving Output Timing



COM0–COM3 LCD common (row) driving output. (The COM2 and COM3 output state is changed by the Duty Select command. One of the V_{DD}, V_1, V_2, and V_3 levels is selected by a combination of the output of the common counter output and the FR signal.

3.2.2.2 LCD Common (Row) Driving Output



M/S Input signal which selects the master or slave operation for the SED1540. Connected to V_{DD} or V_{SS}. The MS pin changes the I/O state of the FR, OSC1, and OSC2 pins.

M/S = V_{DD}: Master
M/S = V_{SS}: Slave

M/S	FR	OSC1	OSC2	COM output
V_{DD}	Output	Input	Output	Valid
V_{SS}	Input	NC	Input	Valid*

* Using FR to synchronize the master IC with the slave IC provides a COM output of the same waveform for both ICs.

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4.0 COMMANDS

Table 3 lists the commands used with the SED1540. This LSI uses a combination of A_0, R/W ($\overline{RD}$, $\overline{WR}$) to identify a data bus signal. Interpretation and execution of a command depends not on external clock but on internal timing alone. Therefore, a command can be executed so fast that no busy check is needed.

A detailed description of commands follows.

4.1 DISPLAY ON/OFF

This command forces all display to turn on or off.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	1	0	1	0	1	0	1	1	1	D

D 0 = Display OFF
1 = Display ON

4.2 DISPLAY START LINE

This command specifies a line address (shown in Fig. 2.3.6.1) thus marking the display line that corresponds to COM0. Display begins with the specified line address and covers as many lines as match the display duty in address ascending order. Dynamic line address change with the Display Start Line command enables column-wise scrolling or page change.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	1	0	1	1	0	A_4	A_3	A_2	A_1	A_0

– High-order bits

A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0
0	0	0	0	1	1
•	•	•	•	•	•
•	•	•	•	•	•
1	1	1	1	1	31

4.3 SET PAGE ADDRESS

This command is used to specify a page address equivalent to a row address for MPU access to the display data RAM. A required bit of the display data RAM can be accessed by specifying its page address and column address. Changing the page address causes no change in display.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	1	0	1	0	1	1	1	0	A_1	A_0

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

4.4 COLUMN ADDRESS

This command specifies a display data RAM column address. The column address is incremented by 1 each time the MPU accesses from the set address to the display data RAM. Thus, it is possible for the MPU to gain continuous access to only the data. This incrementing stops with address 80; the page address is not continuously changed.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	1	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	0	0	1	1	1	1	79

4.5 READ STATUS

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	0	1	Busy	ADC	ON/ OFF	Reset	0	0	0	0

BUSY: BUSY being “1” means that system is performing an internal operation or is reset. No command is accepted before BUSY = “0”. As long as the cycle time requirement is met, no BUSY check is needed.

ADC: Indicates assignment of column addresses to segment drivers.

0: Inverted (column address 79–n ↔ segment driver n)
1: Forward (column address n ↔ segment driver n)

ON/OFF: Indicates display on or off.

0: Display on
1: Display off

This bit has polarity reverse to the Display ON/OFF command.

RESET: Indicates that system is being initialized by the $\overline{RES}$ signal or the Reset command.

0: Display mode
1: Being reset

4.6 WRITE DISPLAY DATA

This command allows the MPU to write 8 bits of data into the display data RAM. Once the data is written, the column address is automatically incremented by 1; this enables the MPU to write multi-word data continuously.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
1	1	0	Write data							

4.7 READ DISPLAY DATA

This command allows the MPU to read 8 bits of data from the display data RAM location specified by a column address and a page address. Once the data is read, the column address is automatically incremented by 1; this enables the MPU to read multi-word data continuously.

A dummy read is needed immediately after the column address is set. For details, see 3. (1)–(c)??

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
1	0	1	Read data							

4.8 SELECT ADC

This command inverts the relation of assignment between display data RAM column addresses and segment driver outputs. In other words, the Select ADC command can software-invert the order of segment driver output pins, reducing the restrictions on the configuration of ICs at LCD module assembly. For details, see Fig. 2.3.6.1.

Incrementing the column address by 1, which takes place after the MPU writing or reading display data, follows the sequence of column addresses specified in Fig. 2.3.6.1.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	1	0	1	0	1	0	0	0	0	D

D = 0: Clockwise output (forward)
D = 1: Counterclockwise output (reverse)

4.9 STATIC DRIVE ON/OFF

This command forces all display to be on and, at the same time, all common output to be selected.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	1	0	1	0	1	0	0	1	0	D

D = 0: Static drive off
D = 1: Static drive on

4.10 SELECT DUTY

This command is used to select the duty (degree of multiplexity) of LCD driving.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	1	0	1	0	1	0	1	0	0	D

D = 0: Duty 1/3
D = 1: Duty 1/4

4.11 READ MODIFY WRITE

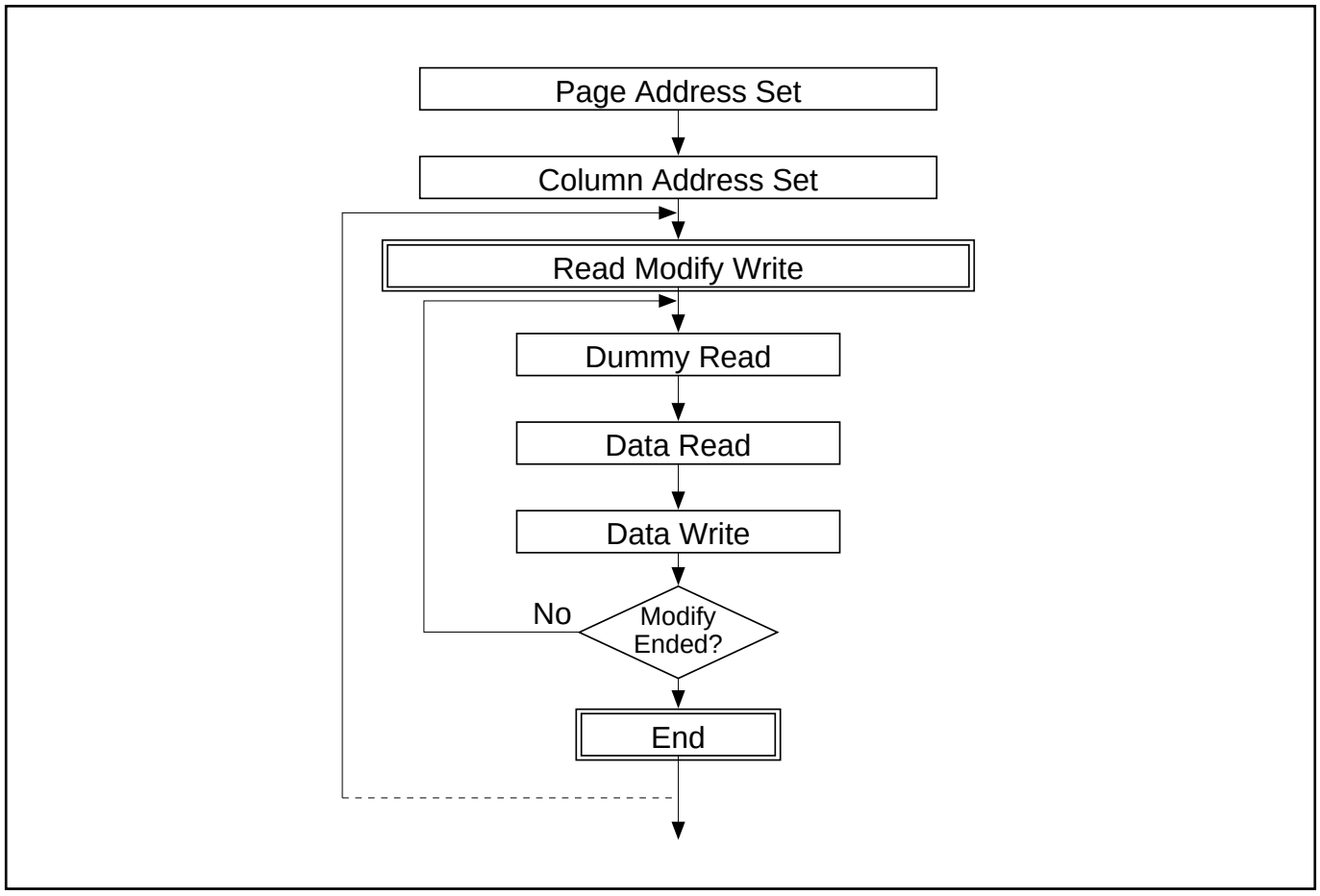
This command is used with the End command in a pair. Once it has been entered, the column address will be incremented not by the Read Display Data command but by the Write Display Data command only. This mode will stay until the End command is entered.

Entry of the End command causes the column address to return to the address which was valid when the Read Modify Write command was entered. This function lessens the load of the MPU when the data in a specific display area are repeatedly updated (as blinking cursor).

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	1	0	1	1	1	0	0	0	0	0

Even in the Read Modify Write mode, any command other than Read/Write Data and Set Column Address may be used.

4.11.1 Cursor Blinking Sequence

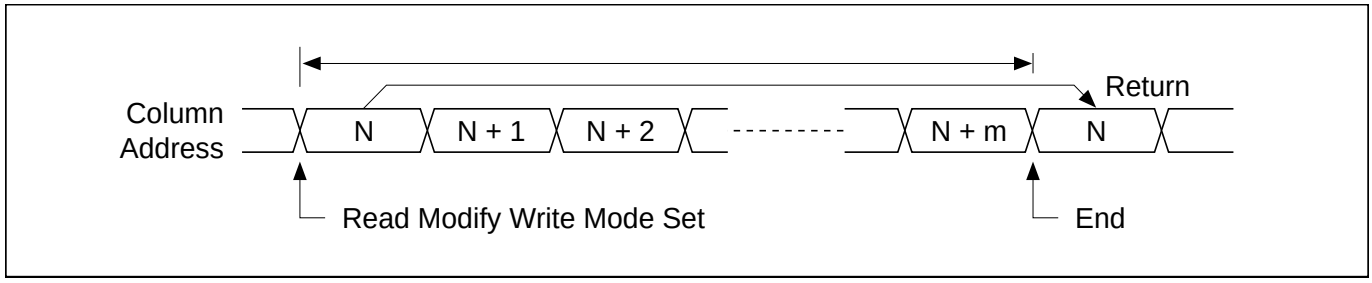


4.12 END

This command cancels the Read Modify Write command, returning the column address to the initial mode address.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	1	0	1	1	1	0	1	1	1	0

4.12.1 End Timing



4.13 RESET

This command initializes the display start line register, column address counter, and page address counter without any effect on the display data RAM. For details, see section 2.3.12.

The reset operation follows entry of the Reset command.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7							D0
0	1	0	1	1	1	0	0	0	1	0

Initialization at power-on is performed not by the Reset command but by a reset signal applied to the $\overline{RES}$ pin.

4.14 SAVE POWER (COMBINED COMMAND)

Static drive going on with display off invokes power-saving mode, reducing current consumption to nearly static current level. During this mode, the SED1540 holds the following conditions:

(a) It stops driving the LCD; the segment and common driver outputs are at V_{DD} level.

(b) Oscillation and external clock input are disabled; OSC2 is in floating condition.

(c) The display data and operational mode are held.

The power-saving mode is cancelled by display on or static drive off.

If an external resistor division circuit is used to give LCD driving voltage level, the current flowing into the resistors must be cut off by the power-save signal.

4.14.1 External Resistor Division Circuit

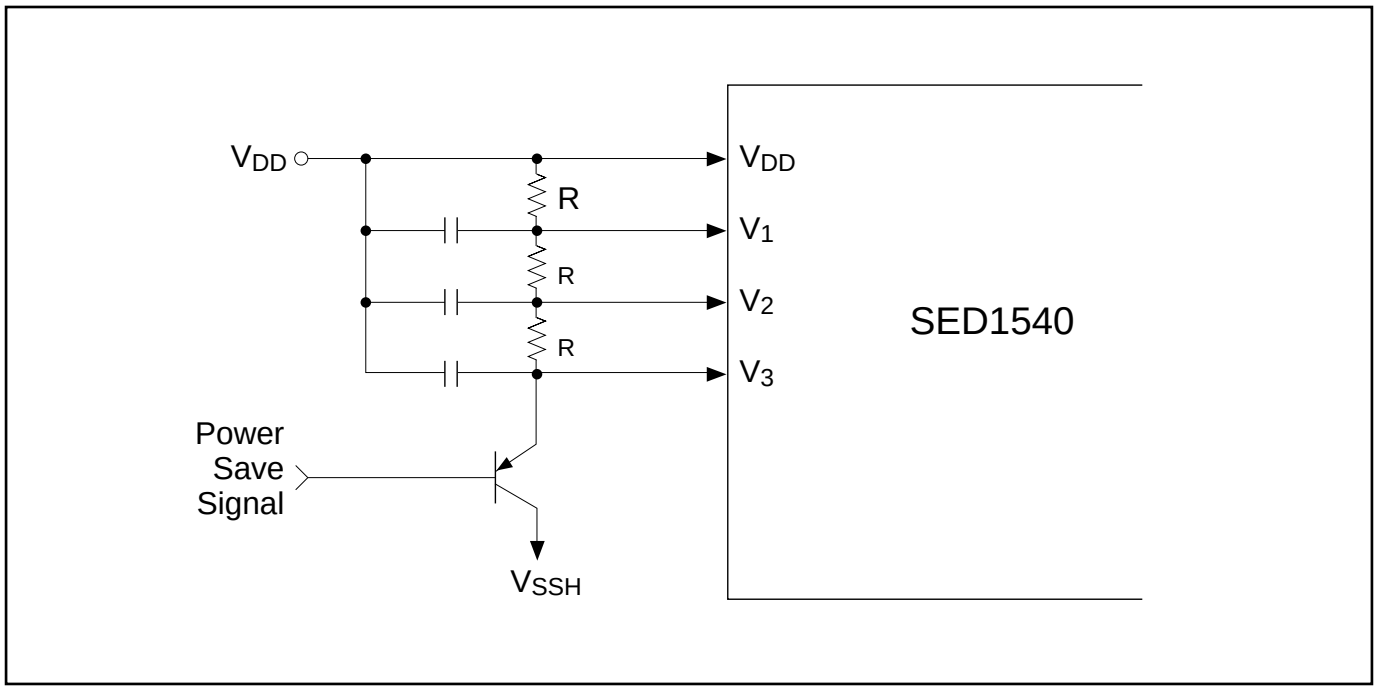


Table 3 Commands

	Command	Code											Function	
		A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns all display on or off, independently of display RAM data or internal status. 1: ON 0: OFF (Power-saving mode with static drive on)*	
(2)	Display start line	0	1	0	1	1	0	Display Start Address (0–31)					Specifies RAM line corresponding to uppermost line (COM0) of display.	
(3)	Set page address	0	1	0	1	0	1	1	1	0	Page (0–3)		Sets display RAM page in page address register.	
(4)	Set column (segment) address	0	1	0	0	Column Address (0–72)							Sets display RAM column address in column address register.	
(5)	Read status	0	0	1	Busy	ADC	ON/OFF	RESET	0	0	0	0	Reads the following status: BUSY 1: Internal operation, 0: Ready ADC 1: CW output (forward), 0: CCW output (reverse) ON/OFF 1: Display off, 0: Display on RESET 1: Being reset, 0: Normal	
(6)	Write display data	1	1	0	Write Data								Writes data from data bus into display RAM.	Display RAM location whose address has been preset is accessed. After access, the column address is incremented by 1.
(7)	Read display data	1	0	1	Read Data								Reads data from display RAM onto data bus.	
(8)	Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	Used to invert relationship of assignment between display RAM column addresses and segment driver outputs. 0: CW output (forward) 1: CCW output (reverse)	
(9)	Static drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects normal display or static driving operation. 1: Static drive (power-saving mode) 0: Normal driving	
(10)	Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD cell driving duty. 1: 1/4 0: 1/3	
(11)	Read modify write	0	1	0	1	1	1	0	0	0	0	0	Increments column address counter by 1 when display data is written. (This is not done when data is read.)	
(12)	End	0	1	0	1	1	1	0	1	1	1	0	Clears read modify write mode.	
(13)	Reset	0	1	0	1	1	1	0	0	0	1	0	Sets display start line register on the first line. Also sets column address counter and page address counter to 0.	

* With display off (command (1)), static drive going on (9) invokes power-saving mode.

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5.0 ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Standard	Unit
Supply voltage (1)		V_{SS}	–8.0 ~ +0.3	V
Supply voltage (2)		V_3	–15.0 ~ + 0.3	V
Supply voltage (3)		V_1, V_2,V_3	V_3 ~ + 0.3	V
Input voltage		V_{IN}	V_{SS} – 0.3 ~ + 0.3	V
Output voltage		V_O	V_{SS} – 0.3 ~ + 0.3	V
Power dissipation		P_D	250	mW
Operating temperature		T_{OPR}	–30 ~ +85	°C
Storage temperature	FP	T_{STG}	–65 ~ +150	°C
	Bare chip		–55 ~ +125	
Soldering temperature/time		T_{SOLDER}	260/10 (at leads)	°C/Sec

Notes:

1. All voltages are based on V_{DD} = 0V.
2. The following condition must always hold true with voltages V_1, V_2 and V_3:
   $V_{DD} \geq V_1 \geq V_2 \geq V_3$.
3. The LSI may be permanently damaged if used with any value in excess of the absolute maximum ratings. During normal operation, the LSI should preferably be used within the specified electrical characteristics. Failure to meet them can cause the LSI to malfunction or lose its reliability.
4. Generally, flat package LSIs may have moisture resistance lowered when solder dipped. In mounting LSIs on a board, it is recommended to use a method which is least unlikely to give thermal stress on the package resin.

5.2 DC CHARACTERISTICS

V_{DD} = 0V, Ta = –20 ~ 75°C

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pin
Operating voltage (1)*1	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0		–2.4		
Operating voltage (2)	Recommended	V_3			–11.0		–3.5	V	V_3 *10
	Allowable				–11.0				
	Allowable	V_1			0.6 × V_3		V_{DD}	V	V_1
	Allowable	V_2			V_3		0.4 × V_3	V	V_2
High level input voltage		V_{IHT}			V_{SS} + 2.0		V_{DD}	V	*2 *3
		V_{IHC}			0.2 × V_{SS}		V_{DD}		
Low level input voltage		V_{ILT}			V_{SS}		V_{SS} + 0.8	V	*2 *3
		V_{ILC}			V_{SS}		0.8 × V_{SS}		
High level output voltage		V_{OHT}	I_{OH} = –3.0mA		V_{SS} + 2.4			V	*4
		V_{OHC1}	I_{OH} = –2.0mA		V_{SS} + 2.4				*5
		V_{OHC2}	I_{OH} = –120µA		0.2 × V_{SS}				OSC2
Low level output voltage		V_{OLT}	I_{OL} = 3.0mA				V_{SS} + 0.4	V	*4
		V_{OLC1}	I_{OL} = 2.0mA				V_{SS} + 0.4		*5
		V_{OLC2}	I_{OL} = 120µA				0.8 × V_{SS}		OSC2
Input leakage current		I_{LI}			–1.0		1.0	µA	*6
Output leakage current		I_{LO}			–3.0		3.0	µA	*7
LCD driver ON resistor		R_{ON}	Ta = 25°C	V_3 = –5.0V		5.0	7.5	KΩ	SEG 0 ~ 72 *11 COM 0 ~ 3
				V_3 = –3.5V		10.0	50.0		
Static current dissipation		I_{DDQ}	$\overline{CS}$ = CL = V_{DD}			0.05	1.0	µA	V_{DD}
Dynamic current dissipation		I_{DD} (1)	During display V_3 = –5.0V	f_{OSC} = 4KHz		1.5	4.0	µA	V_{DD}
				R_f = 1MΩ		9.5	15.0		
		I_{DD} (2)	During access t_{CYC} = 200KHz			300	500		*8
Input pin capacitance		C_{IN}	Ta = 25°C f = 1MHz			5.0	8.0	pF	All input pins

(Continued) V_{DD} = 0V, Ta = –20 ~ 75°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Oscillation frequency	f_{OSC}	Rf = 1.0MΩ ± 2% V_{SS} = –5.0V	15	18	21	KHz	*9
		Rf = 1.0MΩ ± 2% V_{SS} = –3.0V	11	16	21		
Reset time	t_R		1.0		1000	µs	$\overline{RES}$

Notes:

*1. Operation over a wide range of voltages is guaranteed except where a sudden voltage change occurs during access.

*2. Pins A_0, D_0–D_7, E($\overline{RD}$), R/W ($\overline{WR}$) and $\overline{CS}$

*3. Pins CL, FR, M/S and $\overline{RES}$

*4. Pins D_0–D_7

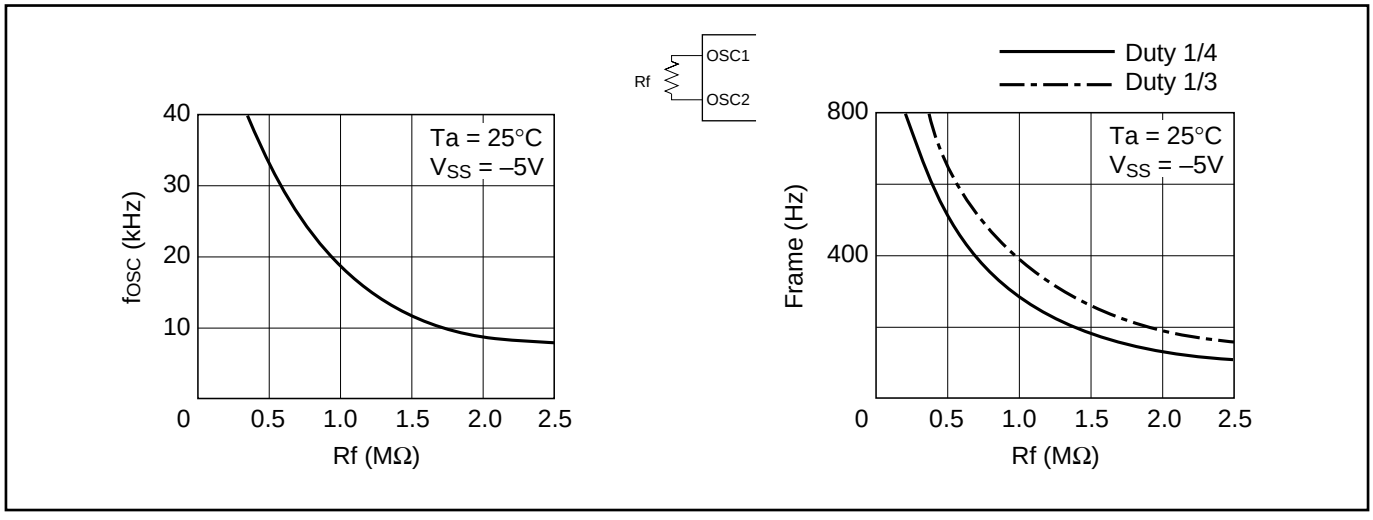
*5. Pin FR

*6. Pins A_0, E ($\overline{RD}$), R/W ($\overline{WR}$), $\overline{CS}$, CL and $\overline{RES}$

*7. Applicable when pins D_0–D_7 and FR are at high impedance.

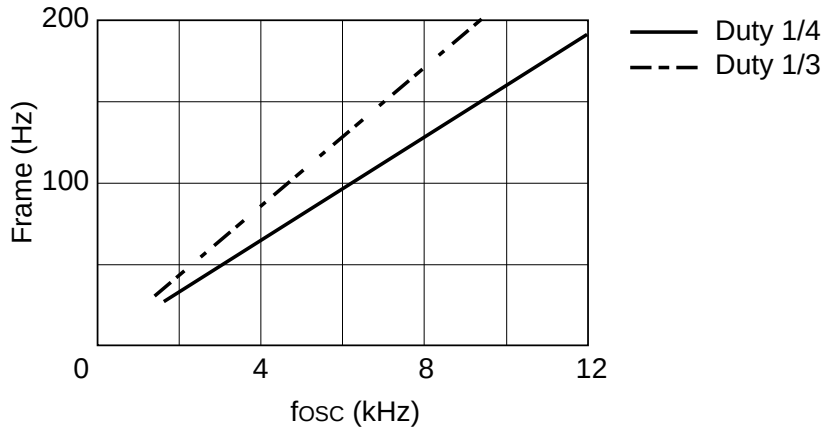
*8. This value is current consumption when a vertical stripe pattern is written at t_{CYC}.

*9. Relationship between oscillation frequency, frame and Rf (SED1540)

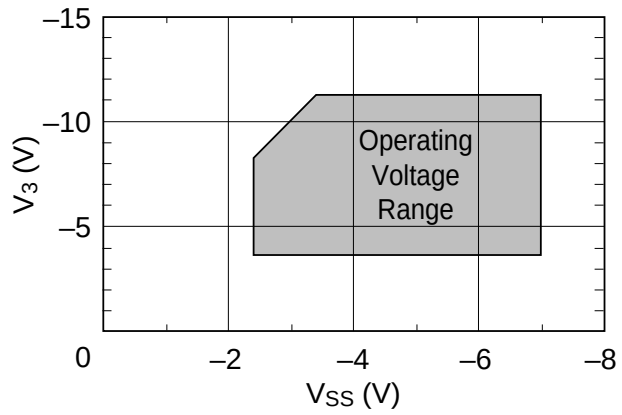


Notes (continued):

Relationship between external clock (fCL) and frame (SED1540)



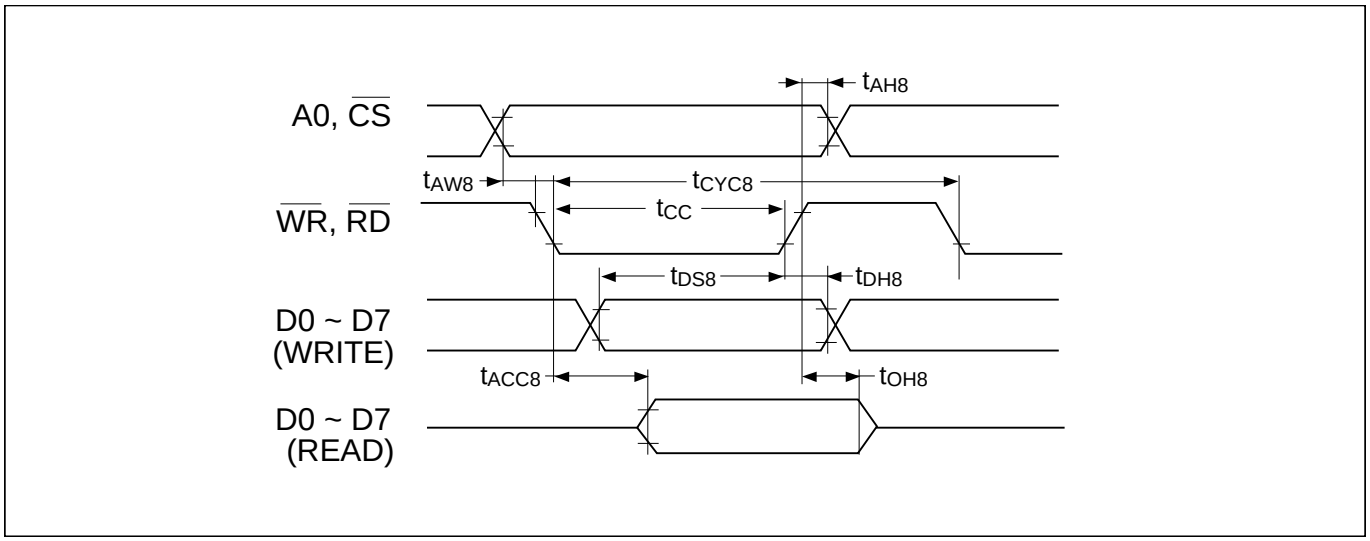
*10.Operating voltage ranges of V_{SS} and V_3



*11.Resistance with a voltage of 0.1V applied between the output pin (SEG, COM) and each power pin (V_1, V_2). It is specified within the operating voltage (2) range.

5.3 TIMING CHARACTERISTICS

5.3.1 System Bus Read/Write I (80 Family MPU)



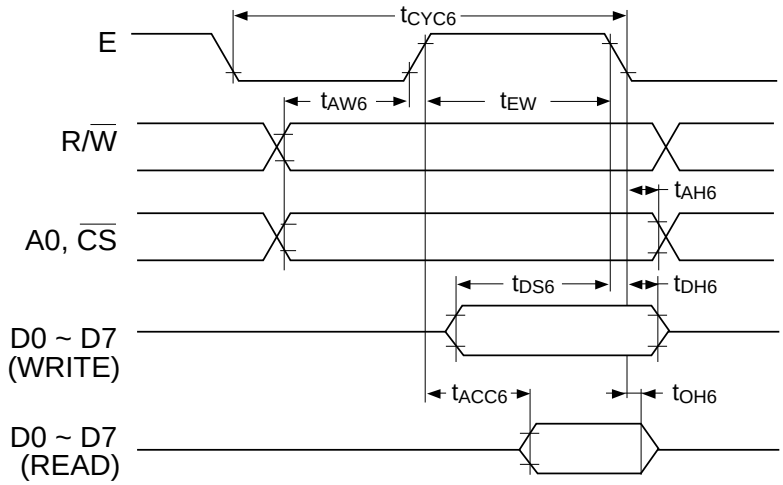
Ta = –20 to 75°C, V_{SS} = –5.0V ± 10%, Unit: ns

Signal	Symbol	Parameter	Min.	Max.	Condition
A_0, $\overline{CS}$	t_{AH8}	Address hold time	10		
	t_{AW8}	Address setup time	20		
$\overline{WR}$, $\overline{RD}$	t_{CYC8}	System cycle time	1000		
	t_{CC}	Control pulse width	200		
D_0–D_7	t_{DS8}	Data setup time	80		
	t_{DH8}	Data hold time	10		
	t_{ACC8}	$\overline{RD}$ access time		90	CL = 100pF
	t_{OH8}	Output disable time	10	60	

*1. Each of the values where V_{SS} = –3.0V is about 200% of that where V_{SS} = –5.0V (i.e., the listed value).

*2. The rise or fall time of input signals should be less than 15 ns.

5.3.2 System Bus Read/Write II (68 Family MPU)



Ta = –20 to 75°C, V_{SS} = –5.0V ± 10%, Unit: ns

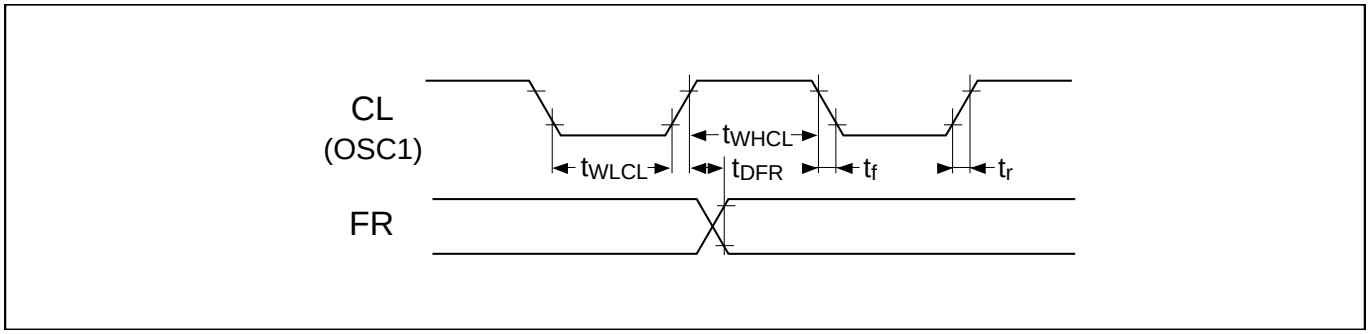
Signal	Symbol	Parameter		Min.	Max.	Condition
A0, CS R/W	tCYC6*1	System cycle time		1000		
	tAW6	Address setup time		20		
	tAH6	Address hold time		10		
D0–D7	tDS6	Data setup time		80		
	tDH6	Data hold time		10		
	tOH6	Output disable time		10	60	CL = 100pF
	tACC6	Access time			90	
E	tEW	Enable pulse width	Read	100		
			Write	80		

*1. t_{CYC6} indicates the cycle time during which CS E = “H”. It does not mean the cycle time of signal E.

*2. Each of the values where V_{SS} = –3.0V is about 200% of that where V_{SS} = –5.0V (i.e., the listed value).

*3. The rise or fall time of input signals should be less than 15 ns.

5.3.3 Display Control Timing



5.3.3.1 Input Timing

Ta = –20 to 75°C, V_{SS} = –5.0V ± 10%
Unit: µs (t_{WLCL}, t_{WHCL}, t_{DFR}), ns (tr, tf)

Signal	Symbol	Parameter	Min.	Typ.	Max.	Condition
CL	t_{WLCL}	Low level pulse width	35			
	t_{WHCL}	High level pulse width	35			
	t_r	Rise time		30	150	
	t_f	Fall time		30	150	
FR	t_{DFR}	FR delay time	–2.0	0.2	2.0	

5.3.3.2 Output Timing

Ta = –20 to 75°C, V_{SS} = –5.0V ± 10%, Unit: µs

Signal	Symbol	Parameter	Min.	Typ.	Max.	Condition
FR	t_{DFR}	FR delay time		0.2	0.4	CL = 100pF

*1. The listed FR input delay time applies to the SED1540 (slave).
The listed FR output delay time applies to the SED1540 (master).

*2. Each of the values where V_{SS} = –3.0V is about 200% of that where V_{SS} = –5.0V (i.e., the listed value).

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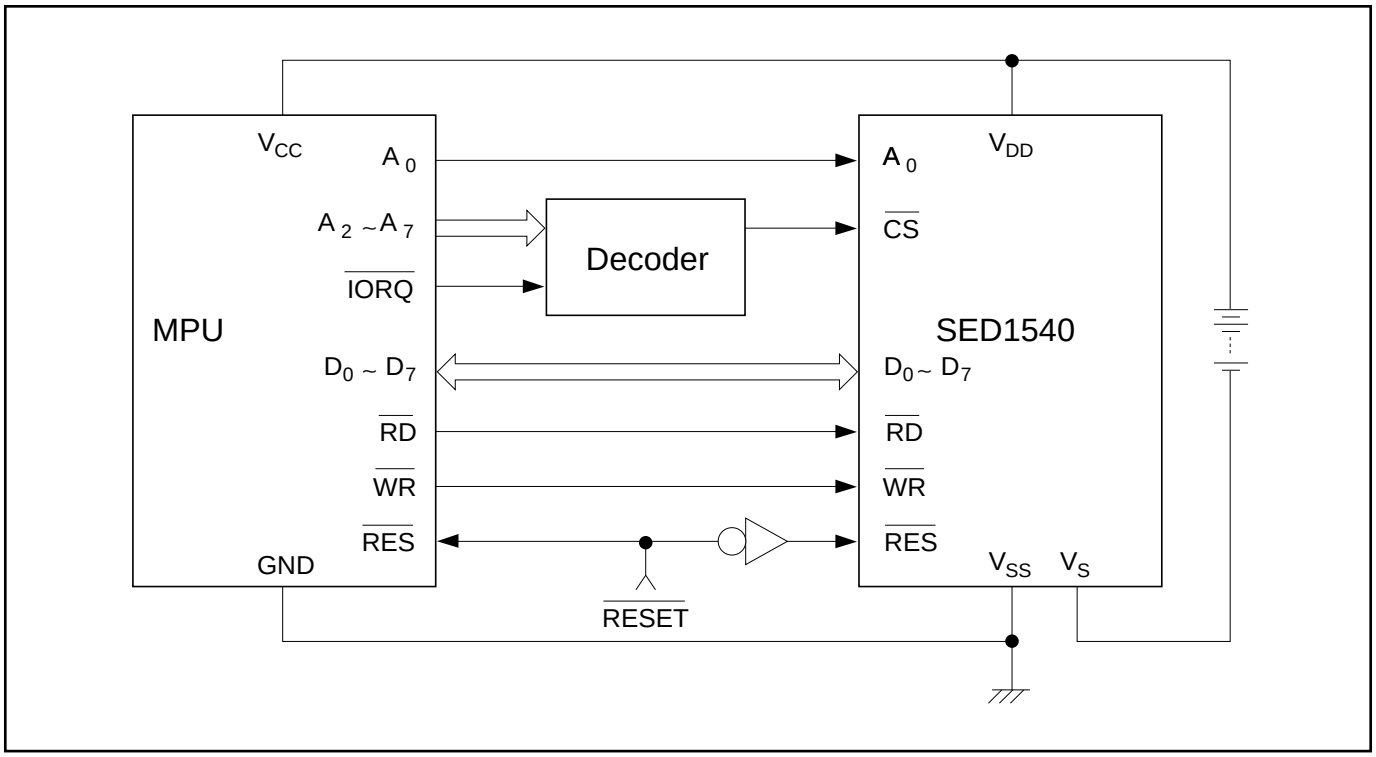
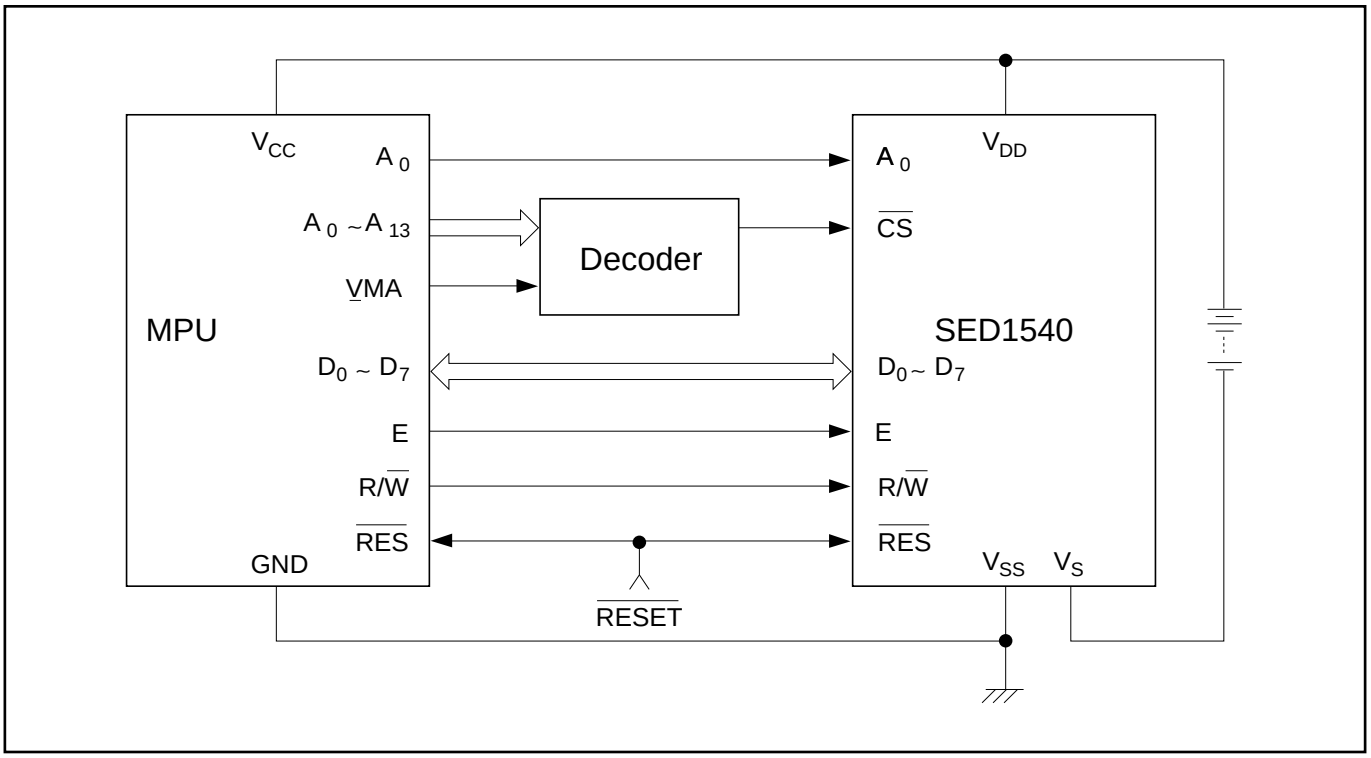
6.0 MPU INTERFACE

6.1 80 FAMILY MPU

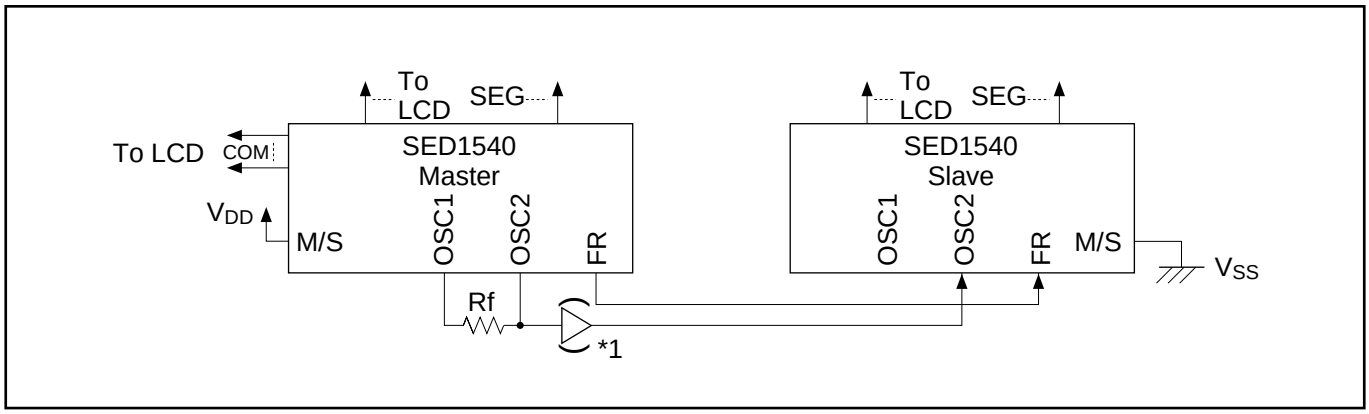


6.2 68 FAMILY MPU

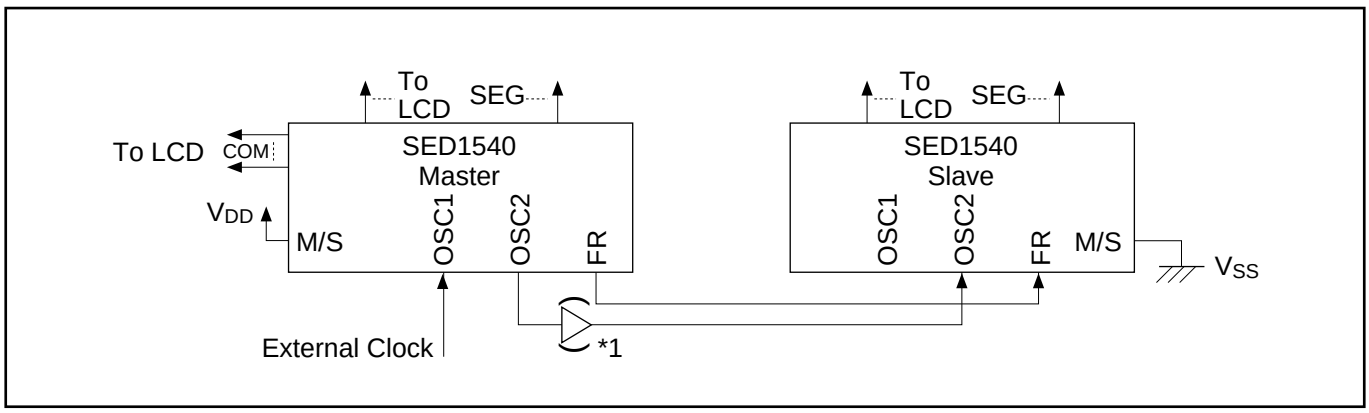


7.0 LCD DRIVER INTERCONNECTIONS

7.1 SED1540 - SED1540 (INTERNAL OSCILLATION)



7.2 SED1540 - SED1540 (EXTERNAL CLOCK OPERATION)



*1. For connection to more than one slave LSI, a CMOS buffer must be used.

*2. For use as the master slave, the same duty must be set.

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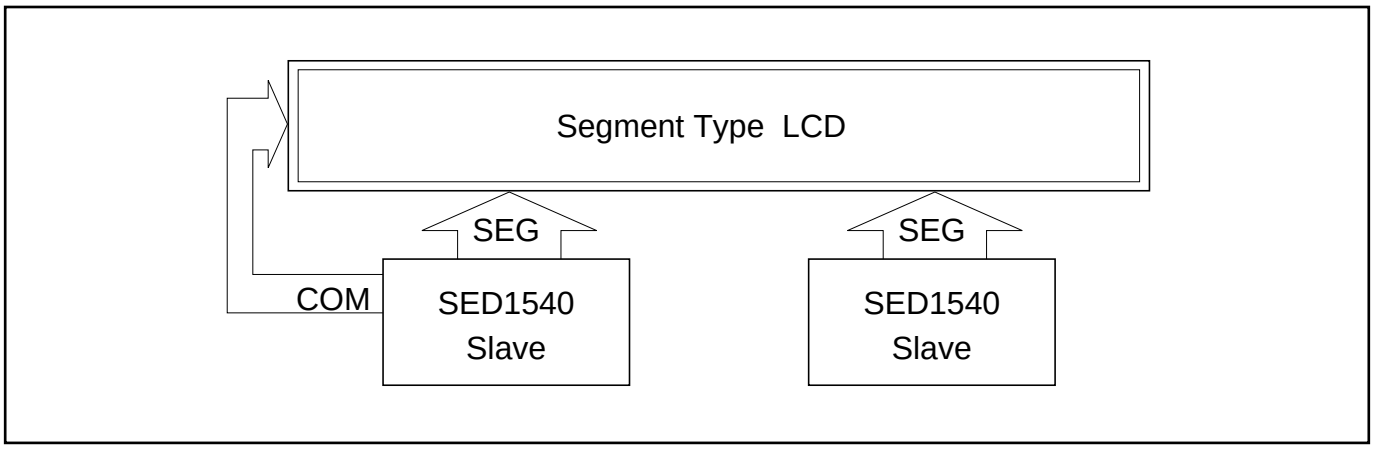
8.0 TYPICAL CONNECTIONS WITH LCD PANEL

8.1 TYPICAL CONNECTIONS WITH LCD PANEL



The slave IC may be omitted in this conneciton. The panel can be driven with the master IC alone.

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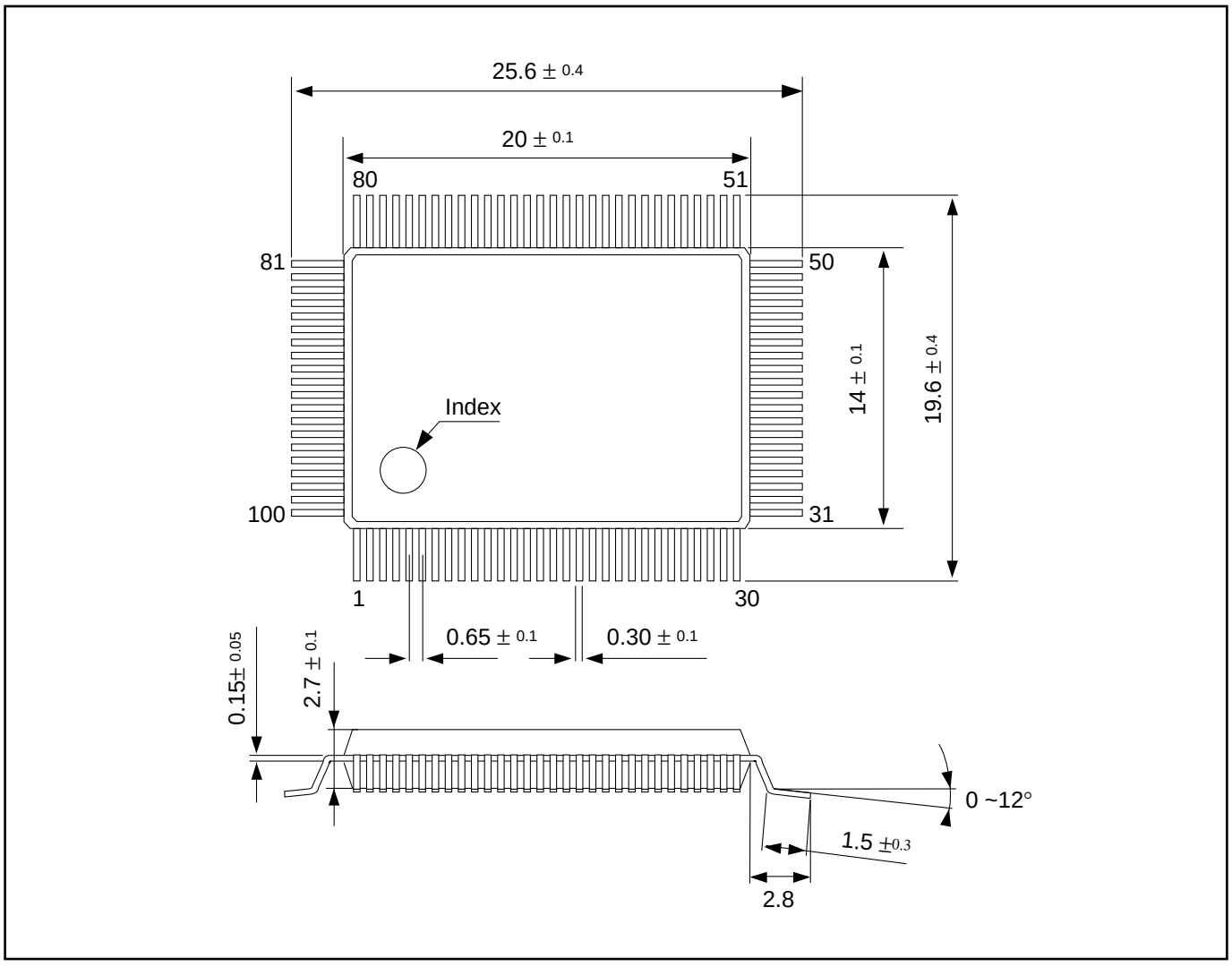
9.0 PACKAGE DIMENSIONS

9.1 PLASTIC QFP 5-100 PIN



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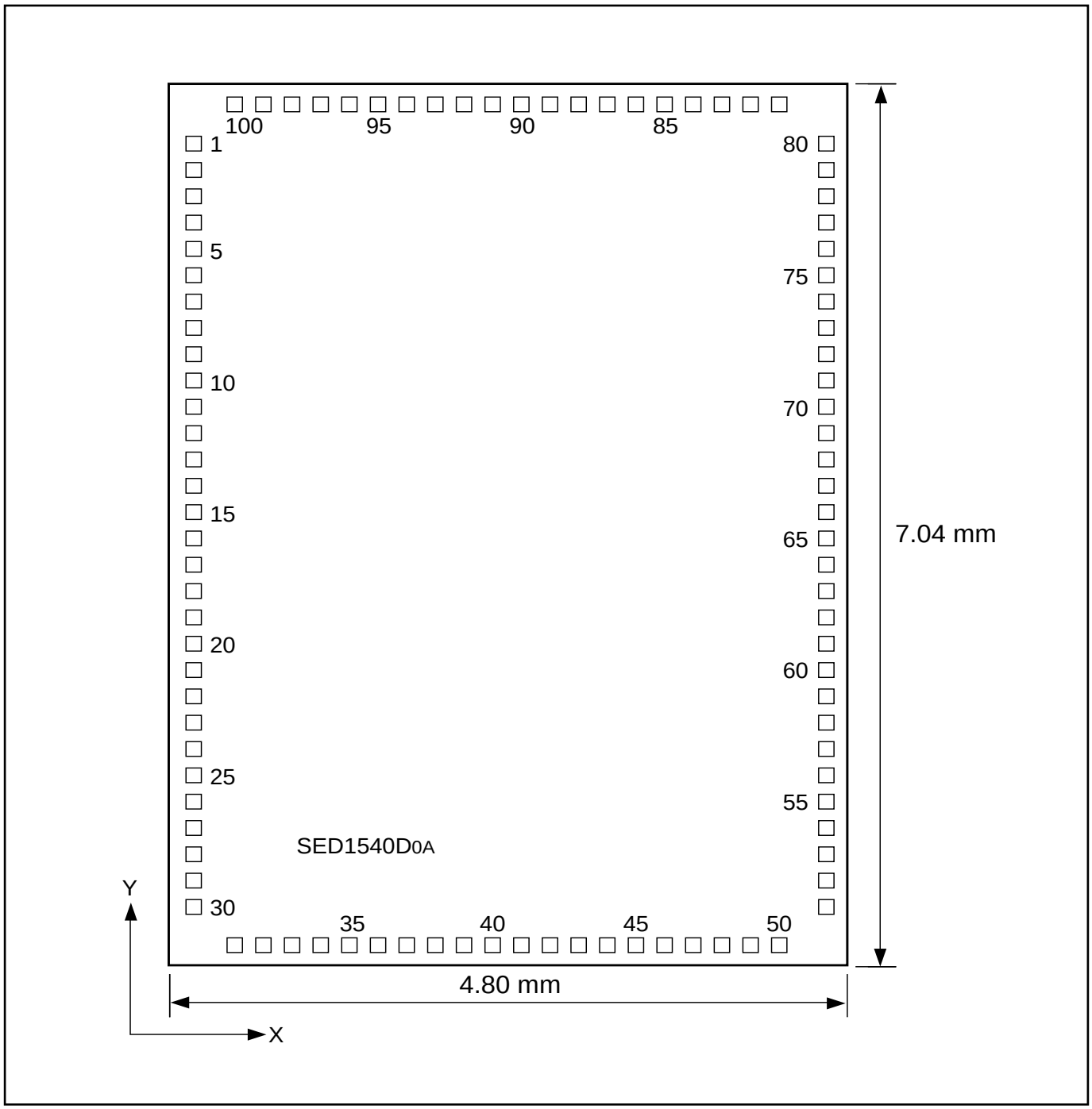
10.0 PAD LAYOUT

10.1 PAD LAYOUT



10.1.1 Al Pad

Chip Specification	Dimensions
Die size	4.80 x 7.04 x 0.525 mm
Pad size	100 x 100 μm

10.1.2 Au Bump Pad

Chip Specification	Dimensions
Minimum bump pitch	199μm
Bump height	20 μm + 10/–5μm
Bump size	132 x 111 μm ± 20 μm

10.2 PAD COORDINATES

unit: μm

Pad No.	Pin Name	X	Y
1	SED71	159	6507
2	SED70	159	6308
3	SED69	159	6108
4	SED68	159	5909
5	SED67	159	5709
6	SED66	159	5510
7	SED65	159	5310
8	SED64	159	5111
9	SED63	159	4911
10	SED62	159	4712
11	SED61	159	4512
12	SED60	159	4169
13	SED59	159	3969
14	SED58	159	3770
15	SED57	159	3570
16	SED56	159	3371
17	SED55	159	3075
18	SED54	159	2876
19	SED53	159	2576
20	SED52	159	2477
21	SED51	159	2277
22	SED50	159	2078
23	SED49	159	1878
24	SED48	159	1679
25	SED47	159	1479
26	SED46	159	1280
27	SED45	159	1080
28	SED44	159	881
29	SED43	159	681
30	SED42	159	482
31	SED41	504	153
32	SED40	704	153
33	SED39	903	153
34	SED38	1103	153
35	SED37	1302	159
36	SED36	1502	159
37	SED35	1701	159
38	SED34	1901	159
39	SED33	2100	159
40	SED32	2300	159
41	SED31	2499	159
42	SED30	2699	159
43	SED29	2898	159
44	SED28	3098	159
45	SED27	3297	159
46	SED26	3497	159
47	SED25	3896	159
48	SED24	3895	159
49	SED23	4095	159
50	SED22	4295	159
51	SED21	4641	482
52	SED20	4641	681
53	SED19	4641	881
54	SED18	4641	1080
55	SED17	4641	1280
56	SED16	4641	1479
57	SED15	4641	1679
58	SED14	4641	1878
59	SED13	4641	2078
60	SED12	4641	2277
61	SED11	4641	2477
62	SED10	4641	2676
63	SED9	4641	2875
64	SED8	4641	3075
65	SED7	4641	3275
66	SED6	4641	3474
67	SED5	4641	3574
68	SED4	4641	3948
69	SED3	4641	4148
70	SED2	4641	4347
71	SED1	4641	4547
72	SED0	4641	4789
73	A_0	4641	5048
74	OSC1	4641	5247
75	OSC2	4641	5447
76	E($\overline{RD}$)	4641	5646
77	R/W ($\overline{WR}$)	4641	5846
78	V_{SS}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3686	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2858	6884
89	FR	2699	6884
90	V_3	2499	6884
91	$\overline{CS}$	2300	6884
92	MC	2100	6884
93	M/S	1901	6884
94	V_2	1701	6884
95	V_1	1502	6884
96	COM 0	1302	6884
97	COM 1	1103	6884
98	COM 2	903	6884
99	COM 3	704	6884
100	SED72	504	6884