

# SED1758

## LOW-POWER 160-BIT LCD SEGMENT DRIVER

### DESCRIPTION

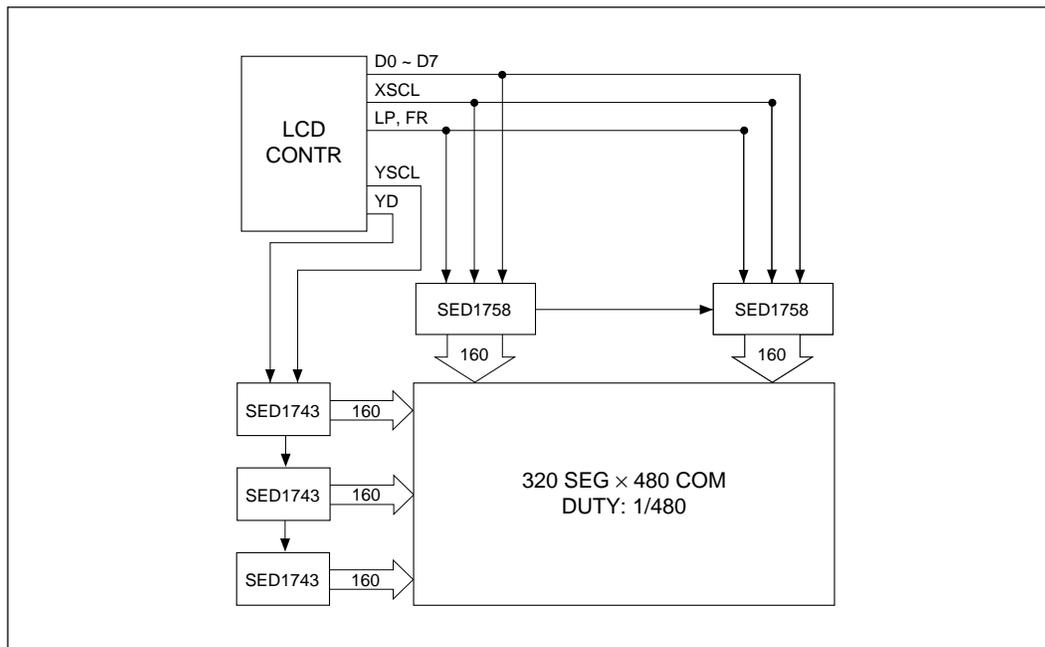
The SED1758 is a 160-bit dot matrix LCD segment (column) driver for driving high-resolution color STN LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of the LCD drive voltages. The device uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1758 is used in conjunction with the SED1743 (160-bit common driver) to drive a large-capacity dot matrix LCD panel.

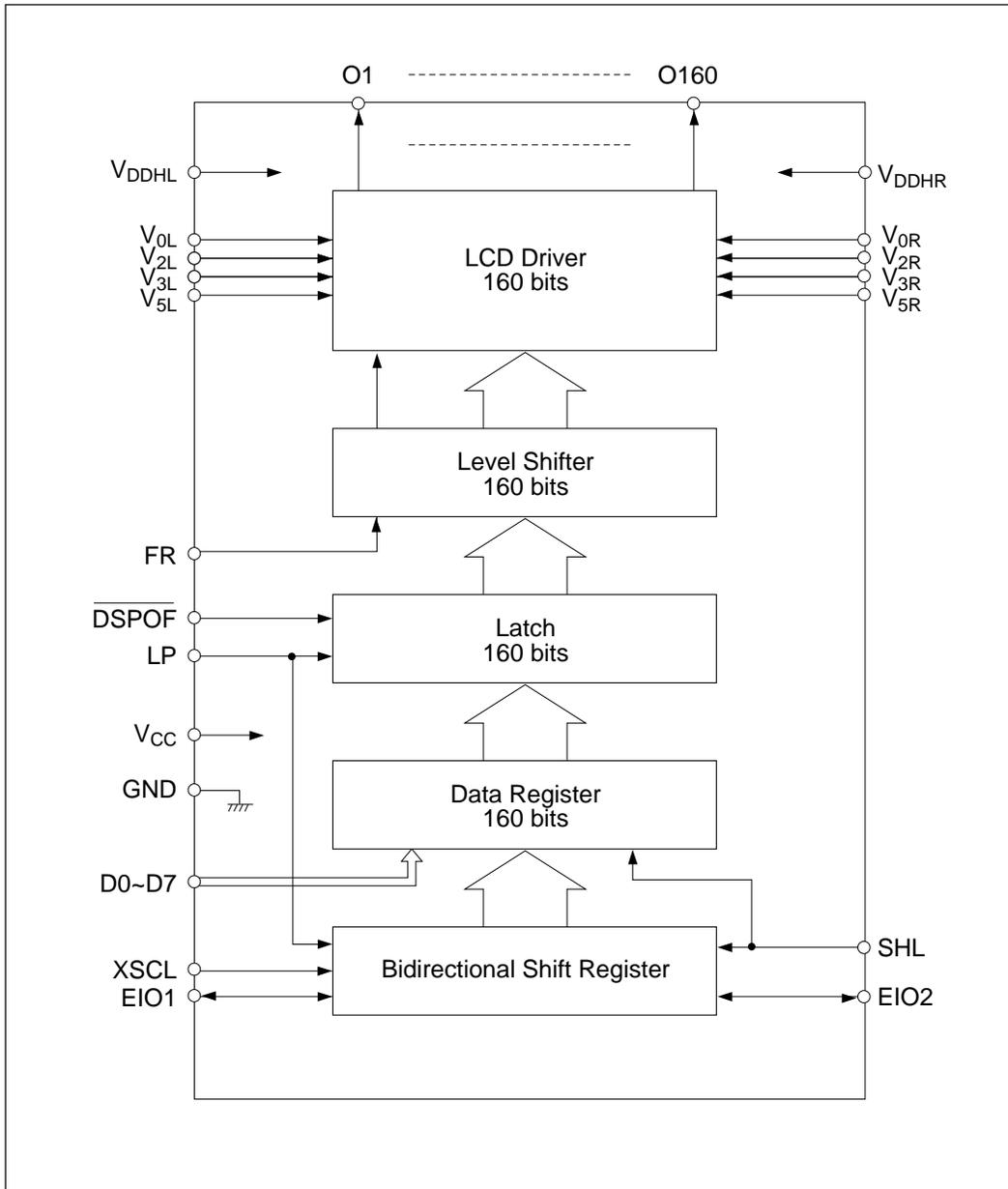
### FEATURES

- Low-power, high-speed CMOS technology
- 160-bit segment (column) driver
- High-speed 8-bit data bus
- Duty cycle ..... 1/100 to 1/500
- Adjustable LCD drive voltages
- Unbiased display off function
- Adjustable offset bias of the LCD according to  $V_{DDH}$  and GND
- Shift clock frequency . 16MHz max at  $V_{DD} = 5V$
- Ability to adjust offset bias of the LCD source from  $V_{DD}$
- High-speed daisy chain enable support
- Adjustable offset bias of the liquid crystal according to the  $V_{DDH}$  and GND
- LCD voltage ..... 8 to 42V
- Supply voltage ..... 2.7 to 5.5V
- Package
  - T0A ..... Slim TAB (9.3mm)
  - T0B ..... Bending TAB
  - T0G ..... Ultra slim TAB (7.3mm)

### SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ **BLOCK DESCRIPTION**

● **Enable Shift Register**

The enable shift register is a bidirectional shift register where the direction of the shift is selected by the SHL input. The output of this shift register is used to store the data bus signals in the data register.

When the enable signal is in a disable state, the internal clock signal and data bus are fixed at “L”, placing the chip in power save mode.

When multiple segment drivers are used, the EIO terminals of the various drivers are cascade connected and the EIO terminal of the first driver is connected to GND. (See the example of connection, below.)

The enable control circuit automatically senses when 160 bits worth of data have been received, and sends the enable signal, thus eliminating the need for a control signal from the control LSI.

● **Data Register**

This is a register to convert the data bus signal from serial to parallel using the output of the enable shift register. Consequently, the relationships between the serial display data and the segment output is determined independently of the shift clock input number.

● **Latch**

The latch receives the contents of the data registers when triggered by the falling edge of the LP, and outputs them to the level shifter.

● **Level Shifter**

The level shifter is a level interface circuit which converts the signal voltage level from a logic circuit level to the LC driver voltage level.

● **LCD Driver**

The LCD driver outputs the LC drive voltage.

The relationship between the data bus signal, the AC signal FR, and the segment output voltage is as follows:

DSPOFF	Data Bus Signal	FR Voltage	Driver $\bar{O}$ Voltage
H	H	H	V0
		L	V5
	L	H	V2
		L	V3
L	—	—	V5



■ PIN DESCRIPTION

Pin Name	I/O	Function	No. of Pins																																							
O0 to O160	O	Segment (column) output to drive LC. Output transition occurs on falling edge of LP.	160																																							
D0 to D7	I	Display data input.	8																																							
XSCL	I	Display data shift clock input (triggers on falling edge)	1																																							
LP	I	Display data latch pulse input (triggers on falling edge)	1																																							
EIO1 EIO2	I/O	Enable I/O This is set to input or output depending on the level of the SHL input. The output is reset by the LP input, and once the 160-bit data reception is complete, the terminals automatically fall to "L".	2																																							
SHL	I	Shift direction select and EIO terminal I/O control pin. When the data has been input to terminals (D0, D1, ..., D7) in the order (a0, a1, ..., a6, a7) (b0, b1, ..., b6, b7) ... (t0, t1, ..., t6, t7), the relationship between the data and the segment output is as shown in the table below: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th rowspan="2">SHL</th> <th colspan="7">O Output</th> <th colspan="2">EIO</th> </tr> <tr> <th>O1</th> <th>O2</th> <th>O3</th> <th></th> <th>O158</th> <th>O159</th> <th>O160</th> <th>1</th> <th>2</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>a7</td> <td>a6</td> <td>a5</td> <td>...</td> <td>t2</td> <td>t1</td> <td>t0</td> <td>I</td> <td>O</td> </tr> <tr> <td>H</td> <td>t0</td> <td>t1</td> <td>t2</td> <td>...</td> <td>a5</td> <td>a6</td> <td>a7</td> <td>O</td> <td>I</td> </tr> </tbody> </table> <p><b>Note:</b> The relationship between the data and the segment output is independent of the shift clock number.</p>	SHL	O Output							EIO		O1	O2	O3		O158	O159	O160	1	2	L	a7	a6	a5	...	t2	t1	t0	I	O	H	t0	t1	t2	...	a5	a6	a7	O	I	1
SHL	O Output							EIO																																		
	O1	O2	O3		O158	O159	O160	1	2																																	
L	a7	a6	a5	...	t2	t1	t0	I	O																																	
H	t0	t1	t2	...	a5	a6	a7	O	I																																	
FR	I	LC drive output AC signal input	1																																							
Vcc, GND	Power	Power source for logic: GND : 0V Vcc : +3.3, +5V	2																																							
VDDHL, VOL, V2L, V3L, V5L, VDDHR, VOR, V2R, V3R, V5R	Power	LC drive circuit power: GND : 0V VDDH: +14 to +42V VDDH ≥ V0 ≥ V2 ≥ 7/9 × V0 2/9 × V0 ≥ V3 ≥ V5 ≥ GND	10																																							
DSPOFF	I	Forced bias set input. "L" level input forces the bias to the V5 level. * When this function is used, it cannot be used in combination with the SED1703.	1																																							

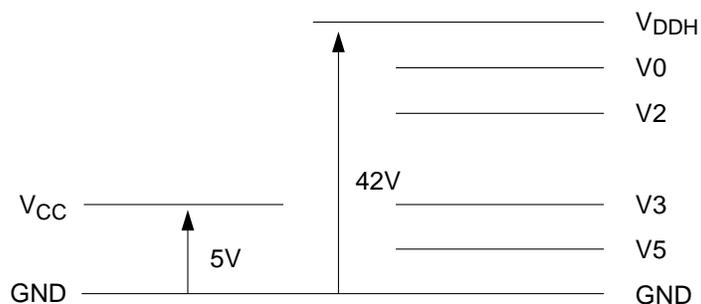
Total: 187

■ ELECTRICAL CHARACTERISTICS  
 ● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Power voltage (1)	V <sub>CC</sub>	-0.3 to +7.0	V
Power voltage (2)	V <sub>DDH</sub>	-0.3 to +45.0	V
Power voltage (3)	V <sub>0</sub> , V <sub>2</sub> , V <sub>3</sub> , V <sub>5</sub>	GND - 0.3 to V <sub>CC</sub> + 0.3	V
Input voltage	V <sub>I</sub>	GND - 0.3 to V <sub>CC</sub> + 0.3	V
Output voltage	V <sub>O</sub>	GND - 0.3 to V <sub>CC</sub> + 0.3	V
EIO output current	I <sub>O1</sub>	20	mA
Operating temperature	T <sub>OPR</sub>	-30 to +85	°C
Storage temperature 1	T <sub>STG1</sub>	-65 to +150	°C
Storage temperature 2	T <sub>STG2</sub>	-55 to +100	°C

Notes:

1. All voltages are given relative to GND = 0V.
2. Storage temperature 1 is the recommendation for the chip itself, and storage temperature 2 is the recommendation for the chip mounted on a TCP.
3. Ensure that the relationship between V<sub>0</sub>, V<sub>2</sub>, V<sub>3</sub> and V<sub>5</sub> is always as follows: V<sub>DDH</sub> ≥ V<sub>0</sub> ≥ V<sub>2</sub> ≥ V<sub>3</sub> ≥ V<sub>5</sub> ≥ GND.



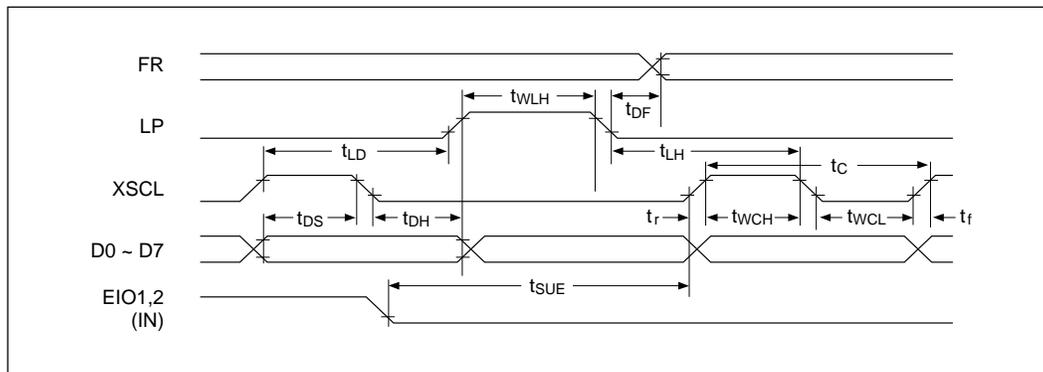
4. The LSI may be permanently damaged if the logic system power is floating or V<sub>CC</sub> is less than or equal to 2.6V when power is applied to the LC drive circuit system. Special caution must be paid to the power sequences when turning the power on and off.

● DC Electrical Characteristics

Unless otherwise specified, GND = V5 = 0V,  
V<sub>CC</sub> = +5.0V ±10%, T<sub>a</sub> = -30 to +85°C

Parameter	Symbol	Conditions		Applicable Pins	Min	Typ	Max	Unit
Power voltage (1)	V <sub>CC</sub>			V <sub>CC</sub>	2.7	—	5.5	V
Recommended operating voltage	V <sub>0</sub>			V <sub>OL</sub> , V <sub>DDHL</sub> , V <sub>OR</sub> , V <sub>DDHR</sub>	14.0	—	40.0	V
Possible operating voltage	V <sub>0</sub>	Function			8.0	—	42.0	V
Power voltage (2)	V <sub>2</sub>	Recommended value		V <sub>2L</sub> , V <sub>2R</sub>	7/9 × V <sub>0</sub>	—	V <sub>0</sub>	V
Power voltage (3)	V <sub>3</sub>	Recommended value		V <sub>3L</sub> , V <sub>3R</sub>	GND	—	2/9 × V <sub>0</sub>	V
High-level input voltage	V <sub>IH</sub>	V <sub>CC</sub> = 2.7 to 5.5V		EIO1, EIO2, FR, D0 ~ D7, XSCL, SHL, LP, DSPOFF	0.8 × V <sub>CC</sub>	—	—	V
Low-level input voltage	V <sub>IL</sub>				—	—	0.2 × V <sub>CC</sub>	V
High-level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 2.7 to 5.5V	I <sub>OH</sub> = -0.6mA	EIO1, EIO2	V <sub>CC</sub> - 0.4	—	—	V
Low-level output voltage	V <sub>OL</sub>		I <sub>OL</sub> = 0.6mA		—	—	0.4	V
Input leakage current	I <sub>LI</sub>	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		D0 ~ D7, LP, FR, XSCL, SHL, DSPOFF	—	—	2.0	μA
I/O leakage current	I <sub>LI/O</sub>	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		EIO1, EIO2	—	—	5.0	μA
Static current	I <sub>GND</sub>	V <sub>0</sub> = 14.0 to 42.0V, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = GND		GND	—	—	25	μA
Output resistance	R <sub>SEG</sub>	ΔV <sub>ON</sub> = 0.5V Recom- mended value	V <sub>0</sub> = +36.0V, 1/24	O1 ~ O160	—	0.85	2.6	KΩ
			V <sub>0</sub> = +26.0V, 1/20		—	0.90	2.6	
Output resistance deviation within the chip	ΔR <sub>SEG</sub>	ΔV <sub>ON</sub> = 0.5V V <sub>0</sub> = +36.0V, 1/24		O1 ~ O160			90	Ω
Average operating consumption current (1)	I <sub>CC</sub>	V <sub>CC</sub> = +5.0V, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = GND, f <sub>XSCL</sub> = 5.38MHz, f <sub>LP</sub> = 33.6KHz, f <sub>FR</sub> = 70Hz; Input data: checker pattern display, no load		V <sub>CC</sub>	—	0.5	1.1	mA
		V <sub>CC</sub> = +3.0V; other parameters are the same as for V <sub>CC</sub> = 5V			—	0.2	0.6	
Average operating consumption current (2)	I <sub>0</sub>	V <sub>0</sub> = +30.0V, V <sub>CC</sub> = +5.0V, V <sub>3</sub> = +4.0V, V <sub>2</sub> = +26.0V, V <sub>5</sub> = 0.0V; other parameters are the same as for the I <sub>CC</sub> item		V <sub>0</sub>	—	0.15	0.9	mA
Input terminal capacitance	C <sub>I</sub>	Freq. = 1MHz, T <sub>a</sub> = 25°C, Chip alone		D0 ~ D7, LP, FR, XSCL, SHL, DSPOFF	—	—	8	pF
I/O terminal capacitance	C <sub>I/O</sub>			EIO1, EIO2	—	—	15	pF

● AC Characteristics  
 ○ Input Timing Characteristics



$V_{CC} = 5.0V \pm 10\%$ ,  $T_a = -30$  to  $85^\circ C$

Parameter	Symbol	Conditions	Min	Max	Unit
XSCl frequency	$t_c$	$t_r, t_f \leq 11ns *3$	62	—	ns
XSCl high-level pulse width	$t_{wCH}$	—	20	—	ns
XSCl low-level pulse width	$t_{wCL}$	—	20	—	ns
Data setup time	$t_{DS}$	—	10	—	ns
Data hold time	$t_{DH}$	—	10	—	ns
XSCl → LP rising edge	$t_{LD}$	—	-5	—	ns
LP → XSCl falling edge	$t_{LH}$	—	30	—	ns
LP high-level pulse width	$t_{WLH}$	*1	40	—	ns
		*2	35	—	ns
Allowable FR delay	$t_{DF}$	—	-300	+300	ns
EIO setup time	$t_{SUE}$	—	30	—	ns
Input signal conversion time	$t_r, t_f$	*4	—	50	ns

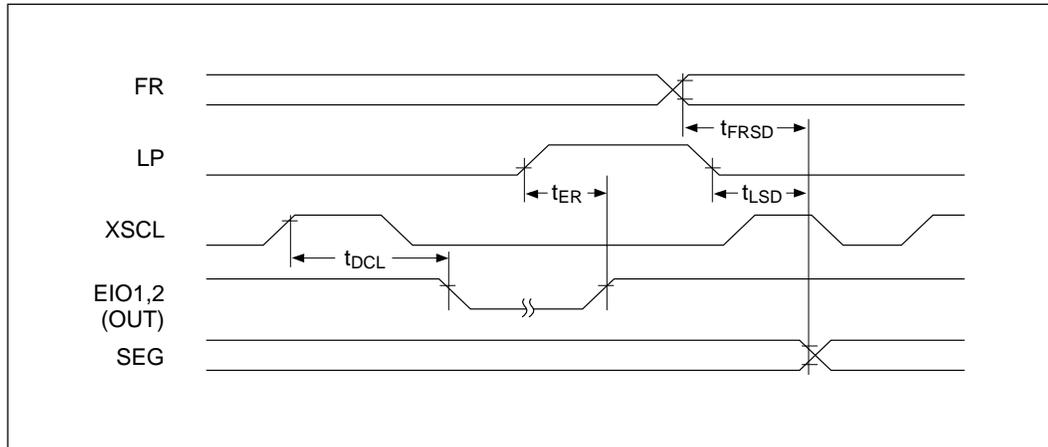
$V_{CC} = 2.7$  to  $4.5V$ ,  $T_a = -30$  to  $85^\circ C$

Parameter	Symbol	Conditions	Min	Max	Unit
XSCl frequency	$t_c$	$t_r, t_f \leq 15ns *3$	100	—	ns
XSCl high-level pulse width	$t_{wCH}$	—	35	—	ns
XSCl low-level pulse width	$t_{wCL}$	—	35	—	ns
Data setup time	$t_{DS}$	—	15	—	ns
Data hold time	$t_{DH}$	—	10	—	ns
XSCl → LP rising edge	$t_{LD}$	—	-10	—	ns
LP → XSCl falling edge	$t_{LH}$	—	60	—	ns
LP high-level pulse width	$t_{WLH}$	*1	75	—	ns
		*2	65	—	ns
Allowable FR delay	$t_{DF}$	—	-300	+300	ns
EIO setup time	$t_{SUE}$	—	40	—	ns
Input signal conversion time	$t_r, t_f$	*4	—	50	ns

- Notes:**
- \*1.  $t_{WLH}$  indicates the time when LP is "H" and XSCl is "L" when LP is input during the interval when XSCl is "L".
  - \*2.  $t_{WLH}$  when LP rises beginning during the interval when XSCl is "H" (where the definition is the same as in "\*1").
  - \*3. When the shift clock (XSCl) is set to high-speed operation, the constraint that follows holds true:  
 $t_r + t_f \leq (t_c - t_{wCL} - t_{wCH})$ .
  - \*4. During high-speed data transfer with continuous shift clock, the maximum LP signal  $t_r + t_f$  is  
 $(t_c + t_{wCH} - t_{LD} - t_{WLH} - t_{LH})$ .

## SED1758

### ○ Output Timing Characteristics



$V_{CC} = +5.0V \pm 10\%$ ,  $V_0 = +14.0$  to  $+42.0V$

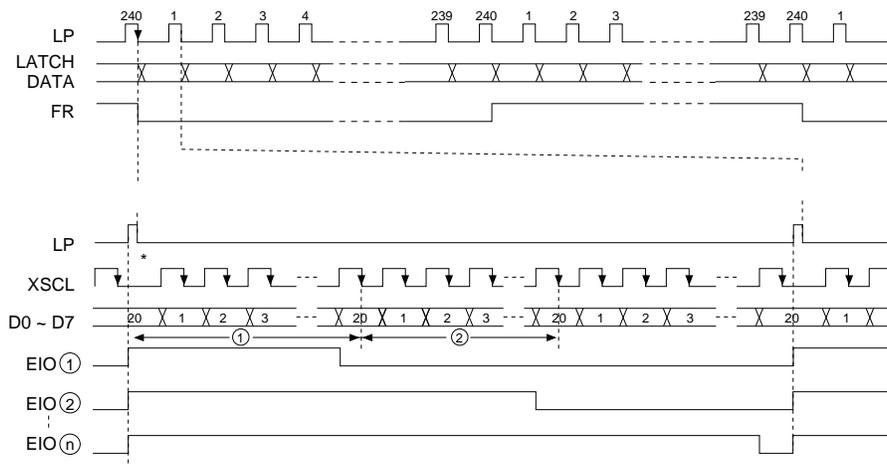
Parameter	Symbol	Conditions	Min	Max	Unit
EIO reset time	$t_{ER}$	CL = 15pF (EIO)	—	120	ns
EIO output delay time	$t_{DCL}$		—	55	ns
LP → SEG output delay time	$t_{LSD}$	CL = 100pF (On)	—	200	ns
FR → SEG output delay time	$t_{FRSD}$		—	400	ns

$V_{CC} = +2.7$  to  $4.5V$ ,  $V_0 = +14.0$  to  $+28.0V$

Parameter	Symbol	Conditions	Min	Max	Unit
EIO reset time	$t_{ER}$	CL = 15pF (EIO)	—	240	ns
EIO output delay time	$t_{DCL}$		—	85	ns
LP → SEG output delay time	$t_{LSD}$	CL = 100pF (On)	—	400	ns
FR → SEG output delay time	$t_{FRSD}$		—	800	ns

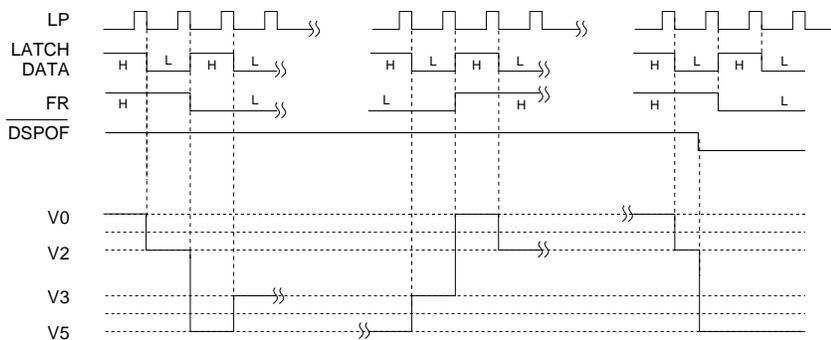
● Timing Diagram

Timing Diagram (assuming 1/240 duty). (This diagram provided only as a reference.)



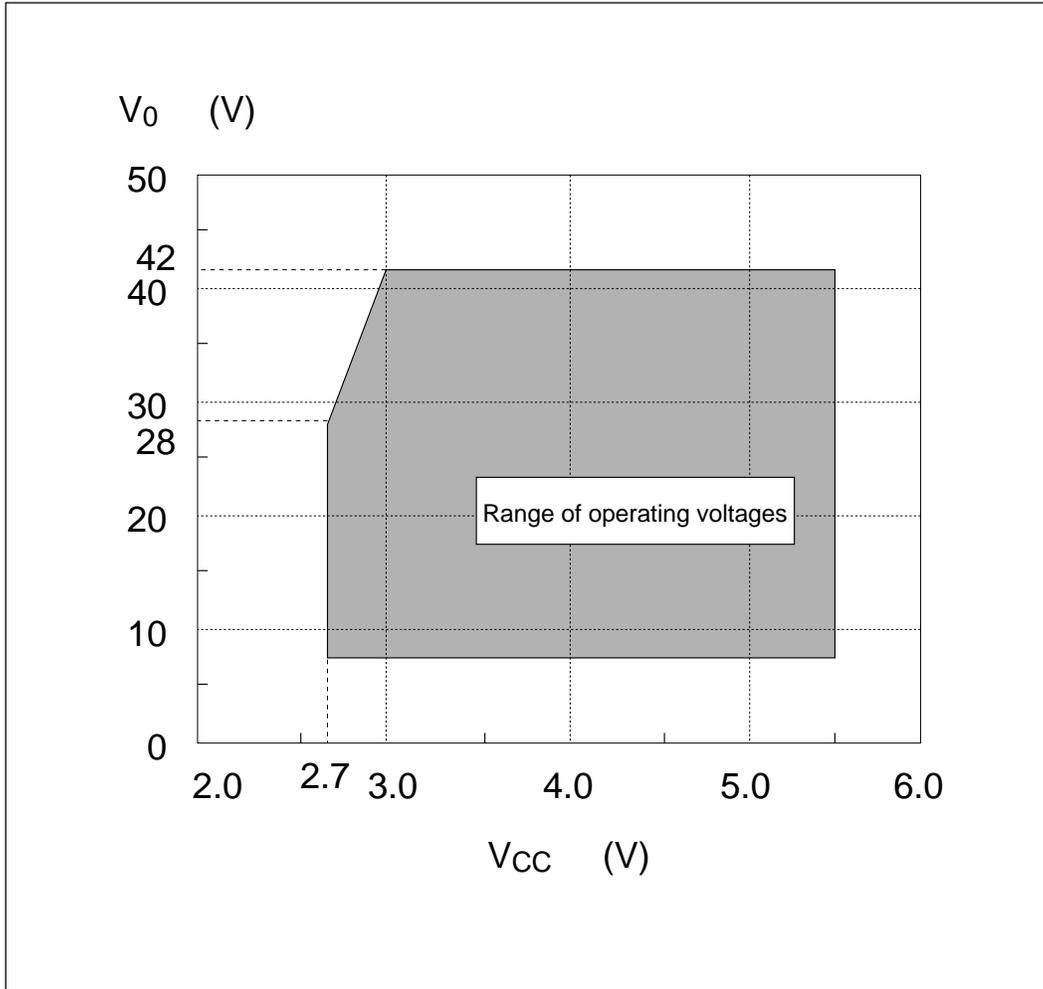
① ~ ③ indicate driver cascade numbers.

Under high-speed data transfer, it is necessary to make the XSCS frequency longer than the LP pulse delay timing to ensure the LP → XSCS ( $t_{LH}$ ) standard values.



■ RANGE OF OPERATING VOLTAGES  $V_{CC} - V_0$

It is necessary to set the voltage of  $V_0$  in the range of voltages  $V_{CC} - V_0$  shown in the figure below:



## ■ LCD DRIVING POWER

### ● Method of Forming Each Voltage Level

The simplest way to obtain the voltage levels for driving the LCs is to use resistive voltage dividers between V0 and GND, and to drive the LCs with op amp voltage followers.

In consideration of the use of op amps, V5 (the lowest voltage setting for driving LCs) and GND are separated and given separate terminals.

However, when the voltage level of V5 is above GND and the voltage difference between V5 and GND is large, the performance of the LC output driver is reduced. Therefore, ensure that the voltage gap between V5 and GND is in the range of 0V to 2.5V.

Permanent damage may result to the LSI when there is serial resistance in the V0 or GND power line. This is because, a voltage drop will occur at V0 or GND of the LSI power terminal (depending on the IO when the signal is changed), causing the power level relationships within the LCD (i.e.,  $V_{DDH} \geq V0 \geq V2 \geq V3 \geq V5 \geq \text{GND}$ ) to fail.

When a guard resistance is inserted, voltage stabilization using a capacitance is necessary.

### ● Cautions During Power Up and Power Down

Because of the high voltage of the LC driving system of this LSI, if the power to the logic system is floating or if Vcc is less than or equal to 2.6V when a high voltage of 30V or more is applied to the LC driving system, or if the LC driving signal is output before the LC driving system voltage stabilizes, then too much current will flow, causing damage to the LSI.

It is recommended that the display off function ( $\overline{\text{DSPOF}}$ ) be used until the LC drive system voltage stabilizes, and that the LC drive output voltage be put to the V5 level.

Follow the sequences below during power up and power down:

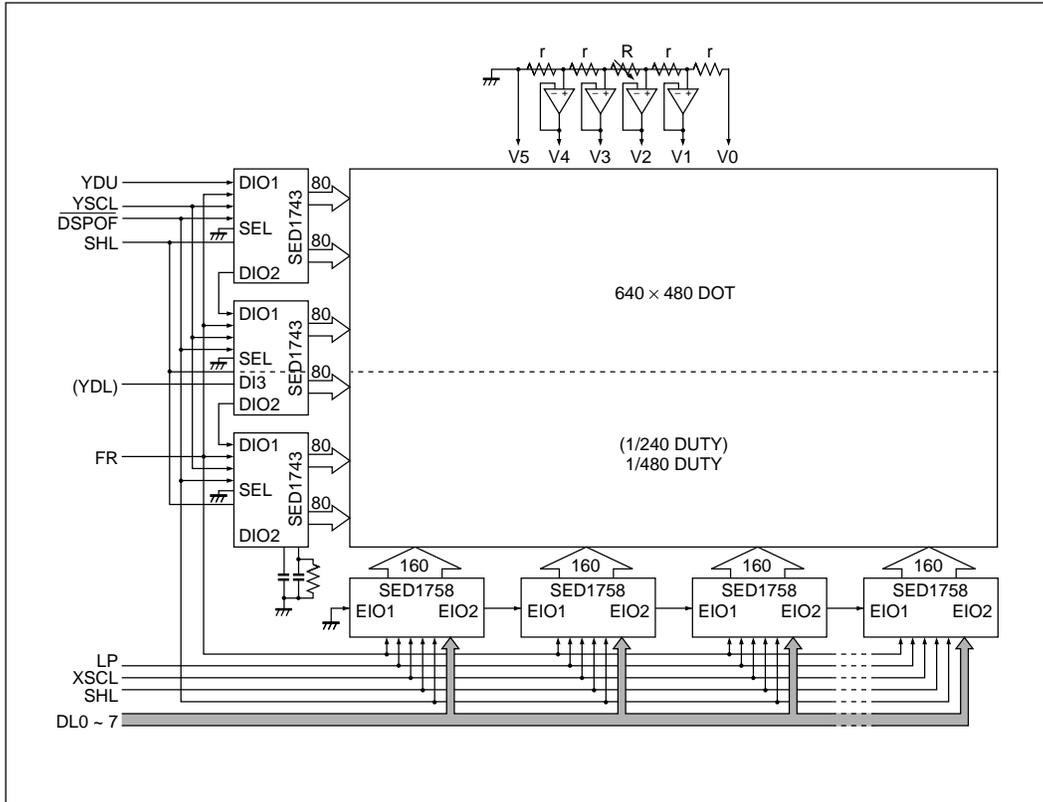
Power up: Logic system on → LC drive system on (or simultaneous)

Power down: LC drive system off → Logic system off (or simultaneous)

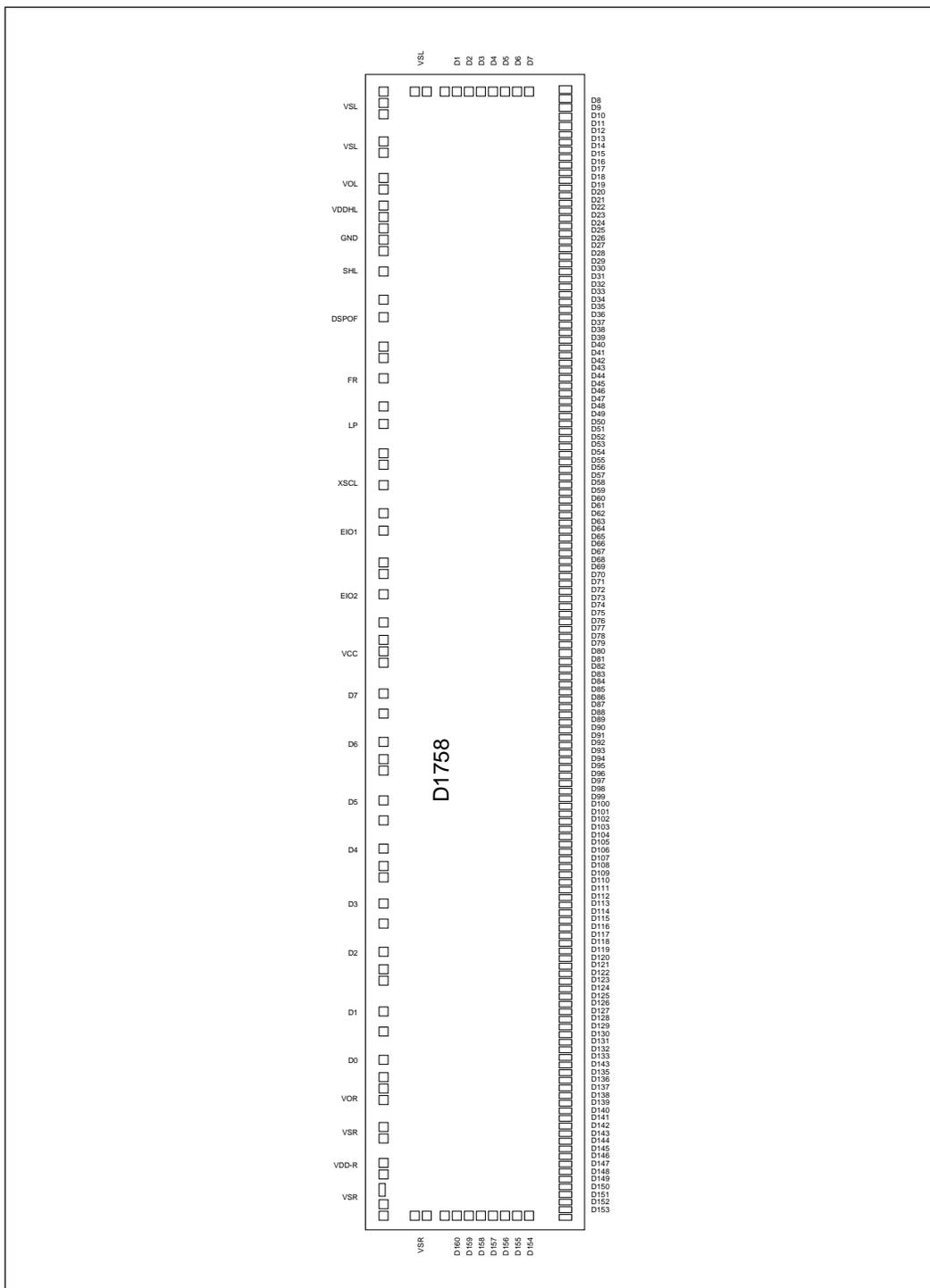
In order to prevent excessive current, insert a high-speed fuse in series with the LC power source. The optimal value of the guard resistance must be selected based on the capacitance of the LC cells.

# SED1758

- EXAMPLE OF CONNECTION
- Large Screen LCD Structure Diagram



■ PAD LAYOUT



■ PAD COORDINATES

Pin No.	Pin Name	X	Y
1	NC	-5953	-915
2	V3L	-5834	-915
3	V3L	-5692	-927
4	V2L	-5419	-915
5	V2L	-5292	-915
6	V0L	-5035	-915
7	V0L	-4907	-915
8	VDDHL	-4748	-937
9	VDDHL	-4620	-937
10	GND	-4491	-937
11	GND	-4364	-937
12	NC	-4235	-937
13	SHL	-4033	-937
14	NC	-3743	-937
15	DSPOF	-3541	-937
16	NC	-3250	-937
17	NC	-3121	-937
18	FR	-2920	-937
19	NC	-2629	-937
20	LP	-2428	-937
21	NC	-2137	-937
22	NC	-2008	-937
23	XSCL	-1806	-937
24	NC	-1561	-937
25	EIO1	-1288	-937
26	NC	-994	-937
27	NC	-865	-937
28	EIO2	-637	-937
29	NC	-345	-937
30	VCC	-119	-937
31	VCC	7	-937
32	NC	136	-937
33	D7	427	-937
34	NC	628	-937
35	D6	919	-937
36	NC	1121	-937
37	NC	1250	-937
38	D5	1540	-937
39	NC	1742	-937
40	D4	2033	-937
41	NC	2234	-937
42	NC	2363	-937
43	D3	2654	-937
44	NC	2855	-937
45	D2	3146	-937
46	NC	3347	-937
47	NC	3477	-937
48	D1	3767	-937
49	NC	3969	-937
50	D0	4259	-937

Pin No.	Pin Name	X	Y
51	NC	4461	-937
52	V0R	4620	-937
53	V0R	4748	-937
54	V2R	5005	-937
55	V2R	5132	-937
56	VDDHR	5390	-937
57	VDDHR	5517	-937
58	V3R	5692	-927
59	V3R	5834	-915
60	NC	5953	-915
61	V5R	5946	-604
62	V5R	5946	-497
63	NC	5967	-311
64	O160	5967	-188
65	O159	5967	-64
66	O158	5967	58
67	O157	5967	182
68	O156	5967	305
69	O155	5967	429
70	O154	5967	552
71	NC	5972	924
72	O153	5878	924
73	O152	5784	924
74	O151	5690	924
75	O150	5596	924
76	O149	5509	924
77	O148	5428	924
78	O147	5348	924
79	O146	5268	924
80	O145	5187	924
81	O144	5107	924
82	O143	5027	924
83	O142	4947	924
84	O141	4866	924
85	O140	4786	924
86	O139	4706	924
87	O138	4626	924
88	O137	4545	924
89	O136	4465	924
90	O135	4385	924
91	O134	4304	924
92	O133	4224	924
93	O132	4144	924
94	O131	4064	924
95	O130	3983	924
96	O129	3903	924
97	O128	3823	924
98	O127	3743	924
99	O126	3662	924
100	O125	3582	924

Pin No.	Pin Name	X	Y
101	O124	3502	924
102	O123	3421	924
103	O122	3341	924
104	O121	3261	924
105	O120	3181	924
106	O119	3100	924
107	O118	3020	924
108	O117	2940	924
109	O116	2859	924
110	O115	2779	924
111	O114	2699	924
112	O113	2619	924
113	O112	2538	924
114	O111	2458	924
115	O110	2378	924
116	O109	2298	924
117	O108	2217	924
118	O107	2137	924
119	O106	2057	924
120	O105	1976	924
121	O104	1896	924
122	O103	1816	924
123	O102	1736	924
124	O101	1655	924
125	O100	1575	924
126	O99	1495	924
127	O98	1415	924
128	O97	1334	924
129	O96	1254	924
130	O95	1174	924
131	O94	1093	924
132	O93	1013	924
133	O92	933	924
134	O91	853	924
135	O90	772	924
136	O89	692	924
137	O88	612	924
138	O87	532	924
139	O86	451	924
140	O85	371	924
141	O84	291	924
142	O83	210	924
143	O82	130	924
144	O81	50	924
145	O80	-39	924
146	O79	-130	924
147	O78	-210	924
148	O77	-290	924
149	O76	-370	924
150	O75	-451	924

Pin No.	Pin Name	X	Y
151	O74	-531	924
152	O73	-611	924
153	O72	-692	924
154	O71	-772	924
155	O70	-852	924
156	O69	-932	924
157	O68	-1013	924
158	O67	-1093	924
159	O66	-1173	924
160	O65	-1254	924
161	O64	-1334	924
162	O63	-1414	924
163	O62	-1494	924
164	O61	-1575	924
165	O60	-1655	924
166	O59	-1735	924
167	O58	-1815	924
168	O57	-1896	924
169	O56	-1976	924
170	O55	-2056	924
171	O54	-2137	924
172	O53	-2217	924
173	O52	-2297	924
174	O51	-2377	924
175	O50	-2458	924
176	O49	-2538	924
177	O48	-2618	924
178	O47	-2698	924
179	O46	-2779	924
180	O45	-2859	924
181	O44	-2939	924
182	O43	-3020	924
183	O42	-3100	924
184	O41	-3180	924
185	O40	-3260	924
186	O39	-3341	924
187	O38	-3421	924
188	O37	-3501	924
189	O36	-3581	924
190	O35	-3662	924
191	O34	-3742	924
192	O33	-3822	924
193	O32	-3903	924
194	O31	-3983	924
195	O30	-4063	924
196	O29	-4143	924
197	O28	-4224	924
198	O27	-4304	924
199	O26	-4384	924
200	O25	-4465	924

Pin No.	Pin Name	X	Y
201	O24	-4545	924
202	O23	-4625	924
203	O22	-4705	924
204	O21	-4786	924
205	O20	-4866	924
206	O19	-4946	924
207	O18	-5026	924
208	O17	-5107	924
209	O16	-5187	924
210	O15	-5267	924
211	O14	-5348	924
212	O13	-5428	924
213	O12	-5508	924
214	O11	-5595	924
215	O10	-5690	924
216	O9	-5784	924
217	O8	-5878	924
218	NC	-5972	924
219	O7	-5967	552
220	O6	-5967	429
221	O5	-5967	305
222	O4	-5967	182
223	O3	-5967	58
224	O2	-5967	-64
225	O1	-5967	-188
226	NC	-5967	-311
227	V5L	-5946	-497
228	V5L	-5946	-604





■ DIAGRAM OF EXTERNAL DIMENSIONS (for reference) (SED1758T<sub>06</sub>)

