SED1640

■ DESCRIPTION

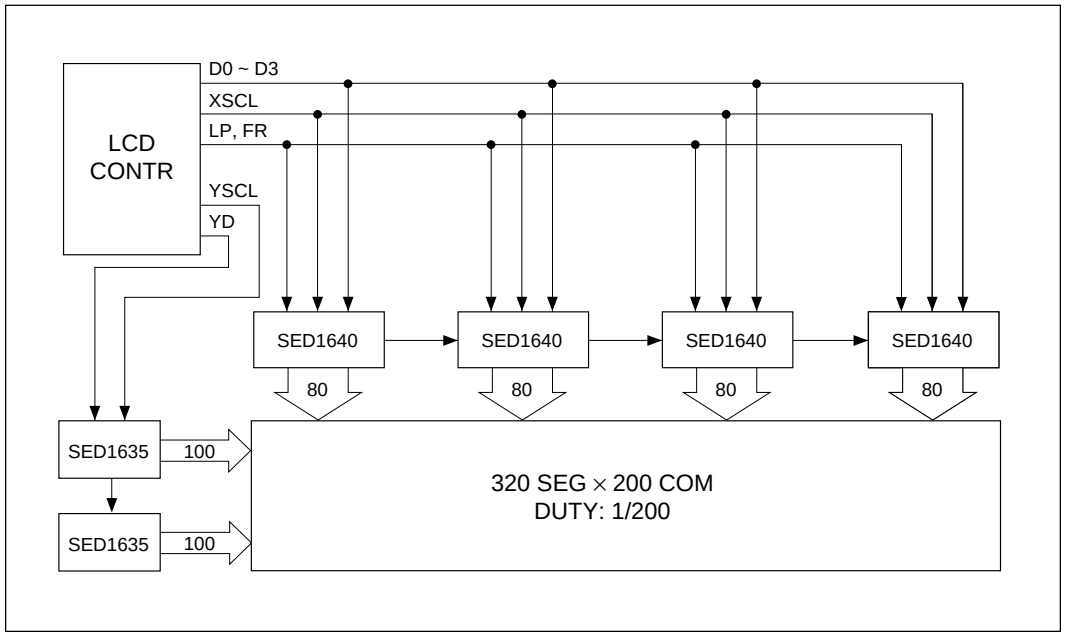
The SED1640 is an 80-output dot matrix LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/300). The LSI has a wide range of LCD driving voltages. The offset bias regulation of the liquid crystal power is possible depending on the V_{DD} level. These unique features allow the SED1640 to interface with a variety of LCD panels. The device does not require a controller to implement an enable daisy chain technology.

The SED1640 is used in conjunction with the SED1651 (100-output row driver) or the SED1635 (100-bit row driver) to drive a large-capacity dot matrix LCD panel.

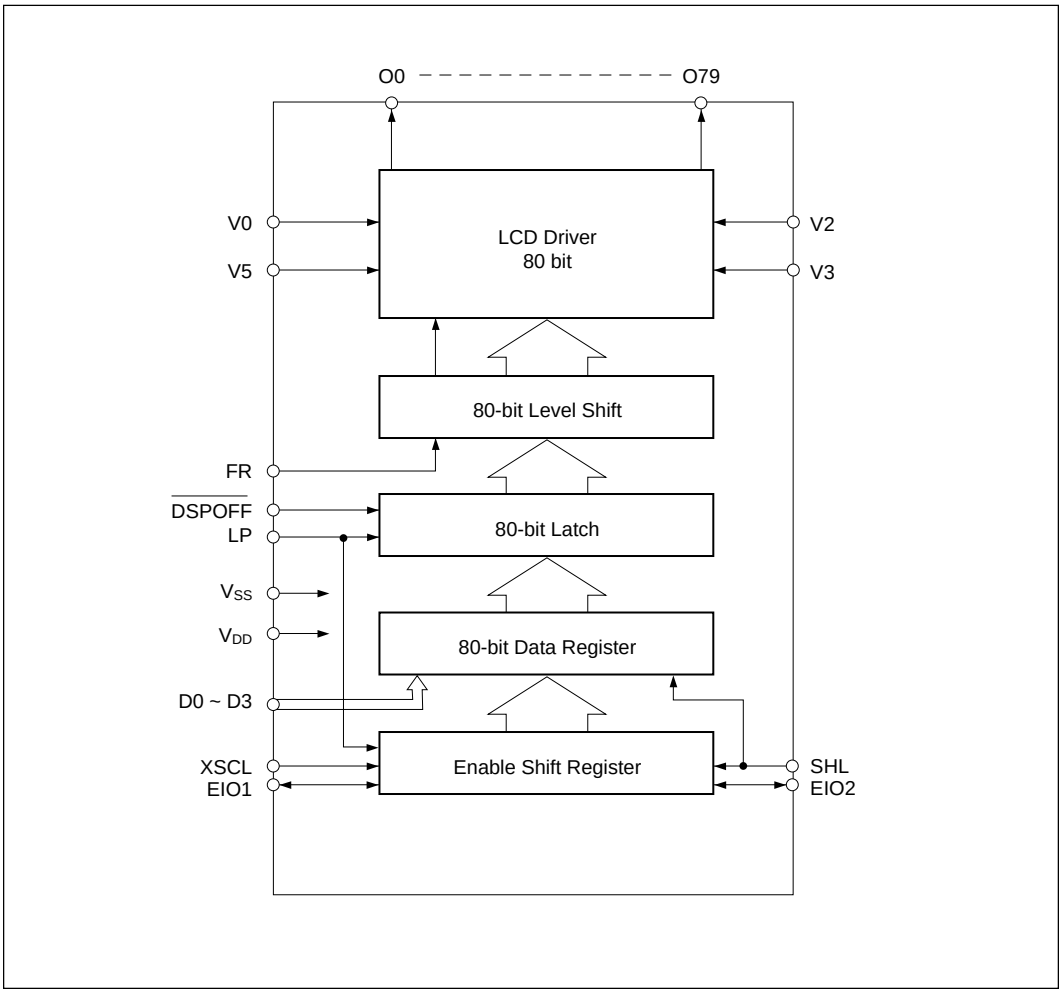
■ FEATURES

- Low-power CMOS technology
- 80-bit segment (column) driver
- High-speed 4-bit bus
- Duty cycle ..... 1/100 to 1/300
- Unbiased display off function
- Shift clock frequency ..... 10MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Daisy chain enable support
- Pin selection of the output shift direction
- LCD voltage ..... –8 to –28V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... Slim DIE (D_{OB})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Enable Shift Register

The enable shift register is a bi-directional shift register where the direction of the shift is selected by the SHL input. The output of this shift register is used to store the data bus signals in the data register.

When the enable signal is in a disable state, the internal clock signal and data bus are fixed at “L”, placing the chip in power save mode.

When multiple segment drivers are used, the EIO terminals of the various drivers are cascade connected and the EIO terminal of the first driver is connected to V_{DD}.

The enable control circuit automatically senses and sends the enable signal when 80 bits worth of data have been received, eliminating the need for a control signal from the control LSI.

● Data Register

This is a register to convert the data bus signal from serial to parallel using the output of the enable shift register. Consequently, the relationships between the serial display data and the segment output are determined independently of the shift clock input number.

● Latch

The latch receives the contents of the data registers when triggered by the falling edge of the LP, and outputs them to the level shifter.

● Level Shifter

The level shifter is a level interface circuit which converts the signal voltage level from a logic circuit level to the LC driver voltage level.

● LCD Driver

The LCD driver outputs the LC drive voltage.

The relationship between the data bus signal, the AC signal FR, and the segment output voltage is as follows:

$\overline{DSPOFF}$	Data Bus Signal	FR	O Output Voltage
H	H	H	V0
		L	V5
	L	H	V2
		L	V3
L	—	—	V0

■ **PIN DESCRIPTION**

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>O0 to O79</td><td>O</td><td>LCD drive segment output; the output changes at the LP falling edge.</td><td>80</td></tr>
<tr><td>D0 to D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock input of display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse input of display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1</td><td>I/O</td><td>Enable I/O</td><td>2</td></tr>
<tr><td>EIO2</td><td></td><td>The terminals are set to the input or output according to the SHL input signal level. The output is reset by LP input. When the 80-bit data is read, the signal automatically goes high.</td><td></td></tr>
<tr><td>SHL</td><td>I</td><td>Used for shift direction selection and I/O control output of EIO terminal.
If data sets (a, b, c, d) (e, f, g, h) ... (w, x, y, z) are entered in this sequence in terminals (D3, D2, D1, D0), the data and segment output are processed as follows:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th>...</th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>...</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>...</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table>
Note: The relationship between the data and segment output is determined regardless of the number of shift clocks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>AC conversion signal input of LCD drive output</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD} : 0V, V_{SS}: –2.7 to –5.5V_{dc}</td><td>3</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power supply</td><td>Power supply for LCD drive circuit
V_{DD}: 0V V5: –8 to –28V_{dc}
$V_{DD} \geq V0 \geq V2 \geq 6/9\ V5$
*1 $3/9\ V5 \geq V3 \geq V5$</td><td>8</td></tr>
<tr><td>DSPOFF</td><td>I</td><td>Forced blank input
When the signal level is low, the output is forcibly set to V0 level.
Note: if this function is used, the SED1631 cannot be used as a pair.</td><td>1</td></tr>
</table>

*1. A pair of V0 to V5 must always be connected to their dedicated LCD power supplies. Total: 107

■ ELECTRICAL CHARACTERISTICS

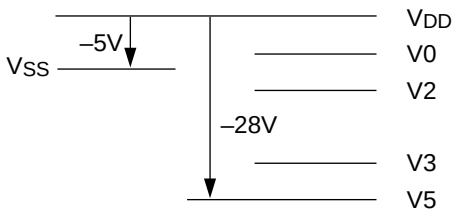
● Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power voltage (1)	V_{SS}	–7.0 to +0.3	V
Power voltage (2)	V5	–30.0 to +0.3	V
Power voltage (3)	V0, V2, V3	V5 – 0.3 to V_{DD} + 0.3	V
Input voltage	VI	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	VO	V_{SS} – 0.3 to V_{DD} + 0.3	V
EIO output current	IO1	20	mA
Operating temperature	T_{OPR}	–40 to +85	°C
Storage temperature 1	T_{STG1}	–65 to +150	°C
Storage temperature 2	T_{STG2}	–55 to +100	°C

Notes:

1. All voltages are based on V_{DD} = 0V.
2. Storage temperature 1 defines the storage temperature of the separate chip, and storage temperature 2 defines the TAB mounted chip.
3. The V0, V2 and V4 voltages must always satisfy the following:

   $V_{DD} \geq V0 \geq C2 \geq C3 \geq V5$



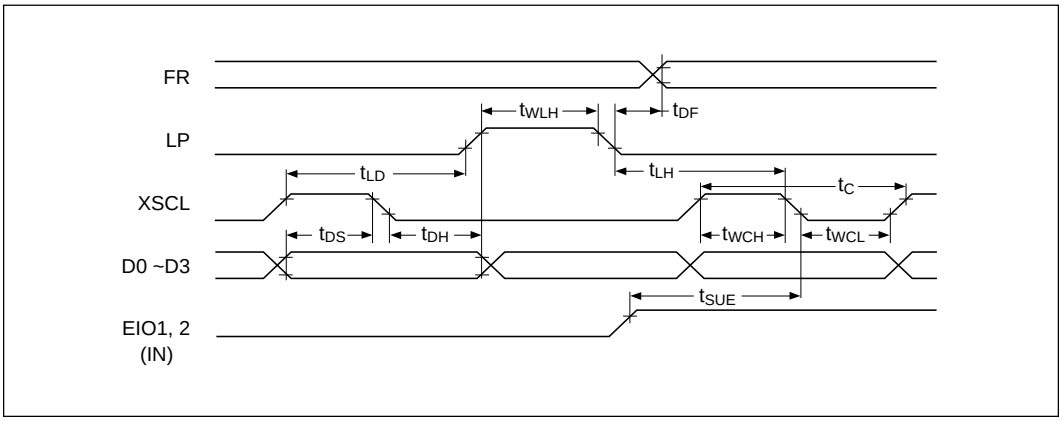
4. If the logic power supply is floating or if it exceeds $V_{SS} = –2.6V_{dc}$ when the LCD drive is powered, the LSI may be destroyed permanently. Care must be taken especially when the system power supply is turned on or off.

- **DC Characteristics**

V_{DD} = V0 = 0V, V_{SS} = –5.0 V_{dc} ± 10%, Ta = –40 to +85°C unless otherwise specified.

Parameter	Symbol	Conditions	Pin Name	Min	Typ	Max	Unit
Power voltage 1	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V5	V_{SS} = –2.7 to –5.5V_{dc}	V5	–28.0	—	–12.0	V
Operation voltage	V5	Function	V5	—	—	–8.0	V
Power voltage 2	V0	Recommended value	V0	V_{DD} – 2.5	—	V_{DD}	V
Power voltage 3	V2	Recommended value	V2	3/9 × V5	—	—	V
Power voltage 4	V3	Recommended value	V3	V5	—	6/9 × V5	V
High-level input current	V_{IH}	V_{SS} = –2.7 to –5.5V_{dc}	EIO1, EIO2, FR, D0 to D3, XSCL, SHL, LP, $\overline{DSPOFF}$	0.2 × V_{SS}	—	—	V
Low-level input current	V_{IL}			—	—	0.8 × V_{SS}	V
High-level output current	V_{OH}	V_{SS} = 2.7 to 5.5V, I_{OH} = 0.6mA	EIO1, EIO2	V_{DD} – 0.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 0.6mA		—	—	V_{SS} + 0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	D0 to D3, LP, FR, XSCL, SHL, $\overline{DSPOFF}$	—	—	2.0	µA
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$	EIO1, EIO2	—	—	5.0	µA
Static current	I_{SS}	V5 = –28.0 to –14.0Vdc, V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{SS}	—	—	25	µA
Output resistance	R_{SEG}	ΔV_{ON} = 0.5, V5 = –20.0V, V3 = 13/15 × V5, V2 = 2/15 × V5, V0 = V_{DD}	O0 to O79	—	1.5	2.5	KΩ
Deviation in chip ON resistance	ΔR_{SEG}	ΔV_{ON} = 0.5, V0 = +36.0V, 1/24	O0 to O159	—	—	90	Ω
Operating current (1)	I_{SS}	V_{SS} = –5.0V_{dc}, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{XSCL} = 2.69MHz, f_{LP} = 16.8KHz, f_{FR} = 70Hz, Input data: Stripe display, no load	V_{SS}	—	0.10	0.2	mA
		V_{SS} = –3.0V_{dc}, other conditions as above	V_{SS}	—	0.07	0.15	mA
Operating current (2)	I_5	V0 = 0.0V, V_{SS} = –5.0V, V3 = –18.6V_{dc}, V2 = –9.3V_{dc}, V5 = –28.0V_{dc}, others as for I_{SS}	V5	—	0.02	0.05	mA
Input capacitance	C_I	Freq. = 1MHz, T_a = 25°C separate chip	D0 to D3, LP, FR, XSCL, SHL, $\overline{DSPOFF}$	—	—	8	pF
Input/output capacitance	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

- **AC Characteristics**
  - **Input Timing Characteristics**



V_{SS} = –5.0V ± 0.5V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
XSCL cycle time	t_C		100	—	ns
XSCL high-level pulse width	t_{WCH}		30	—	ns
XSCL low-level pulse width	t_{WCL}		30	—	ns
Data setup time	t_{DS}		30	—	ns
Data hold time	t_{DH}		20	—	ns
XSCL to LP rise time	t_{LD}		0	—	ns
LP to XSCL fall time	t_{LH}		40	—	ns
LP high-level pulse width	t_{WLH}	*3	40	—	ns
FR delay allowance time	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}		35	—	ns

V_{SS} = –4.5 to –2.7V, T_a = –40 to 85°C

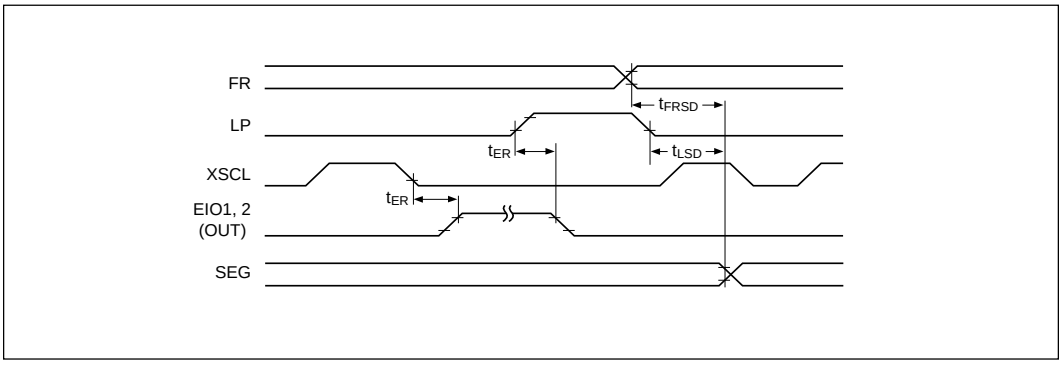
Parameter	Symbol	Conditions		Min	Max	Unit
XSCL cycle time	t_C	V_{SS} = –2.7V	*1	153	—	ns
		V_{SS} = –3.0V	*2	133	—	ns
XSCL high-level pulse width	t_{WCH}			50	—	ns
XSCL low-level pulse width	t_{WCL}			50	—	ns
Data setup time	t_{DS}			50	—	ns
Data hold time	t_{DH}			30	—	ns
XSCL to LP rise time	t_{LD}			0	—	ns
LP to XSCL fall time	t_{LH}	V_{SS} = –2.7V		75	—	ns
		V_{SS} = –3.0V		65	—	ns
LP high-level pulse width	t_{WLH}	V_{SS} = –2.7V	*3	75	—	ns
		V_{SS} = –3.0V	*3	65	—	ns
FR delay allowance time	t_{DF}			–900	+900	ns
EIO setup time	t_{SUE}	V_{SS} = –2.7V		50	—	ns
		V_{SS} = –3.0V		40	—	ns

*1. Equivalent to 6.5MHz

*2. Equivalent to 7.5MHz

*3. "t_{WLH}" defines the time when LP is high and XSCL is low.

- **AC Characteristics**
  - **Output Timing Characteristics**



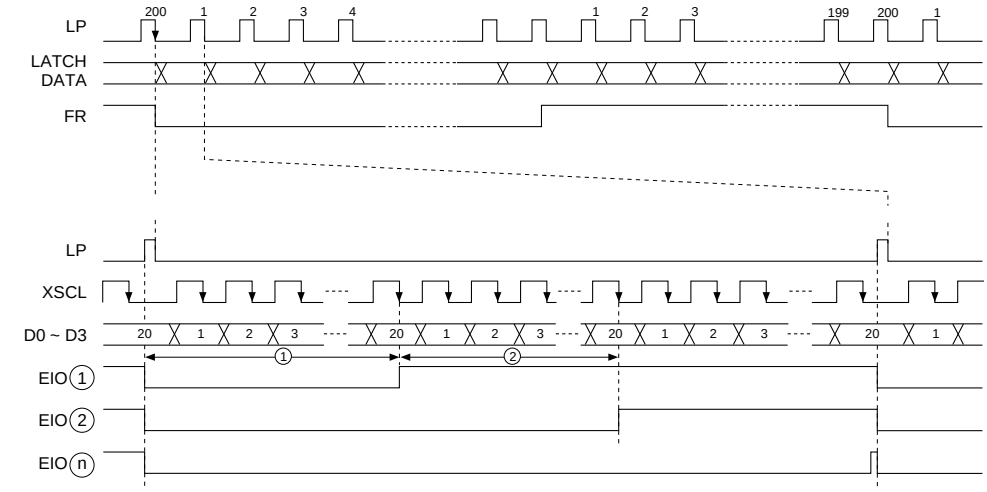
V_{SS} = –5.0V ± 0.5V, V5 = –12.0 to –28.0V

Parameter	Symbol	Conditions	Min	Max	Unit
EIO reset time	t_{ER}	C_L = 15pF (EIO)	—	90	ns
EIO output delay time	t_{DCL}		—	55	ns
Delay time from LP to segment output	t_{LSD}	C_L = 100pF (0...n)	—	200	ns
Delay time from FR to segment output	t_{FRSD}		—	400	ns

V_{SS} = –4.5 to –2.7V, V5 = –12.0 to –28.0V

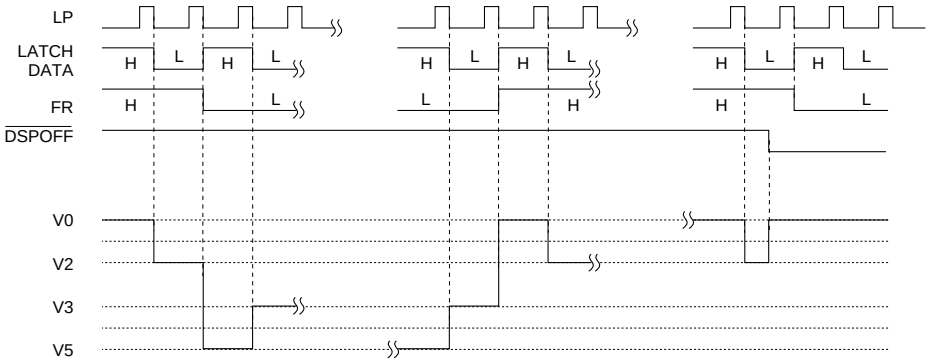
Parameter	Symbol	Conditions		Min	Max	Unit
EIO reset time	t_{ER}	C_L = 15pF (EIO)		—	150	ns
EIO output delay time	t_{DCL}		V_{SS} = –2.7V	—	95	ns
			V_{SS} = –2.7V	—	85	ns
Delay time from LP to segment output	t_{LSD}	C_L = 100pF (0...n)		—	400	ns
Delay time from FR to segment output	t_{FRSD}			—	800	ns

● **Timing Diagram (assuming 1/200 duty) (This diagram is provided only as a reference)**

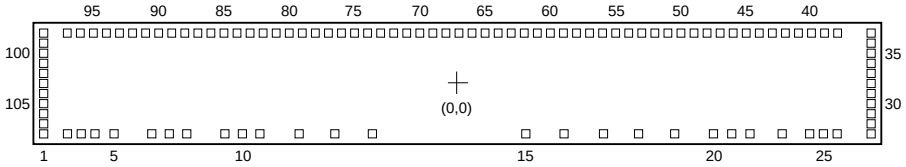


(1) to (n) indicate driver cascade numbers.

* For high-speed data transmission, it is necessary to lengthen the XSCL period in the LP pulse insertion timing to ensure the specified values of LP → XSCL (t_{LH}).



■ PAD LAYOUT



- Chip size ..... 11.59 × 1.40 mm
- Pad pitch ..... 105 µm (Min)
- Chip thickness ..... 625 µm ± 25µm

(1) SED1640DOB Au bump specifications (reference)

Bump size A ..... 106 µm × 80 µm × 4 µm ..... (Pad Nos. 2 to 26)
Bump size B ..... 86 µm × 91 µm × 4 µm ..... (Pad Nos. 1, 27, 37, 98)
Bump size C ..... 86 µm × 68 µm × 4 µm ..... (Pad Nos. 28 to 36, 99 to 107)
Bump size D ..... 82 µm × 74 µm × 4 µm ..... (Pad Nos. 38 to 97)
Bump height A to D ..... 22.5 ± 5.5µm ..... (Pad Nos. 1 to 107)

■ PAD COORDINATES

Pad No.	Pin Name	X	Y
2	V0	–5345	–541
3	V2	–5164	–541
4	V3	–4984	–541
5	V5	–4594	–541
6	V_{SS}	–4091	–541
7	Dummy	–3839	–541
8	SHL	–3587	–541
9	Dummy	–3065	–541
10	Dummy	–2828	–541
11	V_{DD}	–2590	–541
12	$\overline{DSPOFF}$	–2086	–541
13	FR	–1583	–541
14	LP	–1079	–541
15	XSCL	1079	–541
16	D0	1583	–541
17	D1	2086	–541
18	D2	2590	–541
19	Dummy	3065	–541
20	D3	3587	–541
21	Dummy	3839	–541
22	V_{SS}	4091	–541
23	V5	4594	–541
24	V3	4984	–541
25	V2	5164	–541
26	V0	5345	–541
27	EIO1	5644	–544
28	O0	5644	–426
29	O1	5644	–320
30	O2	5644	–215
31	O3	5644	–109
32	O4	5644	–4
33	O5	5644	102
34	O6	5644	207
35	O7	5644	313
36	O8	5644	418
37	O9	5644	546
38	O10	5269	553
39	O11	5090	553
40	O12	4912	553
41	O13	4733	553
42	O14	4554	553
43	O15	4376	553
44	O16	4197	553
45	O17	4019	553
46	O18	3840	553
47	O19	3661	553
48	O20	3483	553
49	O21	3304	553
50	O22	3126	553
51	O23	2947	553
52	O24	2768	553
53	O25	2590	553
54	O26	2411	553
55	O27	2233	553
56	O28	2054	553
57	O29	1875	553
58	O30	1697	553
59	O31	1518	553
60	O32	1340	553
61	O33	1161	553
62	O34	982	553
63	O35	804	553
64	O36	625	553
65	O37	447	553
66	O38	268	553
67	O39	89	553
68	O40	–89	553
69	O41	–268	553
70	O42	–447	553
71	O43	–625	553
72	O44	–804	553
73	O45	–982	553
74	O46	–1161	553
75	O47	–1340	553
76	O48	–1518	553
77	O49	–1697	553
78	O50	–1875	553
79	O51	–2054	553
80	O52	–2233	553
81	O53	–2411	553
82	O54	–2590	553
83	O55	–2768	553
84	O56	–2947	553
85	O57	–3126	553
86	O58	–3304	553
87	O59	–3483	553
88	O60	–3661	553
89	O61	–3840	553
90	O62	–4019	553
91	O63	–4197	553
92	O64	–4376	553
93	O65	–4554	553
94	O66	–4733	553
95	O67	–4912	553
96	O68	–5090	553
97	O69	–5269	553
98	O70	–5644	546
99	O71	–5644	418
100	O72	–5644	313
101	O73	–5644	207
102	O74	–5644	102
103	O75	–5644	–4
104	O76	–5644	–109
105	O77	–5644	–215
106	O78	–5644	–320
107	O79	–5644	–426
1	EIO2	–5644	–544

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