SED1510

CMOS SEGMENT–TYPE LCD CONTROLLER DRIVER

- **Serial Data Interface**
- **Built-in Display data RAM**
- **4 COM Driver Output and 32 SEG Driver Output**

■ DESCRIPTION

The SED1510 is an intelligent CMOS LCD driver-controller for segment type liquid crystal display with the ability of alpha-numeric and graphic application. It can directly drive any static and multiplexed LCD containing up to 4 backplanes and 32 segments.

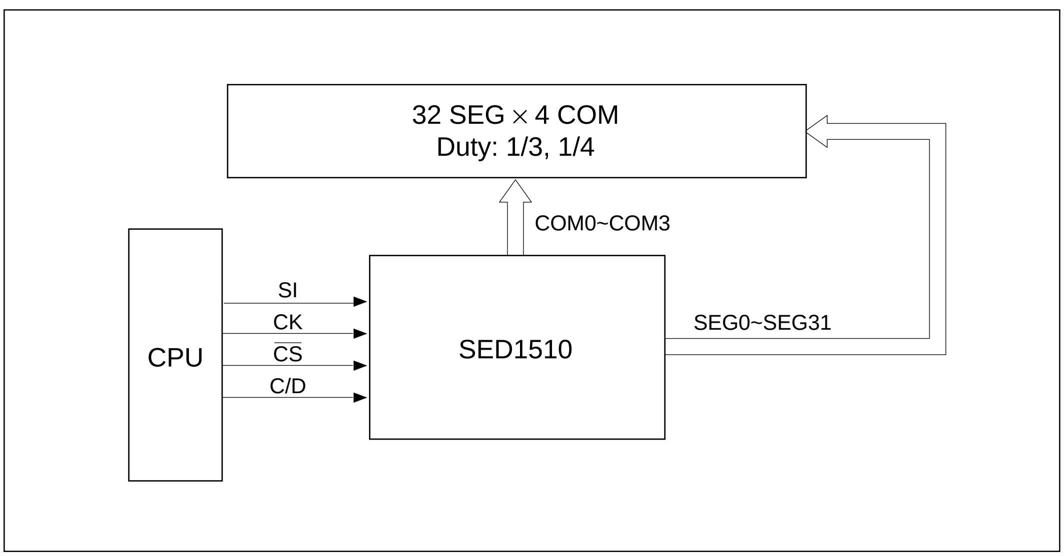
The SED1510 communicates with a host microprocessor through a serial interface. It stores the serial data that is sent from the microprocessor in the built-in data RAM and generates a liquid drive signal.

The SED1510 is manufactured with low power consumption CMOS process allowing use of single power supply between 0.9 and 6.0V.

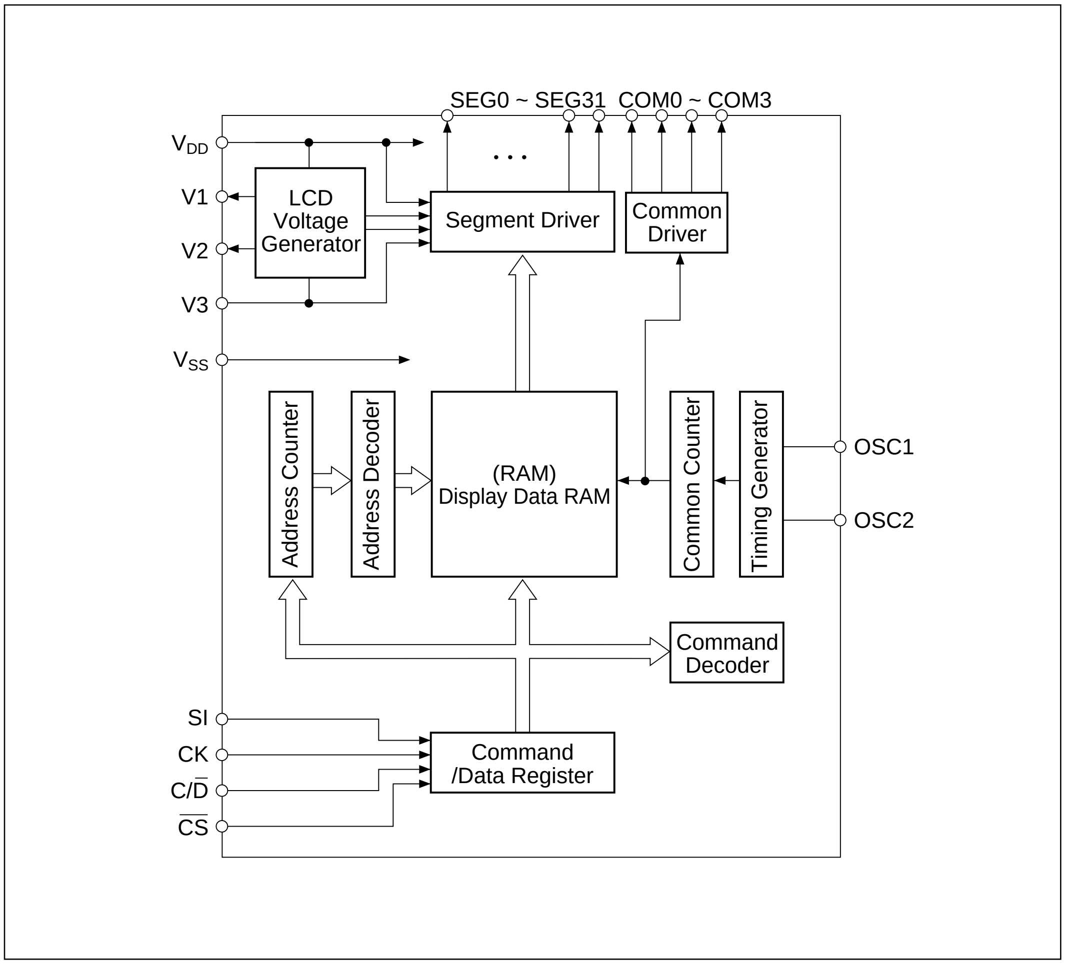
■ FEATURES

- Low-power CMOS technology
- High-speed serial data interface
- Built-in display data RAM (128 bits)
- Provides up to 4 backplanes and 32 segments
- Built-in LCD driver circuitry
- Duty cycle 1/4, 1/3
- Low power consumption .... 150 µW
- Supply voltage .... 0.9 to 6.0V
- LCD voltage .... 1.8 to 6.0V
- Package ..... 1510 .... QFP-12 48-pin (F0C)
QFP-6 60-pin (F0E)
Al pad (D0C)

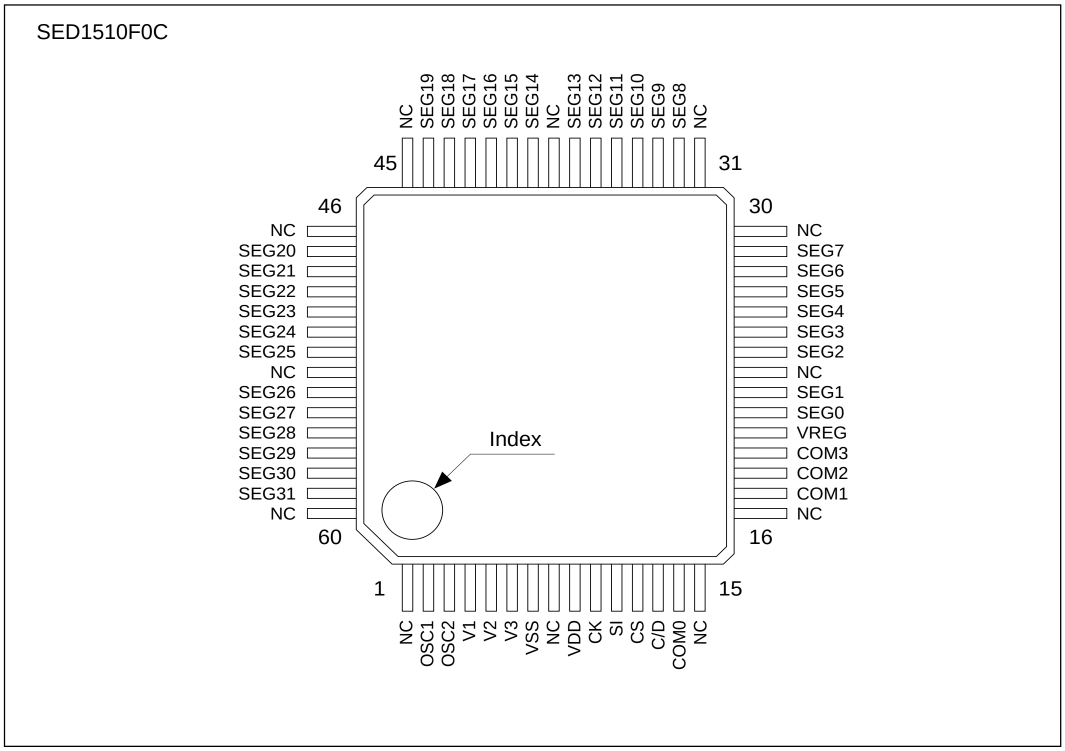
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



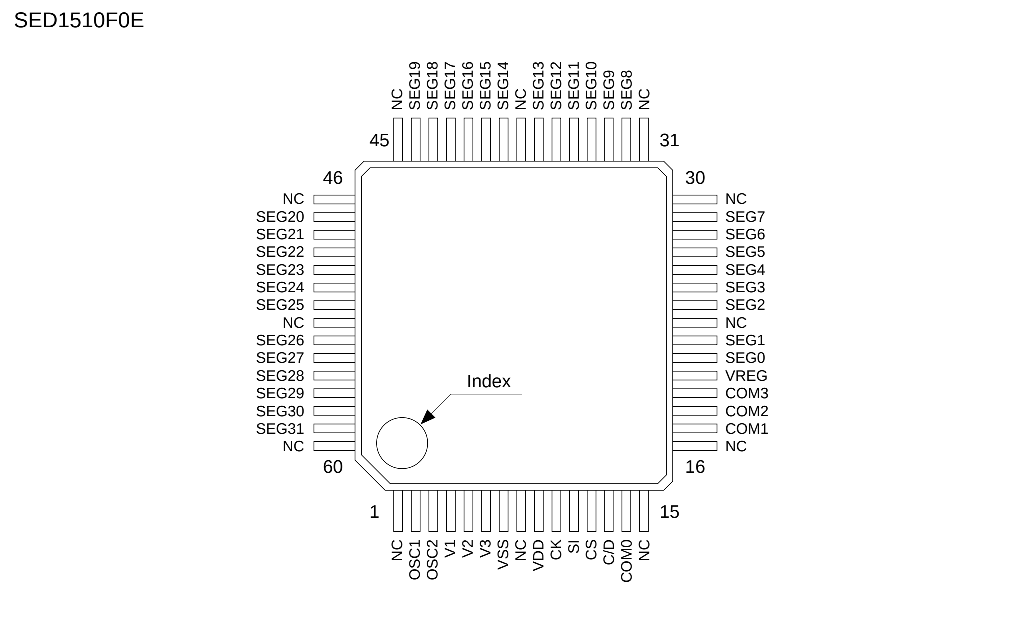
■ PINOUT (SED1510F0C)



■ PIN DESCRIPTION

Number	Name	Description
1	OSC1	Oscillator feedback resistor connection or external clock input
2	OSC2	Oscillator feedback resistor connection
3	V1	LCD driver voltage monitoring outputs
4	V2	
5	V3	LCD driver supply voltage
6	V_{SS}	Negative supply
7	V_{DD}	Positive supply
8	CK	Serial data clock input
9	SI	Serial data input
10	$\overline{CS}$	Active-LOW chip select input
11	C/$\overline{D}$	Command/data select input
12 to 15	COM0 to COM3	LCD common driver outputs
16	VREG	Regulated voltage monitor output
17 to 48	SEG0 to SEG31	LCD segment driver outputs

■ PINOUT (SED1510F0E)



■ PIN DESCRIPTION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NC	21	SEG0	41	SEG16
2	OSC1	22	SEG1	42	SEG17
3	OSC2	23	NC	43	SEG18
4	V1	24	SEG2	44	SEG19
5	V2	25	SEG3	45	NC
6	V3	26	SEG4	46	NC
7	VSS	27	SEG5	47	SEG20
8	NC	28	SEG6	48	SEG21
9	VDD	29	SEG7	49	SEG22
10	CK	30	NC	50	SEG23
11	SI	31	NC	51	SEG24
12	CS	32	SEG8	52	SEG25
13	C/D	33	SEG9	53	NC
14	COM0	34	SEG10	54	SEG26
15	NC	35	SEG11	55	SEG27
16	NC	36	SEG12	56	SEG28
17	COM1	37	SEG13	57	SEG29
18	COM2	38	NC	58	SEG30
19	COM3	39	SEG14	59	SEG31
20	VREG	40	SEG15	60	NC

■ AC ELECTRICAL CHARACTERISTICS

V_{DD} = 0V, V_{SS} = –5.0 ± 0.5V, T_a = –20 to 75°C

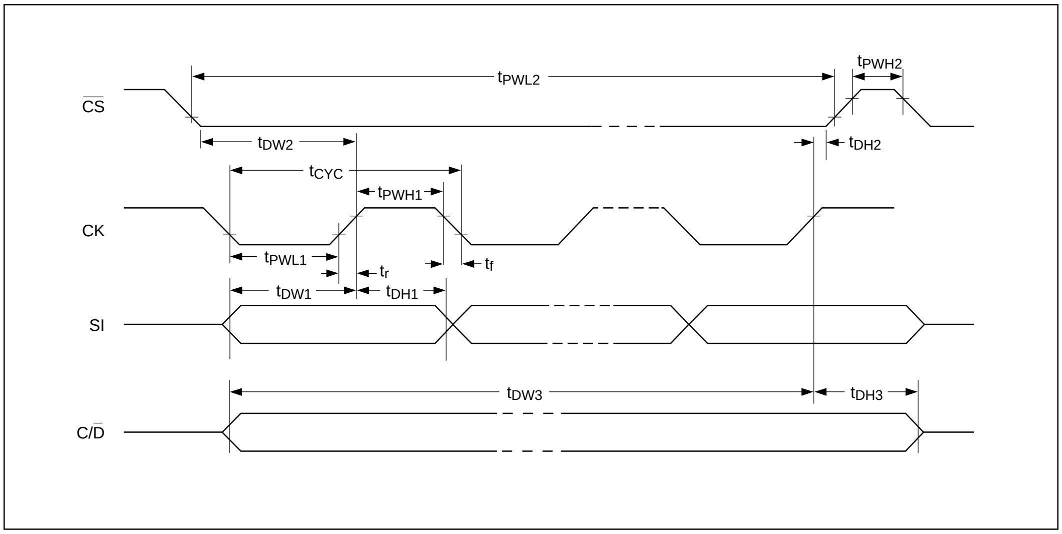
Parameter	Symbol	Condition	Min	Typ	Max	Unit
CK period	t_{CYC}	—	900	—	—	ns
CK LOW-level pulsewidth	t_{PWL1}	—	400	—	—	ns
CK HIGH-level pulsewidth	t_{PWH1}	—	400	—	—	ns
SI to CK setup time	t_{DW1}	—	100	—	—	ns
CK to SI hold time	t_{DH1}	—	200	—	—	ns
$\overline{CS}$ LOW-level pulsewidth	t_{PWL2}	$t_{PWL2} \geq 8t_{CYC}$	7200*1	—	—	ns
$\overline{CS}$ HIGH-level pulsewidth	t_{PWH2}	—	400	—	—	ns
$\overline{CS}$ to CK setup time	t_{DW2}	Referenced to the rising edge of the first CK cycle	100	—	—	ns
CK to $\overline{CS}$ hold time	t_{DH2}	Referenced to the rising edge of the eighth CK cycle	200	—	—	ns
C/$\overline{D}$ to CK setup time	t_{DW3}	Referenced to the rising edge of the eighth CK cycle	9	—	—	µs
CK to C/$\overline{D}$ hold time	t_{DH3}	Referenced to the rising edge of the eighth CK cycle	1	—	—	µs
Rise time	t_r	—	—	—	50	ns
Fall time	t_f	—	—	—	50	ns

*1. $t_{CYC} \times 8$

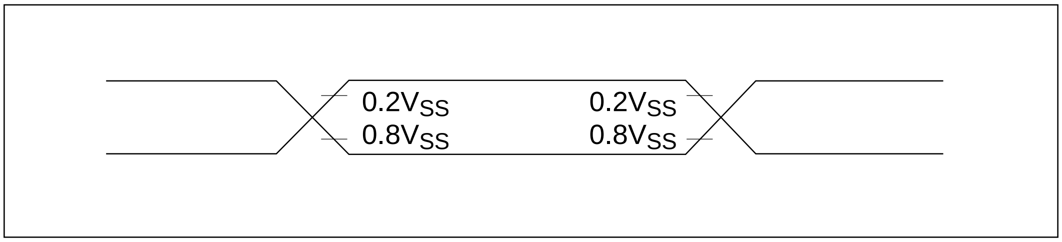
V_{DD} = 0V, V_{SS} = –6.0 to –1.5V, T_a = –20 to 75°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CK period	t_{CYC}	—	10	—	—	µs
CK LOW-level pulsewidth	t_{PWL1}	—	4.5	—	—	µs
CK HIGH-level pulsewidth	t_{PWH1}	—	4.5	—	—	µs
SI to CK setup time	t_{DW1}	—	1.2	—	—	µs
CK to SI hold time	t_{DH1}	—	2.3	—	—	µs
$\overline{CS}$ LOW-level pulsewidth	t_{PWL2}	$t_{PWL2} \geq 8t_{CYC}$	80*1	—	—	µs
$\overline{CS}$ HIGH-level pulsewidth	t_{PWH2}	—	4.5	—	—	µs
$\overline{CS}$ to CK setup time	t_{DW2}	Referenced to the rising edge of the first CK cycle	1.2	—	—	µs
CK to $\overline{CS}$ hold time	t_{DH2}	Referenced to the rising edge of the eighth CK cycle	2.3	—	—	µs
C/$\overline{D}$ to CK setup time	t_{DW3}	Referenced to the rising edge of the eighth CK cycle	100	—	—	µs
CK to C/$\overline{D}$ hold time	t_{DH3}	Referenced to the rising edge of the eighth CK cycle	11	—	—	µs
Rise time	t_r	—	—	—	50	ns
Fall time	t_f	—	—	—	50	ns

*1. $t_{CYC} \times 8$



- **Timing Measurement**

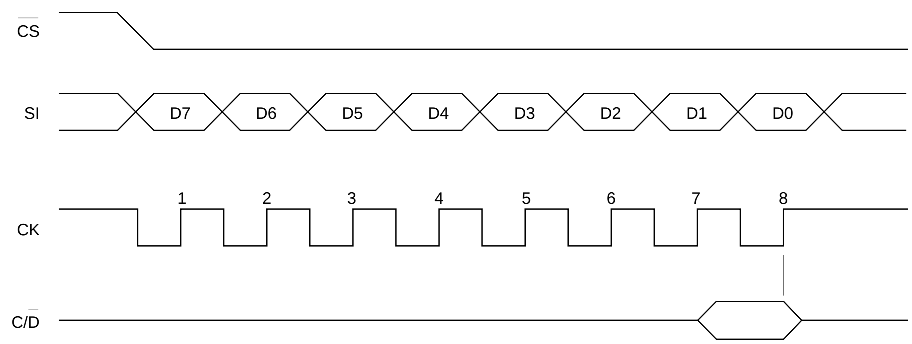


■ FUNCTIONAL DESCRIPTION

● Command/Data Register

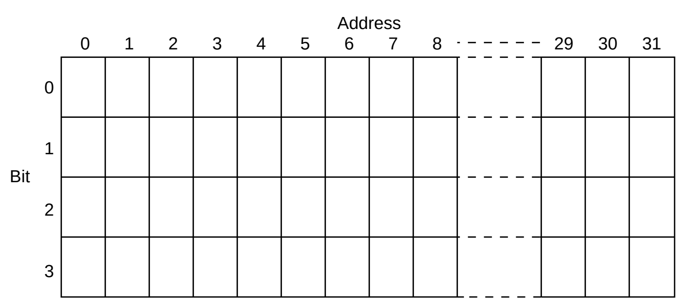
The command/data register comprises an 8-bit shift register and a 3-bit counter. The counter is reset and re-enabled on the falling edge of $\overline{CS}$. The CK counter is initialized when the built-in timing generator circuit (CR oscillating circuit) starts oscillating. The counter is incremented, and the serial input data is shifted into the register on the rising edge of CK. The data is input msb-first as shown in the following figure.

C/$\overline{D}$ is sampled, and the register data is latched into either the display data memory or the command decoder on every eighth rising edge of CK. C/$\overline{D}$ should be set HIGH when a command is input, and LOW, when display data is input.



● Display Data Memory

The format of the 32 × 4-bit memory is shown in the following figure.



Each 8-bit display data byte loaded from the command/data register is stored in two consecutive addresses as shown in the following figure. The upper four bits are stored at the location specified by the address counter, and the lower four bits, at the next location. The address counter is automatically incremented by two.

Bit 3			Bit 0
D7	D6	D5	D4

Current Address

Bit 3			Bit 0
D3	D2	D1	D0

Current Address + 1

A single 4-bit word can be written to memory using the Data Memory Write command as shown in the following figure. The lower four bits are stored at the location specified by the address counter. The address counter is automatically incremented by one.

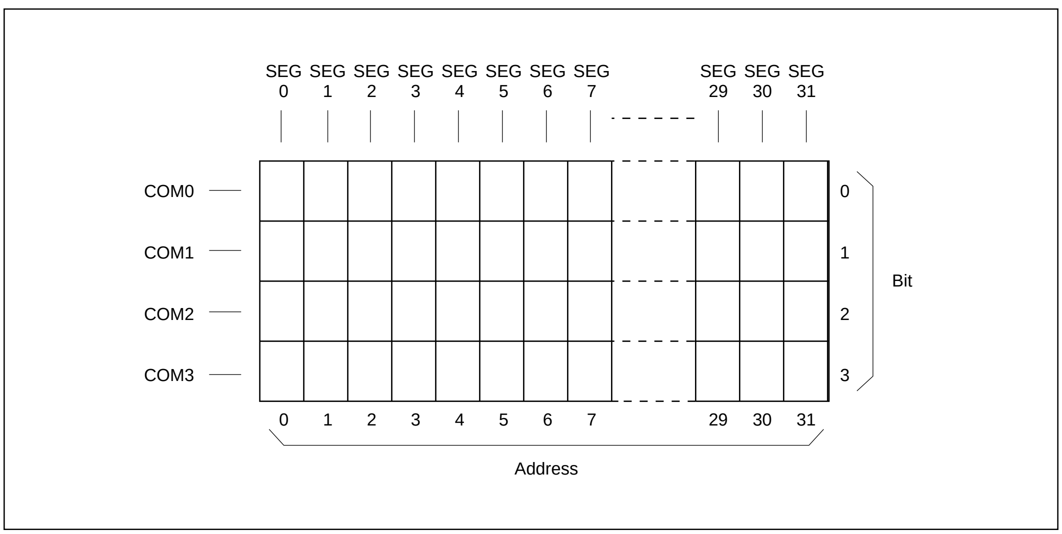
1	0	0	X	D3	D2	D1	D0

Note: x = don't care.

The display data memory address of the SED1511 is automatically incremented by 2 when 8-bit display data is stored.

Address 0 is automatically set when the built-in timing generating circuit (CR oscillating circuit) starts oscillating after power on.

Display memory data is output on SEG0 to SEG31 in synchronization with the COM0 to COM3 output scan. The correspondence between memory location and display position is shown in the following figure. When the data is 0, the segment is OFF, and when 1, ON.

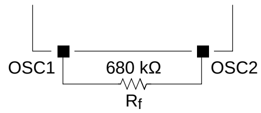


- **Address Counter**

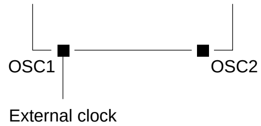
The 5-bit address counter is used to address display data memory. It is set by the Address Set command, and automatically increments when data is stored in the memory. The counter automatically resets to 0 when it increments past 31 as shown in the following figure.

- **Timing Generator**

A low-power oscillator can be constructed using an external feedback resistor as shown in the following figure.



Alternatively, an 18 kHz external clock can be input on OSC1, and OSC2 left open, as shown in the following figure.



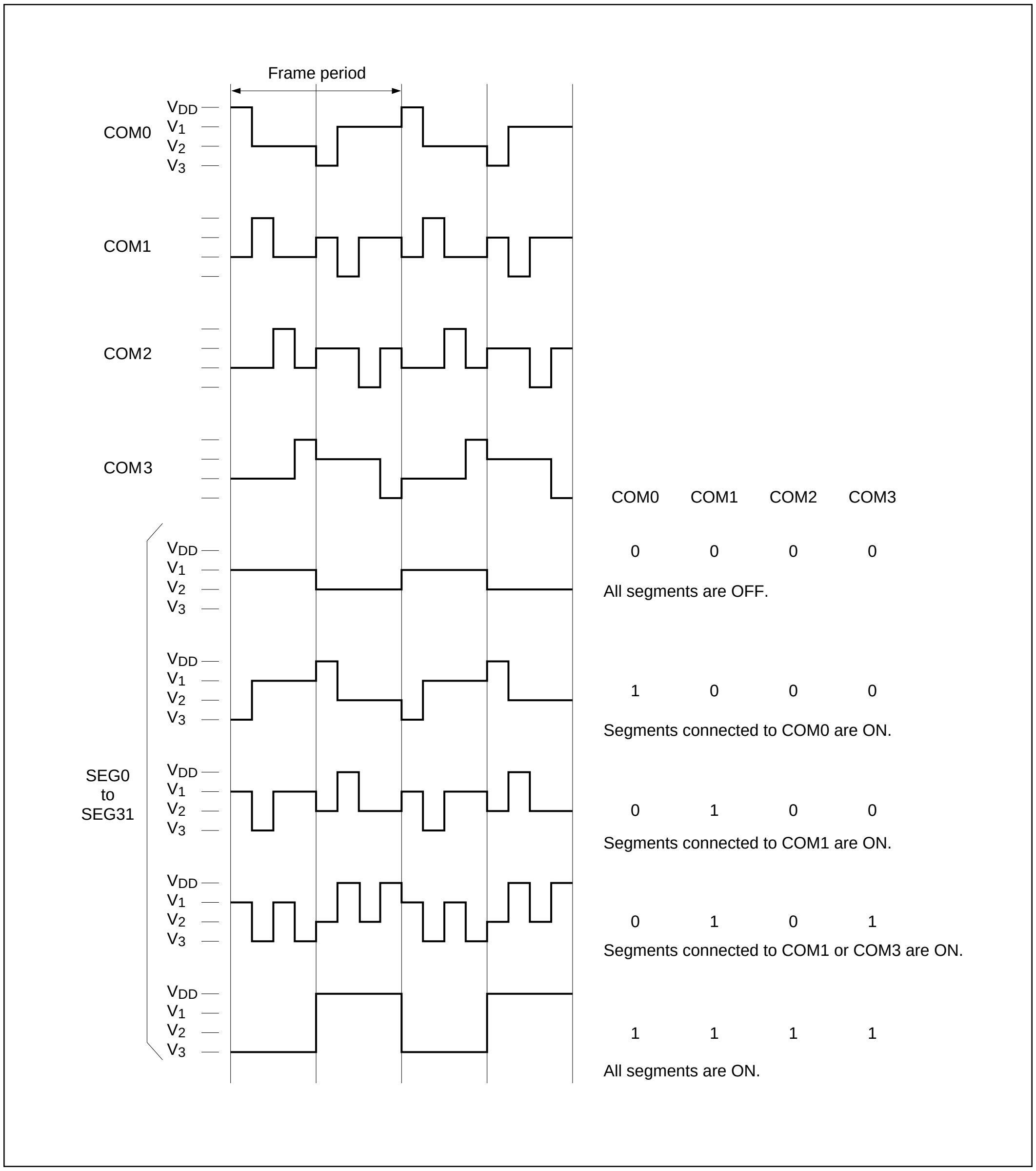
- **Common Counter**

The timing generator clock signal is frequency-divided by the common counter to generate both the common drive timing and the alternating frame timing.

- **Segment and Common Drivers**

The 32 segment drivers and the four common drivers are 4-level outputs that switch between V_{DD} and the V1, V2 and V3 LCD driver voltage levels.

The output states are determined by the display data values and the common counter as shown in the following figure. The outputs are used to drive a 1/3-bias, 1/4-duty LCD panel.


Frame period
COM0
COM1
COM2
COM3
VDD
V1
V2
V3
SEG0
to
SEG31
COM0 COM1 COM2 COM3
0 0 0 0
All segments are OFF.
1 0 0 0
Segments connected to COM0 are ON.
0 1 0 0
Segments connected to COM1 are ON.
0 1 0 1
Segments connected to COM1 or COM3 are ON.
1 1 1 1
All segments are ON.

● Commands

The SED1510F0C samples C/D on every eighth rising edge of CK. If C/D is HIGH, the command/data register contents are latched into the command decoder. The command decoder executes the following six commands.

Address Set

Set the address counter to the value specified by D0 to D4.

0	0	0	D4	D3	D2	D1	D0

Display ON

Turn all LCD segments ON. The display memory data is not affected.

0	0	1	X	X	X	X	X

Note: x = don’t care.

Display OFF

Turn all LCD segments OFF. The display memory data is not affected.

0	1	0	X	X	X	X	X

Note: x = don’t care.

Display Start

Return to normal display mode. The display memory data is output to the display.

0	1	1	X	X	X	X	X

Note: x = don’t care.

Memory Write

Store the data D0 to D3 at the location specified by the address counter. The address counter is automatically incremented by one. The other display memory locations are not affected.

1	0	0	X	D3	D2	D1	D0

Note: x = don’t care.

Reset

Reset the SED1510F0C. The SED1510F0C then enters normal operating mode, and the display turns OFF.

1	1	0	X	X	X	X	X

Note: x = don’t care.

■ APPLICATION NOTE

● Supply Voltages

In addition to V_{DD}, there are three LCD supply voltages: V1, V2 and V3. V3 is supplied externally, whereas V1 and V2 are generated internally. V1, V2 and V3 are given by the following equations:

$$V1 = V_{DD} – 1/3\ V_{LCD}$$
$$V2 = V_{DD} – 2/3\ V_{LCD}$$
$$V3 = V_{DD} – V_{LCD}$$

where V_{LCD} is the LCD drive voltage. The voltages must be such that $V_{DD} \geq V1 \geq V2 \geq V3$.

LCD supply voltage connections when the LCD drive supply is connected to V_{SS} are shown in Figure 1, below, and the connections when the drive supply is independent of V_{SS}, in Figure 2.

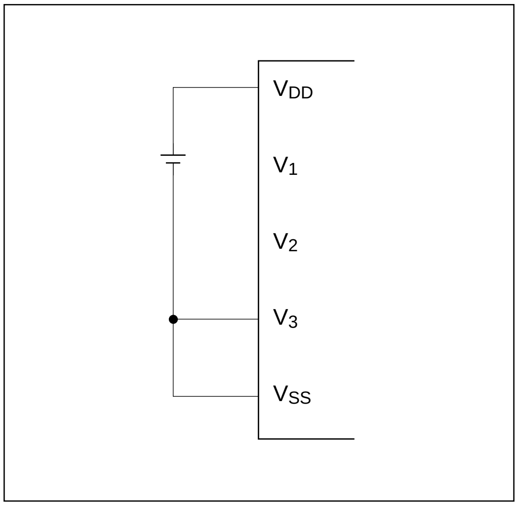


Figure 1. LCD drive supply connected to V_{SS}

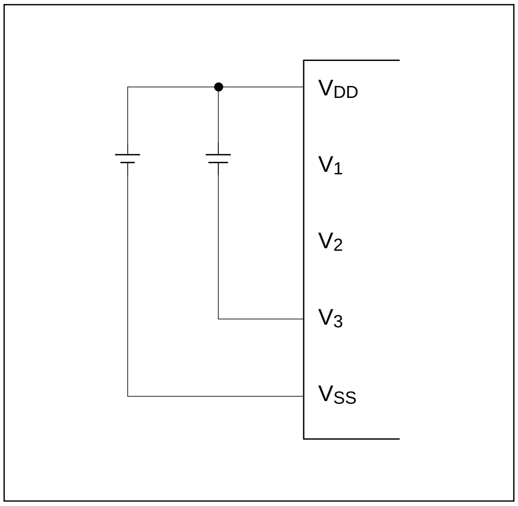
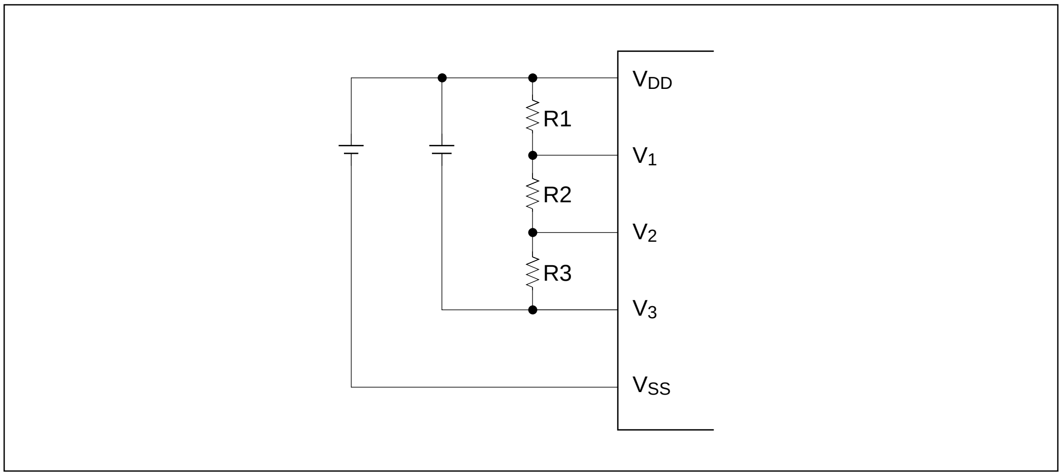
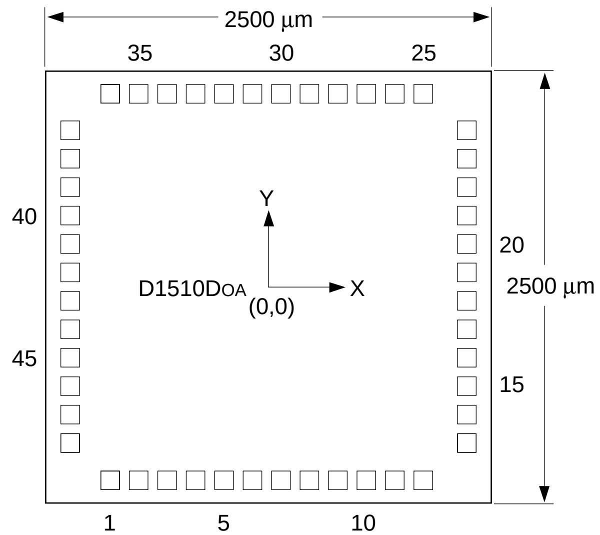


Figure 2. LCD drive supply not connected to V_{SS}

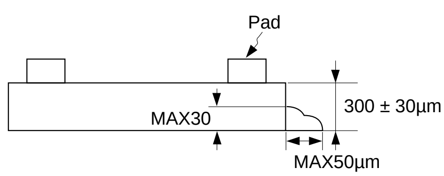
When there is a lot of distortion in the LCD drive waveforms, connect bleeder resistors as shown in the following figure.



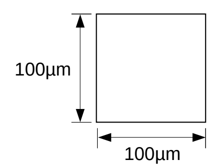
■ PAD LAYOUT AND COORDINATES (SED1510D0A)



- **Sectional Dimensions**



- **Size of Pad Opening**



- **Pad Coordinates**

unit: µm

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	OSC1	–898	–1091	25	SEG8	898	1091
2	OSC2	–738	–1091	26	SEG9	738	1091
3	V1	–578	–1091	27	SEG10	578	1091
4	V2	–418	–1091	28	SEG11	418	1091
5	V3	–258	–1091	29	SEG12	258	1091
6	V_{SS}	–98	–1091	30	SEG13	98	1091
7	V_{DD}	63	–1091	31	SEG14	–63	1091
8	CK	223	–1091	32	SEG15	–223	1091
9	SI	383	–1091	33	SEG16	–383	1091
10	NC	543	–1091	34	SEG17	–543	1091
11	NC	703	–1091	35	SEG18	–703	1091
12	COM0	863	–1091	36	SEG19	–863	1091
13	COM1	1091	–898	37	SEG20	–1091	898
14	COM2	1091	–738	38	SEG21	–1091	578
15	COM3	1091	–578	39	SEG22	–1091	578
16	VREG	1091	–418	40	SEG23	–1091	418
17	SEG0	1091	–258	41	SEG24	–1091	258
18	SEG1	1091	–98	42	SEG25	–1091	98
19	SEG2	1091	63	43	SEG26	–1091	–223
20	SEG3	1091	224	44	SEG27	–1091	–223
21	SEG4	1091	383	45	SEG28	–1091	–383
22	SEG5	1091	543	46	SEG29	–1091	–543
23	SEG6	1091	703	47	SEG30	–1091	–703
24	SEG7	1091	863	48	SEG31	–1091	–863

Note: The origin is the center of the chip. The chip size is 2,500 × 2,500.