SLA50000H SERIES HIGH DENSITY GATE ARRAY

DESCRIPTION

EPSON Electronics America, Inc.'s SLA50000H Series is a family of ultra high-speed VLSI CMOS gate array utilizing a 0.35µm "sea-of-gates" architecture. The SLA50000H products feature 5V tolerant I/O buffers.

- Ultra-high-speed, high density and low power consumption
- Low voltage operation: 3.3V and 2.0V
- Number of raw gates: 28,710 ~ 815,468 gates

FEATURES

- Process — 0.35µm 2/3/4 layer metalization CMOS process
- Integration — A maximum of 815,468 gates (2 input NAND gate equivalent)
- Operating Speed — Internal gates: 140 ps (3.3V Typ), 210 ps (2.0V Typ)
  (2-input pair NAND, F/O = 2, Typical wire load)
  Input buffer: 380 ps (5.0V Typ) Built-in level shifter is used.
  400 ps (3.3V Typ), 1.30 ns (2.0V Typ)
  (F/O = 2, Typical wire load)
  Output buffer: 2.12 ns (5.0V Typ) Built-in level shifter is used.
  2.02 ns (3.3 V Typ), 3.90 ns (2.0V Typ)
  (C_L = 15 pF)
- I/F Levels — Input/Output TTL/CMOS/LVTTL compatible
- Input Modes — TTL, CMOS, LVTTL, TTL Schmitt, CMOS Schmitt, LVTTL Schmitt, PCI
  Built-in pull-up and pull-down resistors can be usable.
  (2 types for each resistor value)
- Output Modes — Normal, 3-state, bi-directional, PCI
- Output Drive — I_{OL} = 0.1, 1, 3, 8, 12, 24 mA selectable
  (Built-in level shifter is used at 5.0V)
  I_{OL} = 0.1, 1, 2, 6, 12 mA selectable (at 3.3V)
  I_{OL} = 0.05, 0.3, 0.6, 2, 4 mA selectable (at 2.0V)
- RAM — Asynchronous 1-port, asynchronous 2-port
- Dual Power — Operation supported by using level-shifter circuit
  Internal logic: Operation supported by low voltage
  I/O Buffer: Built-in interfaces of both high and low voltages possible
- Operation possible at $V_{DD} = 2.0 \pm 0.2V$

LINE UP

The SLA50000H Series comprises 11 types of masters, from which the customer is able to select the master most suitable.

Master	Total BC (Raw Gates)	Number of Pads	Number of Columns (X)	Number of Rows (Y)	Cell Utilization Ratio (U)*1		
					2-layer metal	3-layer metal	4-layer metal
SLA5028/502T/502Q	28710	88	319	90	50%	88%	95%
SLA5075/507T/507Q	75774	144	519	146	47%	85%	95%
SLA5099/509T/509Q	99198	168	594	167	47%	85%	95%
SLA5125/512T/512Q	125772	188	669	188	45%	80%	95%
SLA5177/517T/517Q	177062	224	794	223	45%	75%	95%
SLA5250/525T/525Q	250160	264	944	265	45%	75%	95%
SLA5335/533T/533Q	335858	308	1094	307	43%	75%	95%
SLA5442/544T/544Q	442112	352	1256	352	40%	70%	90%
SLA5506/550T/550Q	506688	376	1344	377	40%	70%	90%
SLA5668/566T/566Q	668552	432	1544	433	40%	70%	90%
SLA5815/581T/581Q	815468	480	1706	478	40%	70%	90%

NOTE: *1: This is the value when there are no cells, such as RAM cells. The cell use efficiency is dependent not only on the scope of the circuits, but also on the number of signals, the number of branches per signal, etc.; thus, use the values in this table only as an estimate

ELECTRICAL CHARACTERISTICS AND SPECIFICATIONS

Absolute Maximum Ratings (For Single Power Supply):

(V_{ss} = 0V)

Item	Symbol	Limits	Unit
Power Supply Voltage	V_{DD}	-0.3 to 4.0	V
Input Voltage	V_I	-0.3 to V_{DD} + 0.5 *1	V
Output Voltage	V_O	-0.3 to V_{DD} + 0.5 *1	V
Output Current/Pin	I_{OUT}	± 30	mA
Storage Temperature	T_{STG}	-65 to 150	°C

*1: Possible to use from -0.3V to 7.5V of I/O buffer voltage in the open-drain systems and input buffer in the IDC and IDH systems.

Absolute Maximum Ratings (For Dual Power Supplies):

(V_{ss} = 0V)

Item	Symbol	Limits	Unit
Power Supply Voltage	HV_{DD}	-0.3 to 7.0	V
	LV_{DD}	-0.3 to 4.0	V
Input Voltage	HV_I	-0.3 to HV_{DD} + 0.5 *1	V
	LV_I	-0.3 to LV_{DD} + 0.5 *1	V
Output Voltage	HV_O	-0.3 to HV_{DD} + 0.5 *1	V
	LV_O	-0.3 to LV_{DD} + 0.5 *1	V
Output Current/Pin	I_{OUT}	± 30 (± 50 *2)	mA
Storage Temperature	T_{STG}	-65 to 150	°C

**1: Possible to use from -0.3V to 7.5V of I/O buffer voltage in the open-drain systems and input buffer in the IDC and IDH systems.

*2: Possible to use for 24mA of output buffer.

Recommended Operating Conditions (For Single Power Supplies):

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3.00	3.30	3.60	V
Input Voltage	V_I	V_{SS}	--	V_{DD} *1	V
Ambient Temperature	T_a	0 -40	25 25	70 *2 85 *3	°C
Normal Input for Rising Edge Input	t_{ri}	--	--	50	ns
Normal Input for Falling Edge Input	t_{fi}	--	--	50	ns
Schmitt Input for Rising Edge Input	t_{ri}	--	--	5	ms
Schmitt Input for Falling Edge Input	t_{fi}	--	--	5	ms

*1: Possible to use 5.25 or 5.50V of I/O buffer in the open-drain systems and input buffer in the IDC and IDH systems.
*2: The ambient temperature range is recommended for T_j = 0 to 80°C
*3: The ambient temperature range is recommended for T_j = -40 to 125°C

Recommended Operating Conditions (For Single Power Supplies):

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	1.80	2.00	2.20	V
Input Voltage	V_I	V_{SS}	--	V_{DD} *1	V
Ambient Temperature	T_a	0 -40	25 25	70 *2 85 *3	°C
Normal Input for Rising Edge Input	t_{ri}	--	--	100	ns
Normal Input for Falling Edge Input	t_{fi}	--	--	100	ns
Schmitt Input for Rising Edge Input	t_{ri}	--	--	10	ms
Schmitt Input for Falling Edge Input	t_{fi}	--	--	10	ms

*1: Possible to use 5.25 or 5.50V of I/O buffer in the open-drain systems and input buffer in the IDC and IDH systems.
*2: The ambient temperature range is recommended for T_j = 0 to 80°C
*3: The ambient temperature range is recommended for T_j = -40 to 125°C

Recommended Operating Conditions (For Dual Power Supplies):

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (High Voltage)	HV_{DD}	4.75 4.50	5.00 5.00	5.25 5.50	V
Power Supply Voltage (Low Voltage)	LV_{DD}	3.00	3.30	3.60	V
Input Voltage	HV_I	V_{SS}	--	HV_{DD}	V
	LV_I	V_{SS}	--	LV_{DD} *1	
Ambient Temperature	T_a	0 -40	25 25	70 *2 85 *3	°C
Normal Input for Rising Edge Input	tri	--	--	50	ns
Normal Input for Falling Edge Input	tri	--	--	50	ns
Schmitt Input for Rising Edge Input	tri	--	--	5	ms
Schmitt Input for Falling Edge Input	tri	--	--	5	ms

*1: Possible to use 5.25 or 5.50V of I/O buffer in the open-drain systems and input buffer in the LIDC and LIDH systems.
*2: The ambient temperature range is recommended for T_j = 0 to 80°C
*3: The ambient temperature range is recommended for T_j = -40 to 125°C

Recommended Operating Conditions (For Dual Power Supplies):

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (High Voltage)	HV_{DD}	3.00	3.30	3.60	V
Power Supply Voltage (Low Voltage)	LV_{DD}	1.80	2.00	2.20	V
Input Voltage	HV_I	V_{SS}	--	HV_{DD}	V
	LV_I	V_{SS}	--	LV_{DD}	
Ambient Temperature	T_a	0 -40	25 25	70 *1 85 *2	°C
Normal Input for Rising Edge Input	H_{tri}	--	--	50	ns
	L_{tri}	--	--	100	
Normal Input for Falling Edge Input	H_{tfi}	--	--	50	ns
	L_{tfi}	--	--	100	
Schmitt Input for Rising Edge Input	H_{tri}	--	--	5	ms
	L_{tri}	--	--	10	
Schmitt Input for Falling Edge Input	H_{tfi}	--	--	5	ms
	L_{tfi}	--	--	10	

*1: Possible to use 5.25 or 5.50V of I/O buffer in the open-drain systems and input buffer in the LIDC and LIDH systems or HIDC and HIDH systems.
*2: The ambient temperature range is recommended for T_j = 0 to 80°C
*3: The ambient temperature range is recommended for T_j = -40 to 125°C

Electrical Characteristics of the SLA50000H Series:

(V_{DD} = 5.0V, V_{SS} = 0V, T_a = -40 to 85°C)

Item	Symbol	Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	--		-1	--	1	µA
Off State Leakage Current	I_{OZ}	--		-1	--	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1mA (Type S), -1mA (Type M), -3mA (Type 1), -8mA (Type 2), -12mA (Type 3, Type 4) V_{DD} = Min		HV_{DD} -0.4	--	--	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1mA (Type S), 1mA (Type M), 3mA (Type 1), 8mA (Type 2), 12mA (Type 3), 24mA (Type 4) V_{DD} = Min		--	--	0.4	V
High Level Input Voltage	V_{IH1}	CMOS Level, HV_{DD} = Max		3.5	--	--	V
Low Level Input Voltage	V_{IL1}	CMOS Level, HV_{DD} = Min		--	--	1.0	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		2.0	--	4.0	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.8	--	3.1	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0.3	--	--	V
High Level Input Voltage	V_{IH2}	TTL Level, HV_{DD} = Max		2.0	--	--	V
Low Level Input Voltage	V_{IL2}	TTL Level, HV_{DD} = Min		--	--	0.8	V
High Level Input Voltage	V_{T2+}	TTL Schmitt		1.2	--	2.4	V
Low Level Input Voltage	V_{T2-}	TTL Schmitt		0.6	--	1.8	V
Hysteresis Voltage	V_{H2}	TTL Schmitt		0.1	--	--	V
High Level Input Voltage	V_{IH3}	PCI Level, HV_{DD} = Max		2.0	--	--	V
Low Level Input Voltage	V_{IL3}	PCI Level, HV_{DD} = Min		--	--	0.8	V
High Level Output Current	I_{OH3}	PCI Response, V_{OH} = 1.4V, HV_{DD} = Min V_{OH} = 3.1V, HV_{DD} = Max		 -44 --	 -- --	 -- -142	 mA mA
Low Level Output Current	I_{OL3}	PCI Response V_{OH} = 2.20V, HV_{DD} = Min V_{OL} = 0.71V, HV_{DD} = Max		 95 --	 -- --	 -- 206	 mA mA
Pull-up Resistance*	R_{PU}	V_I = 0V	Type 1	30	60	(120) 144	KΩ
			Type 2	60	120	(240) 288	
Pull-down Resistance*	R_{PD}	V_I = V_{DD}	Type 1	30	60	(120) 144	KΩ
			Type 2	60	120	(240) 288	
High Level Maintenance Current	I_{BHH}	Bus Hold Response, (TTL)	V_{IN} = 2.0V, HV_{DD} = Min	--	--	-80	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response, (TTL)	V_{IN} = 0.8V, HV_{DD} = Min	--	--	33	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response, (TTL)	V_{IN} = 0.8V, HV_{DD} = Max	-550	--	--	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response, (TTL)	V_{IN} = 2.0V, HV_{DD} = Max	330	--	--	µA
Input Terminal Capacitance	C_I	f = 1Mhz, V_{DD} = 0V		--	--	10	pF
Output Terminal Capacitance	C_O	f = 1Mhz, V_{DD} = 0V		--	--	10	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1Mhz, V_{DD} = 0V		--	--	10	pF

* The values in parentheses are for the case of T_a = 0 to 70°C.

Electrical Characteristics of the SLA50000H Series:

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_a = -40 to 85°C)

Item	Symbol	Conditions		Min	Typ	Max	Unit
Quiescent Current*	I_{DDS}	Quiescent Conditions		--	--	170	µA
Input Leakage Current	I_{LI}	--		-1	--	1	µA
Off State Leakage Current	I_{OZ}	--		-1	--	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1mA (Type S), -1mA (Type M), -2mA (Type 1), -6mA (Type 2), -12mA (Type 3, Type 4) V_{DD} = Min		V_{DD} -0.4	--	--	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1mA (Type S), 1mA (Type M), 2mA (Type 1), 6mA (Type 2), 12mA (Type 3), 24mA (Type 4) V_{DD} = Min		--	--	0.4	V
High Level Input Voltage	V_{IH1}	LVTTL Level, V_{DD} = Max		2.0	--	--	V
Low Level Input Voltage	V_{IL1}	LVTTL Level, V_{DD} = Min		--	--	0.8	V
High Level Input Voltage	V_{T1+}	LVTTL Schmitt		1.1	--	2.4	V
Low Level Input Voltage	V_{T1-}	LVTTL Schmitt		0.6	--	1.8	V
Hysteresis Voltage	V_{H1}	LVTTL Schmitt		0.1	--	--	V
High Level Input Voltage	V_{IH3}	PCI Level, V_{DD} = Max		1.71	--	--	V
Low Level Input Voltage	V_{IL3}	PCI Level, V_{DD} = Min		--	--	0.98	V
High Level Output Current	I_{OH3}	PCI Response, V_{OH} = 0.90V, V_{DD} = Min V_{OH} = 2.52V, V_{DD} = Max		 -36 --	 -- --	 -- -115	 mA mA
Low Level Output Current	I_{OL3}	PCI Response V_{OH} = 1.80V, V_{DD} = Min V_{OL} = 2.52V, V_{DD} = Max		 48 --	 -- --	 -- 137	 mA mA
Pull-up Resistance**	R_{PU}	V_I = 0V	Type 1	20	50	(100) 120	KΩ
			Type 2	40	100	(200) 240	
Pull-down Resistance**	R_{PD}	V_I = V_{DD}	Type 1	20	50	(100) 120	KΩ
			Type 2	40	100	(200) 240	
High Level Maintenance Current	I_{BHH}	Bus Hold Response, V_{IN} = 2.0V, V_{DD} = Min		--	--	-20	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response, V_{IN} = 0.8V, V_{DD} = Min		--	--	17	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response, V_{IN} = 0.8V, V_{DD} = Max		-350	--	--	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response, V_{IN} = 2.0V, V_{DD} = Max		210	--	--	µA
Input Terminal Capacitance	C_I	f = 1Mhz, V_{DD} = 0V		--	--	10	pF
Output Terminal Capacitance	C_O	f = 1Mhz, V_{DD} = 0V		--	--	10	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1Mhz, V_{DD} = 0V		--	--	10	pF

* The quiescent current is a typical value (T_j=85°C) for each master.

** The values in parentheses are for the case of T_a = 0 to 70°C.

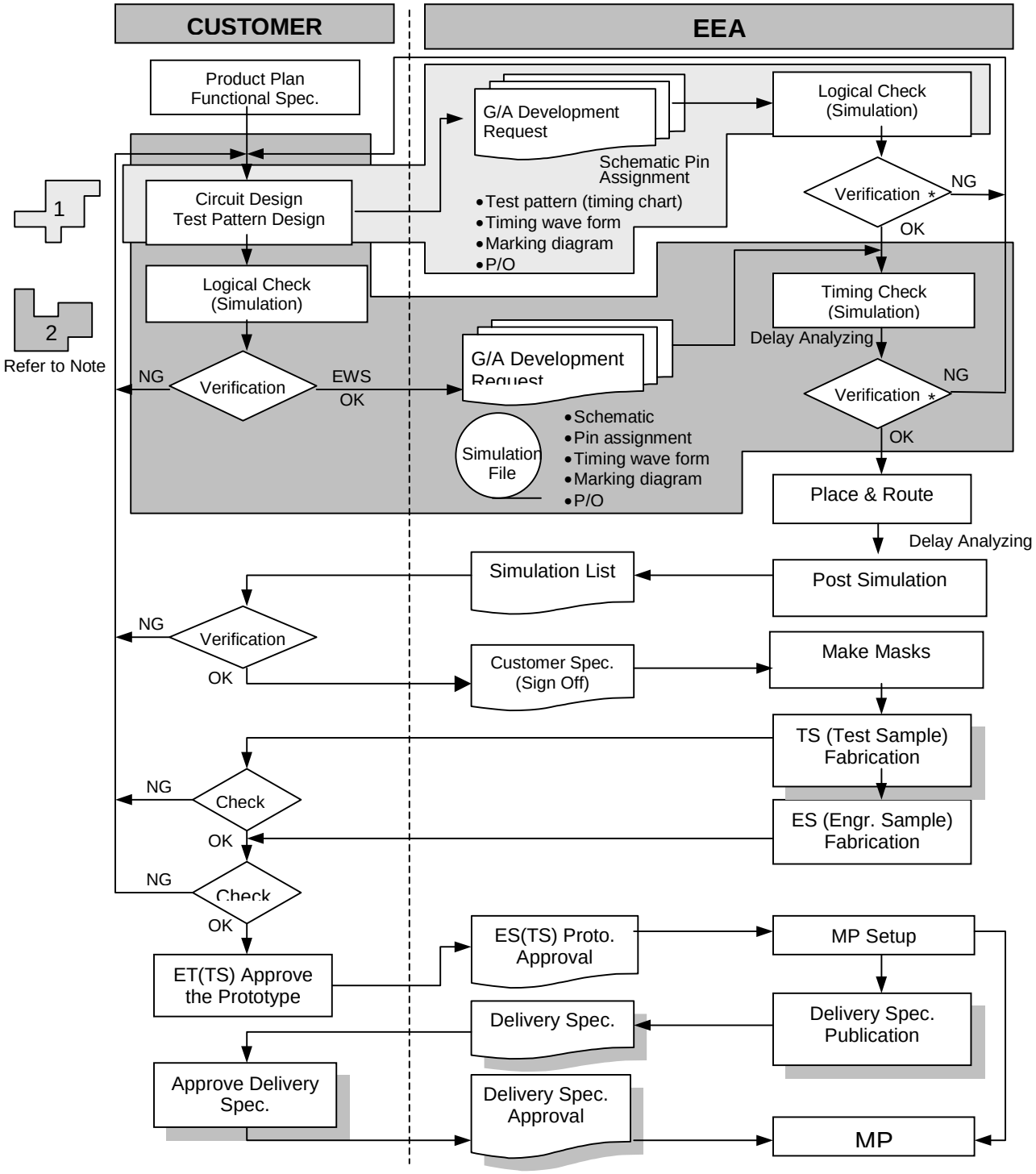
Electrical Characteristics of the SLA50000H Series:

(V_{DD} = 2.0V ± 0.2V, V_{SS} = 0V, T_a = -40 to 85°C)

Item	Symbol	Conditions		Min	Typ	Max	Unit
Quiescent Current*	I_{DDS}	Quiescent Conditions		--	--	150	µA
Input Leakage Current	I_{LI}	--		-1	--	1	µA
Off State Leakage Current	I_{OZ}	--		-1	--	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.05mA (Type S), -0.3mA (Type M), -0.6mA (Type 1), -2mA (Type 2), -4mA (Type 3, Type 4) V_{DD} = Min		V_{DD} -0.2	--	--	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.05mA (Type S), 0.3mA (Type M), 0.6mA (Type 1), 2mA (Type 2), 4mA (Type 3), 8mA (Type 4) V_{DD} = Min		--	--	0.2	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} = Max		1.6	--	--	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} = Min		--	--	0.3	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		0.4	--	1.6	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.3	--	1.4	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0	--	--	V
Pull-up Resistance	R_{PU}	V_I = 0V	Type 1	30	120	300	KΩ
			Type 2	60	240	600	
Pull-down Resistance	R_{PD}	V_I = V_{DD}	Type 1	30	120	300	KΩ
			Type 2	60	240	600	
High Level Maintenance Current	I_{BHH}	Bus Hold Response, V_{IN} = 1.6V, V_{DD} = Min		--	--	-2	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response, V_{IN} = 0.3V, V_{DD} = Min		--	--	2	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response, V_{IN} = 0.3V, V_{DD} = Max		-100	--	--	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response, V_{IN} = 1.6V, V_{DD} = Max		100	--	--	µA
Input Terminal Capacitance	C_I	f = 1Mhz, V_{DD} = 0V		--	--	10	pF
Output Terminal Capacitance	C_O	f = 1Mhz, V_{DD} = 0V		--	--	10	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1Mhz, V_{DD} = 0V		--	--	10	pF

* The quiescent current is a typical value (T_j=85°C) for each master.

GATE ARRAY DEVELOPMENT FLOW



* Jobs are done by customer and EEA engineer. Steps in shadowed boxes are based on customer's requirement.

NOTE: When the customer performs all tasks to the point of logical simulations and delay simulations on engineering workstations, etc., the route taken is (2, Joint Design). When EEA performs the logical simulations, the route taken is (1, Turnkey Design).

EEA CUSTOMER ENGINEERING

To help customers implement their design of EEA ASIC's, we offer training at our design centers and at customer sites when required.

When a design is started, an EEA engineer is assigned to the project and will remain with the project through its completion. EEA engineers will work with the customer on design, software and other technical issues. When the design files are transferred to EEA, the assigned engineer will verify the design's integrity and prepare it for place and route. The EEA Customer Engineering Group provides all technical customer-support services including:

- Pre-Sale Technical Support
- Customer Training
- Design Assistance
- Custom Cell Development
- Place and Route
- Scan Insertion and ATPG
- Netlist Conversion and Synthesis
- Software Documentation
- Simulation Support
- Turnkey Design
- Design Verification
- Static Timing Analysis
- JTAG Insertion
- Test Vector Conversion

EDA/CAE SUPPORT

- Schematic Capture
  - Viewlogic (Synopsys): Viewdraw
  - EEA: Auklet (ECS)
- Synthesis
  - Synopsys: DesignCompiler
  - Exemplar Logic: Leonardo
- Simulation
  - Cadence: Verilog-XL
  - Synopsys: VSS (VHDL)
  - Avant!: Polaris (Purespeed)
  - Viewlogic (Synopsys): Viewsim
  - Modeltech: V-System (VHDL)
- DFT
  - Synopsys: TestCompiler+
  - Viewlogic (Synopsys): TestGen (Sunrise)
- Place & Route
  - Cadence: GateEnsemble
  - Avant!: Aquarius-GA (Apollo)
- Delay Calculation (Post-Route)
  - EEA: Peacock (EXDT)

EDA/CAE SUPPORT (continued)

- Static Timing
  - Synopsys: PrimeTime (DesignTime)
  - Viewlogic (Synopsys): Motive

- Layout Verification
  - Cadence: Dracula/LVS

NOTICE

For additional information about EEA ASIC products and services, or to discuss a solution tailored to your specific requirements, call your local EEA sales office or contact the factory.

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