EPSON

SLA35000 Series

High Density Gate Array

- Super-high-density gate array
- Operates on 3.0/3.3/5.0V power sources
- Number of gates: 41 to 162k gates (sea of gates)

■ DESCRIPTION

The SLA 35000 series are Sea-of-gate type CMOS gate arrays adopting a super-high-density architecture and having a significantly increased number of gates per chip than their equivalent processing equipment.
This series are ideal for midsize systems having a relatively small number of I/Os and provide high cost performance.
There are four models ranging from 41,417 to 161,841 gates which can be operated on any power source of 3.0, 3.3 or 5.0V, enabling them to be used in a variety of low-voltage applied fields.
Their demands are approximately 30% smaller (0.77µ W/MHz/BC when the internal cell is 3.0V) than those of their equivalent SLA 30000 series. This allows them to be used more easily in high density circuits to be mounted on small packages and employed for various applications such as for image processing and in communication equipment.
To develop high-speed/high-density circuits in a shorter period of time, the series enable diverse design techniques to be employed during development such as high accuracy simulation of wiring resistance and blunted waveform in addition to the conventional wiring capacity components, and provide a new layout tool for reducing clock skew.

■ FEATURES

- Super-high density (adopting 0.6µm silicon gate CMOS with 3-metal layer)
- High-speed operation (operation delay of internal gate = 0.4ns at 3.3V, 2-input power NAND standard)
- Selectable supply voltage: 5.0V, 3.3V, and 3.0V
- Low power consumption (0.77µW/MHz/BC when internal cell = 3.0V)
- Output drivability (I_{OL} = 1, 4, 8, 12 mA when 5.0V, I_{OL} = 500µ, 2, 4, 6mA when 3.3V)
- On-chip RAM available

■ PRODUCT LINEUP

Master		SLA3504	SLA3506	SLA3509	SLA3516
Total BCs (Raw Gates)		41,417	64,320	95,760	161,841
Usable Bcs		26,921	38,592	52,668	80,920
Number of PADs		110	130	162	210
Propagation Delay	Internal Gates	tpd = 0.30ns (standard at 5.0V), tpd = 0.40ns (standard at 3.3V)			
	Input Buffers	tpd = 0.48ns (standard at 5.0V), tpd = 0.63ns (standard at 3.3V)			
	Output Buffers	tpd = 2.08ns (standard at 5.0V), tpd = 2.86ns (standard at 3.3V) CL = 50pF			
I/O Level		CMOS, TTL			
Input Mode		TTL, CMOS, Pull-up/Pull-down			
Output Mode		Normal, 3-state, Bi-directional			

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Item	Symbol	Rating	Unit
Power voltage	V_{DD}	–0.3 to 6.0	V
Input voltage	V_I	–0.3 to V_{DD}+0.5	V
Output voltage	V_O	–0.3 to V_{DD}+0.5	V
Output current/pin	I_{OUT}	±25 (±50*1)	mA
Storage temperature	Tstg	–65 to 150	°C

*1: For cell of 24mA output current

■ RECOMMENDED OPERATING CONDITION

● Single power supply

Item	Symbol	Min.	Typ.	Max.	Unit
Power voltage	V_{DD}	2.70 3.00 4.75 4.50	3.00 3.30 5.00 5.00	3.30 3.60 5.25 5.50	V
Input voltage	V_I	V_{SS}	–	V_{DD}	V
Operating temperature	Topr	0 –40	25 25	70 85	°C °C
Normal input during input rise time	tri	–	–	50	ns
Normal input during input fall time	tfi	–	–	50	ns
Schmitt input during input rise time	tri	–	–	5	ms
Schmitt input during input fall time	tfi	–	–	5	ms

■ ELECTRICAL CHARACTERISTICS (V_{DD}=5V)

(V_{DD} = 5V, V_{SS} = 0V, Ta = –40 to 85°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Stand-by current *	I_{DDS}	Stop position		–	–	400	µA
Input leakage current	I_{LI}	–		–1	–	1	µA
Off-state leakage current	I_{OZ}	–		–1	–	1	µA
High level output voltage	V_{OH}	I_{OH} = –1mA (Type M), –4mA (Type 1), –8mA (Type 2), –12mA (Type 3) V_{DD} = Min.		V_{DD} –4	–	–	V
Low level output voltage	V_{OL}	I_{OL} = 1mA (Type M), 4mA (Type 1), 8mA (Type 2), 12mA (Type 3) V_{DD} = Min.		–	–	0.4	V
High level input voltage	V_{IH1}	CMOS level, V_{DD} = Max.		3.5	–	–	V
Low level input voltage	V_{IL1}	CMOS level, V_{DD} = Min.		–	–	1.0	V
High level input voltage	V_{T1+}	CMOS Schmitt, V_{DD} = 5.0V		–	–	4.0	V
Low level input voltage	V_{T1-}	CMOS Schmitt, V_{DD} = 5.0V		0.8	–	–	V
Hysterisis voltage	V_{H1}	CMOS Schmitt, V_{DD} = 5.0V		0.3	–	–	V
High level input voltage	V_{IH2}	TTL level, V_{DD} = Max.		2.0	–	–	V
Low level input voltage	V_{IL2}	TTL level, V_{DD} = Min.		–	–	0.8	V
High level input voltage	V_{T2+}	TTL Schmitt, V_{DD} = 5.0V		–	–	2.4	V
Low level input voltage	V_{T2-}	TTL Schmitt, V_{DD} = 5.0V		0.6	–	–	V
Hysterisis voltage	V_{H2}	TTL Schmitt, V_{DD} = 5.0V		0.1	–	–	V
Pull-up resistor	R_{PU}	V_I = 0V	Type 1	25	50	100	KΩ
			Type 2	50	100	200	
Pull-down resistor	R_{PD}	V_I = V_{DD}	Type 1	25	50	100	KΩ
			Type 2	50	100	200	
Input pin capacitance	C_I	f = 1MHz, V_{DD} = 0V		–	–	12	pF
Output pin capacitance	C_O	f = 1MHz, V_{DD} = 0V		–	–	12	pF
I/O pin capacitance	C_{IO}	f = 1MHz, V_{DD} = 0V		–	–	12	pF

* Stand by current is a representative value of eresy series

■ ELECTRICAL CHARACTERISTICS (V_{DD}=3V)

(V_{DD} = 3V±0.3V, V_{SS} = 0V, Ta = –40 to 85°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Stand-by current*	I_{DDS}	Stop position		–	–	500	µA
Input leakage current	I_{LI}	–		–1	–	1	µA
Off-state leakage current	I_{OZ}	–		–1	–	1	µA
High level output voltage	V_{OH}	I_{OH} = –0.5mA (Type M), –1.8mA (Type 1), –3.5mA (Type 2), –5mA (Type 3) V_{DD} = Min.		V_{DD} –0.3	–	–	V
Low level output voltage	V_{OL}	I_{OL} = 0.5mA (Type M), 1.8mA (Type 1), 3.5mA (Type 2), 5mA (Type 3) V_{DD} = Min.		–	–	0.3	V
High level input voltage	V_{IH1}	CMOS level, V_{DD} = Max.		2.0	–	–	V
Low level input voltage	V_{IL1}	CMOS level, V_{DD} = Min.		–	–	0.8	V
High level input voltage	V_{T1+}	CMOS Schmitt, V_{DD} = 3.0V		–	–	2.3	V
Low level input voltage	V_{T1-}	CMOS Schmitt, V_{DD} = 3.0V		0.5	–	–	V
Hysterisis voltage	V_{H1}	CMOS Schmitt, V_{DD} = 3.0V		0.1	–	–	V
Pull-up resistor	R_{PU}	V_I = 0V	Type 1	50	100	200	KΩ
			Type 2	100	200	400	
Pull-down resistor	R_{PD}	V_O = V_{DD}	Type 1	50	100	200	KΩ
			Type 2	100	200	400	
Input pin capacitance	C_I	f = 1MHz, V_{DD} = 0V		–	–	12	pF
Output pin capacitance	C_O	f = 1MHz, V_{DD} = 0V		–	–	12	pF
I/O pin capacitance	C_{IO}	f = 1MHz, V_{DD} = 0V		–	–	12	pF

* Stand by current is a representative value of eresy series

■ ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V)

(V_{DD} = 3.3V±0.3V, V_{SS} = 0V, Ta = –40 to 85°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Stand-by current*	I_{DDS}	Stop position		–	–	500	µA
Input leakage current	I_{LI}	–		–1	–	1	µA
Off-state leakage current	I_{OZ}	–		–1	–	1	µA
High level output voltage	V_{OH}	I_{OH} = –0.5mA (Type M), –2mA (Type 1), –4mA (Type 2), –6mA (Type 3) V_{DD} = Min.		V_{DD} –0.3	–	–	V
Low level output voltage	V_{OL}	I_{OL} = 0.5mA (Type M), 2mA (Type 1), 4mA (Type 2), 6mA (Type 3) V_{DD} = Min.		–	–	0.3	V
High level input voltage	V_{IH1}	CMOS level, V_{DD} = Max.		2.2	–	–	V
Low level input voltage	V_{IL1}	CMOS level, V_{DD} = Min.		–	–	0.8	V
High level input voltage	V_{T1+}	CMOS Schmitt, V_{DD} = 3.3V		–	–	2.4	V
Low level input voltage	V_{T1-}	CMOS Schmitt, V_{DD} = 3.3V		0.6	–	–	V
Hysterisis voltage	V_{H1}	CMOS Schmitt, V_{DD} = 3.3V		0.1	–	–	V
Pull-up resistor	R_{PU}	V_I = 0V	Type 1	45	90	180	KΩ
			Type 2	90	180	360	
Pull-down resistor	R_{PD}	V_I = V_{DD}	Type 1	45	90	180	KΩ
			Type 2	90	180	360	
Input pin capacitance	C_I	f = 1MHz, V_{DD} = 0V		–	–	12	pF
Output pin capacitance	C_O	f = 1MHz, V_{DD} = 0V		–	–	12	pF
I/O pin capacitance	C_{IO}	f = 1MHz, V_{DD} = 0V		–	–	12	pF

* Stand by current is a representative value of eresy series

■ PERFORMANCE CURVES (V_{DD}=5V)

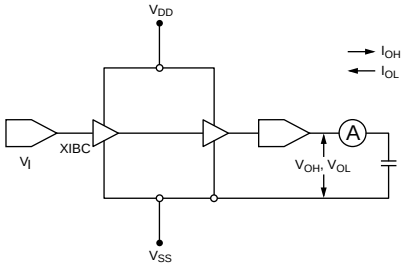
● Output Current Characteristics (5.0V±10%)

TYPE number	Output current	
	I_{OH} (mA)	I_{OL} (mA)
TYPE M	-1	1
TYPE 1	-4	4
TYPE 2	-8	8
TYPE 3	-12	12

The alphanumerics of the *TYPE (M, 1-3) indicate the output cell names (xx * x).**

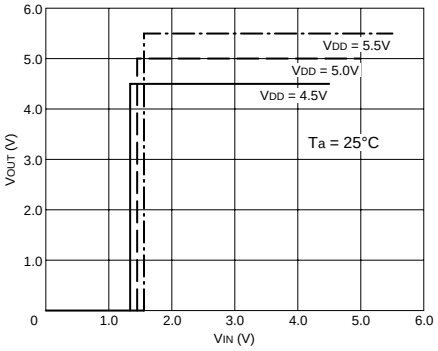
Example: XUO3 Å® Indicates TYPE3

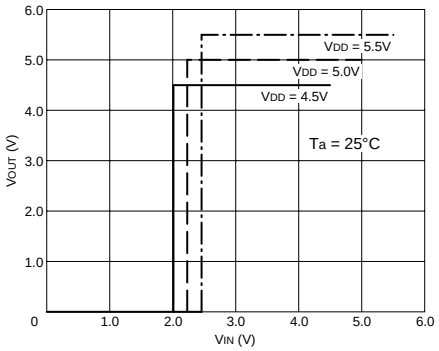
● Measurement Circuit



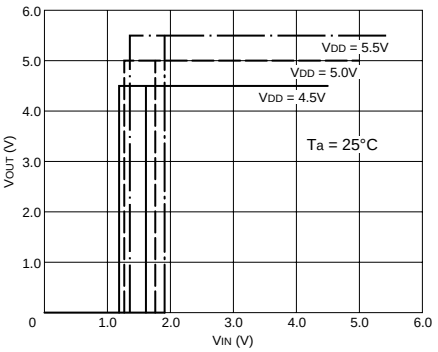
● Output Buffer Characteristics (5V±10%)

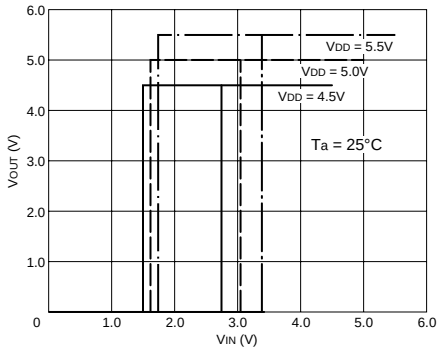
Standard Type





Schmitt – Trigger cell

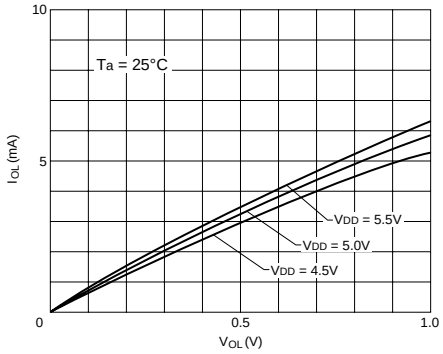




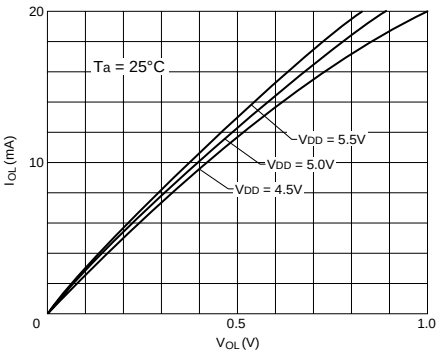
● Output Driver Characteristics

Low level output current

TYPE M



TYPE 1



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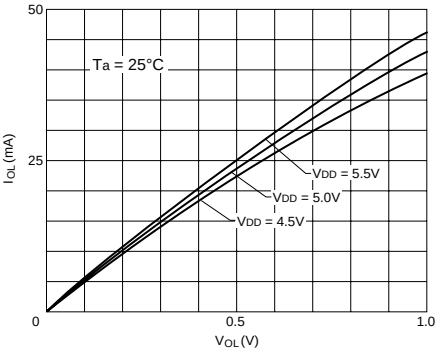
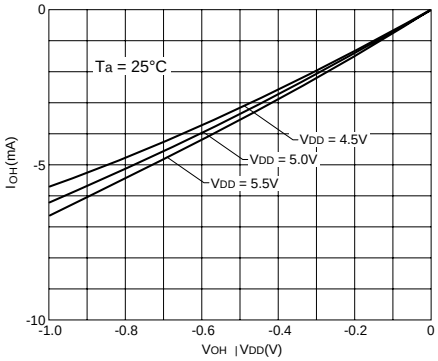
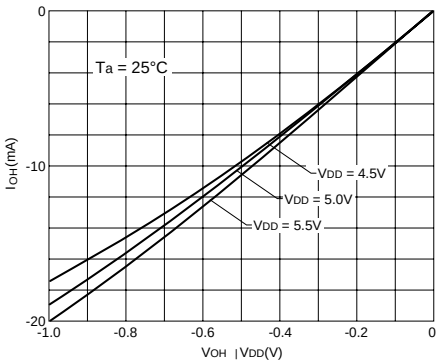


High level output current

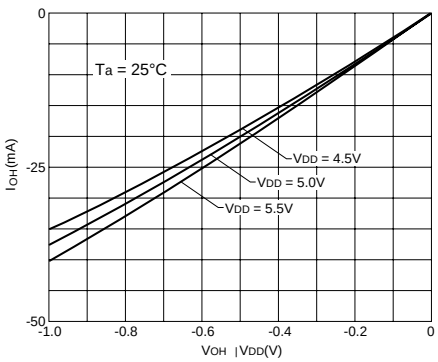
TYPE M



TYPE 1

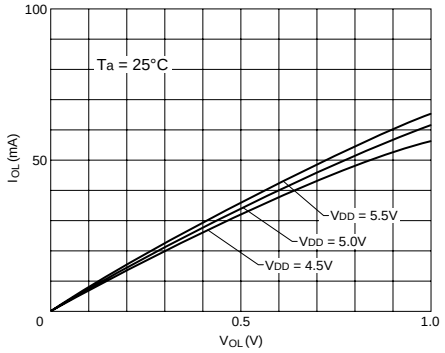


TYPE 2

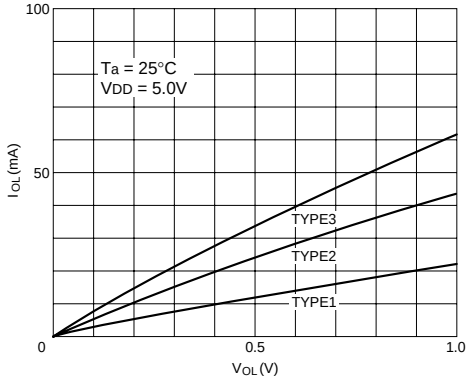


Low level output current

TYPE 3

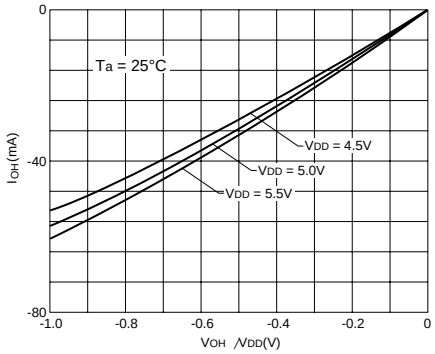


TYPE 1 to 3

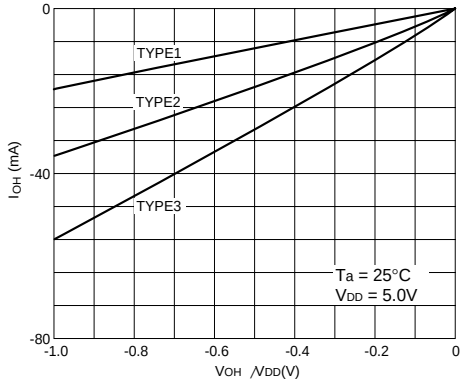


High level output current

TYPE 3

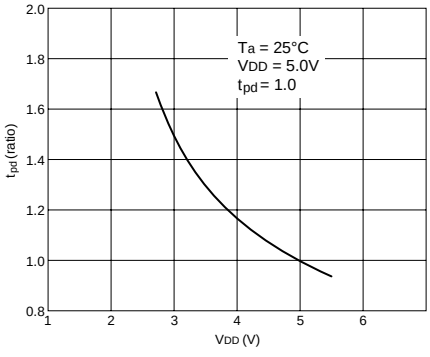


TYPE 1 to 3

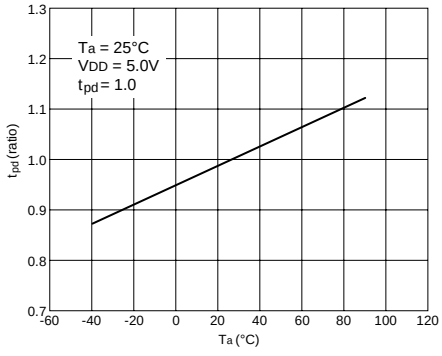


● Delay Characteristics

tpd vs. VDD

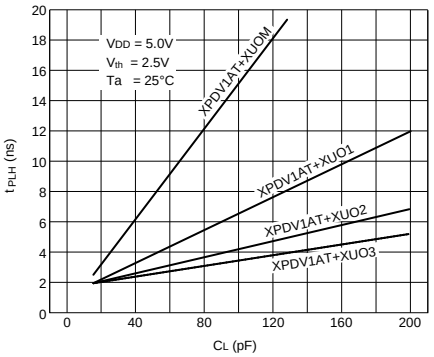


tpd vs. Ta

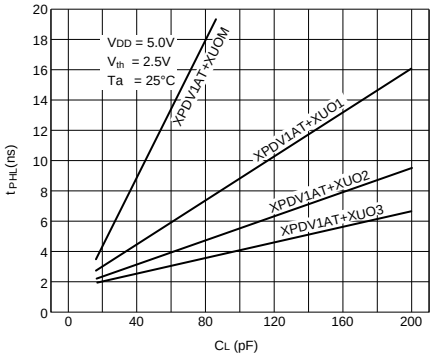


● Output delay time vs. CL

tPLH vs. CL



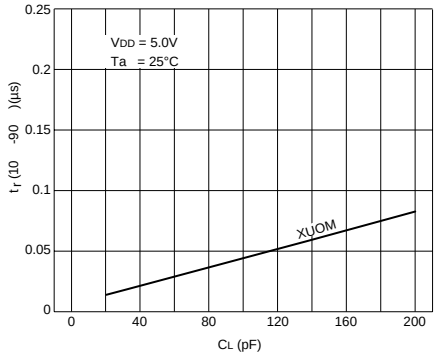
tPHL vs. CL



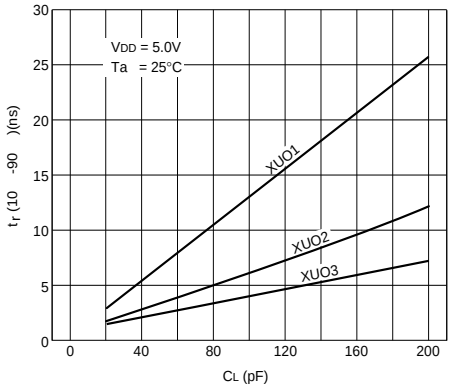
● Output Buffer tr, tf vs. CL

tr vs. CL characteristics

TYPE M

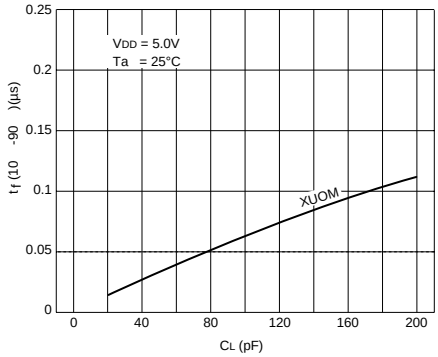


TYPE 1 to 3

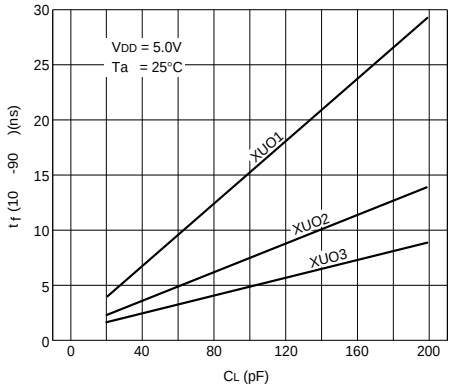


tf vs. CL characteristics

TYPE M



TYPE 1 to 3



■ PERFORMANCE CURVES (V_{DD}=3.3V)

● Output Current Characteristics (3.3V±0.3V)

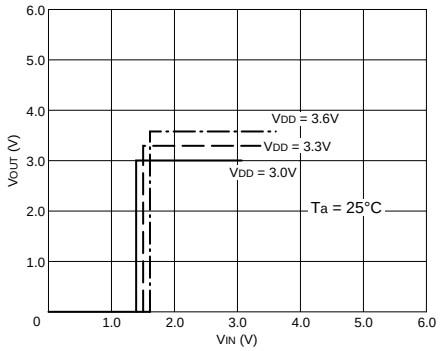
TYPE number	Output current	
	I_{OH} (mA)	I_{OL} (mA)
TYPE M	-0.5	0.5
TYPE 1	-2	2
TYPE 2	-4	4
TYPE 3	-6	6

The alphanumerics of the *TYPE (M, 1-3) indicate the output cell names (xx * x).**

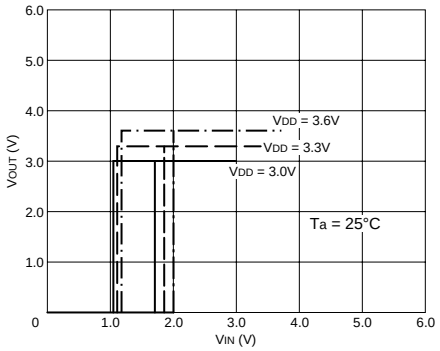
Example: XUO3 Å® Indicates TYPE3

● Output Buffer Characteristics (3.3V±0.3V)

Standard Type



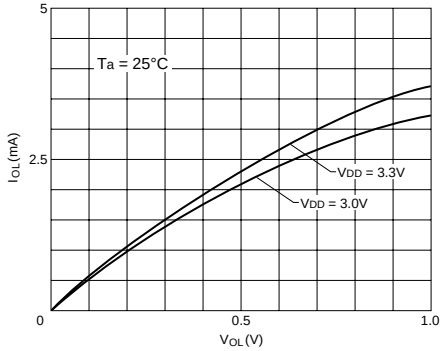
Schmitt–Trigger cell



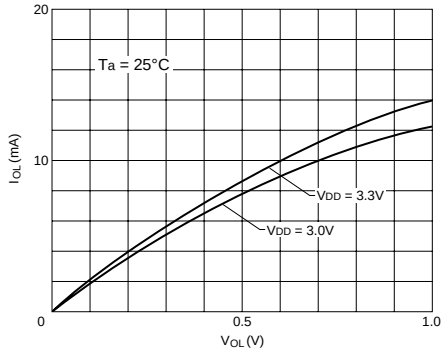
● Output Driver Characteristics

Low level output current

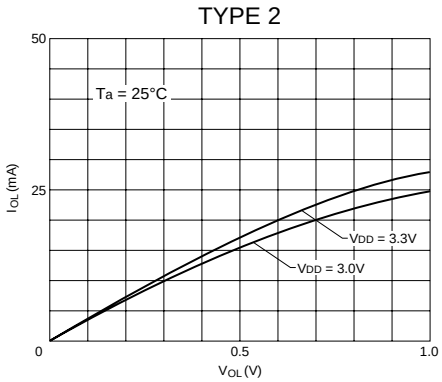
TYPE M



TYPE 1

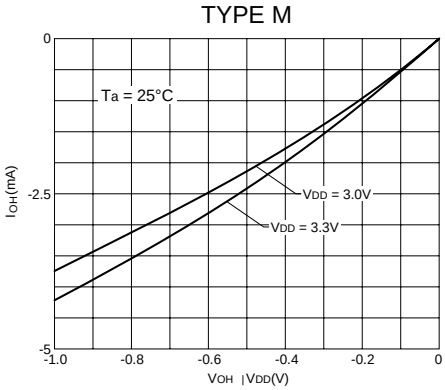


TYPE 2

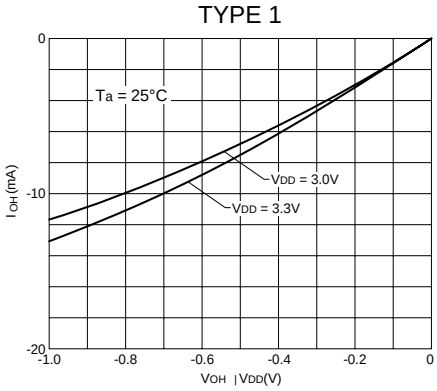


High level output current

TYPE M



TYPE 1



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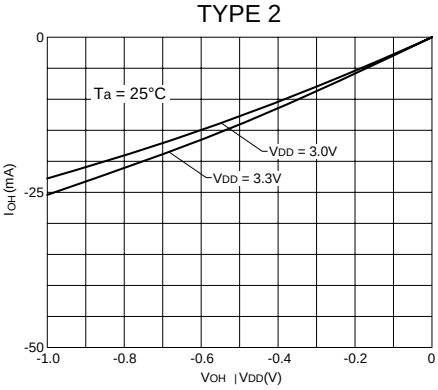
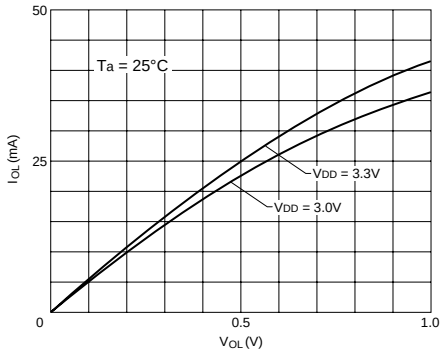
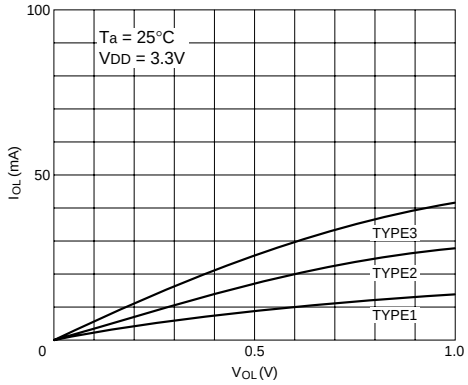


Low level output current

TYPE 3

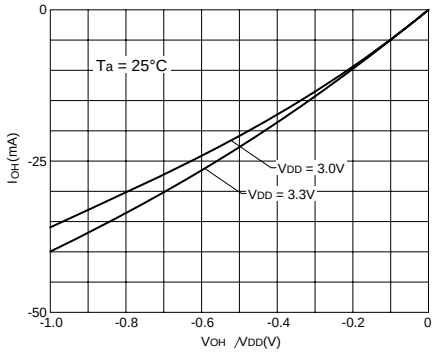


TYPE 1 to 3

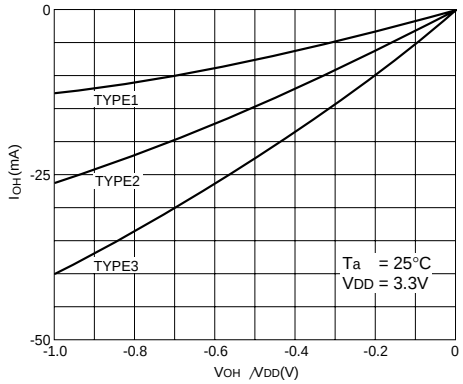


High level output current

TYPE 3

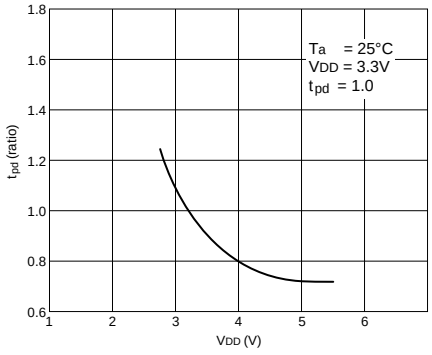


TYPE 1 to 3



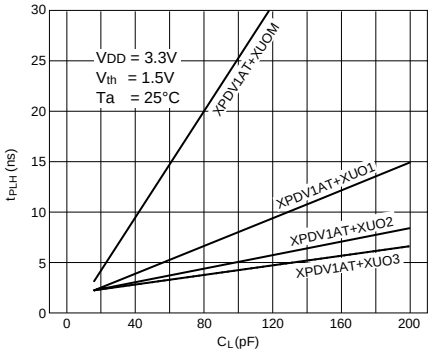
● Delay Characteristics

tpd vs. VDD

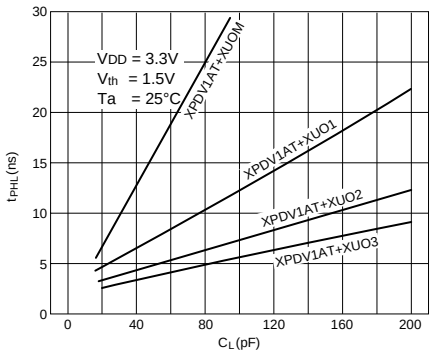


● Output delay time vs. CL

tPLH vs. CL

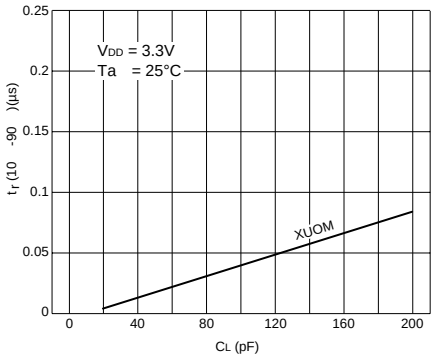


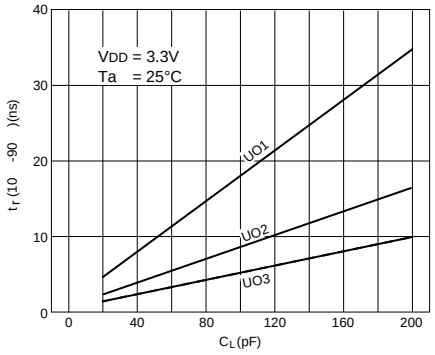
tPHL vs. CL



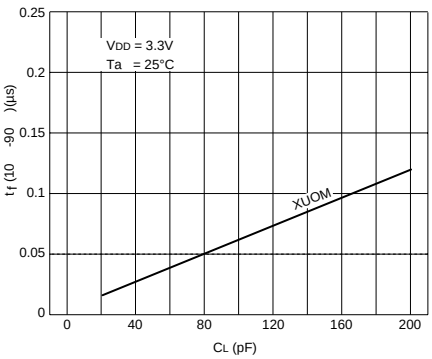
● Output Buffer tr, tf vs. CL

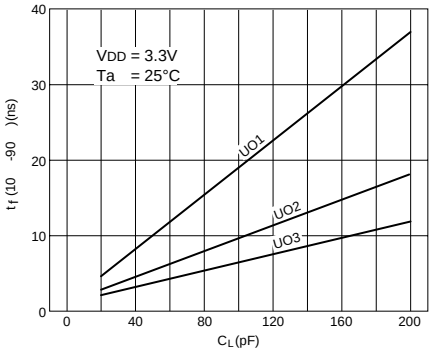
tr vs. CL characteristics





tf vs. CL characteristics





SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I (Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

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http://www.epson.co.jp

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