EPSON

# SLA30000 Series

## High Speed Gate Array

Wide Voltage Operation Products

- Super high-speed, and high density gate array
- Dual power supply operation
- Raw gates from 18K to 216K gates (Sea of gates)

## ■ DESCRIPTION

The SLA30000 Series is an SOG-type CMOS gate array featuring the very high-speed operations, high density, and high output drive capability. This series has a full lineup of gate arrays to cover 18,544 to 216,216 gates for the large-scale, and high-speed systems. They can drive with both +5V and +3V supply voltages.
This series also has a built-in level shifter to provide dual-power interfacing in various low-voltage applications. The I/O cells supporting the PCI Revision 2.0 are available for PCs and peripheral equipments. Also, the micro-ampere order, low-noise output cells are available for portable equipments and instruments of various applications.

## ■ FEATURES

- Super-high density (adopting 0.6μm silicon gate CMOS with 2 and 3-metal layers)
- High-speed operation (operation delay of internal gate = 0.25ns at 5.0V, 2-input power NAND standard)
- Selectable supply voltage: 5.0V, 3.3V, 3.0V and built-in dual-power supplies level shift circuit
- Output drivability ($I_{OL}$ = 100μ, 1, 4, 8, 12 mA when PCI = 5.0V, $I_{OL}$ = 50μ, 500μ, 4, 6, 12 mA when PCI = 3.3V)
- On-chip RAM available
- I/O cells supporting the PCI Revision 2.0 and low noise output cells available

## ■ PRODUCT LINEUP

| Master / Features | | SLA3018 | SLA3030 | SLA3042 | SLA3055 | SLA3075 | SLA3109 | SLA3125 | SLA3216 |
|---|---|---|---|---|---|---|---|---|---|
| | 2-layer Metal | SLA3018 | SLA3030 | SLA3042 | SLA3055 | SLA3075 | SLA3109 | SLA3125 | SLA3216 |
| | 3-layer Metal | SLA301T | SLA303T | SLA304T | SLA305T | SLA307T | SLA310T | SLA312T | SLA321T |
| Total BCs (Raw Gates) | Dual Power Supply | 18,544 | 30,846 | 42,262 | 55,341 | 75,450 | 109,080 | 125,836 | 216,216 |
| | Single Power Supply | 23,572 | 37,232 | 49,680 | 63,784 | 85,251 | 120,802 | 138,400 | 232,582 |
| Usable BCs 2-layer Metal (Dual Power Supply) | 2-layer Metal | 9,272 | 15,423 | 19,863 | 26,010 | 33,952 | 49,086 | 54,109 | 86,486 |
| | 3-layer Metal | 16,318 | 26,219 | 35,077 | 44,272 | 58,851 | 81,810 | 94,377 | 151,351 |
| Usable BCs 2-layer Metal (Single Power Supply) | 2-layer Meta | 11,786 | 18,616 | 23,349 | 29,978 | 38,362 | 54,360 | 59,512 | 93,032 |
| | 3-layer Metal | 20,743 | 31,647 | 41,234 | 51,027 | 66,495 | 90,601 | 103,800 | 162,807 |
| Number of PADs | | 128 | 160 | 184 | 208 | 240 | 256 | 304 | 376 |
| Propagation Delay | Internal Gates | tpd = 0.25ns (standard at 5.0V), tpd = 0.33ns (standard at 3.3V) | | | | | | | |
| | Input Buffers | tpd = 0.48ns (standard at 5.0V), tpd = 0.63ns (standard at 3.3V) | | | | | | | |
| | Output Buffers | tpd = 2.08ns (standard at 5.0V), tpd = 2.86ns (standard at 3.3V) CL = 50pF | | | | | | | |
| I/O Level | | CMOS, TTL, PCI | | | | | | | |
| Input Mode | | TTL, CMOS, Pull-up/Pull-down, schmitt, 3.0/3.3/5.0V Level interface (Level shifter) | | | | | | | |
| Output Mode | | Normal, open drain, 3-state, Bi-directional, 3.0/3.3/5.0V Level interface (Level shifter) | | | | | | | |

## ■ ABSOLUTE MAXIMUM RATINGS

($V_{SS}$=0V)

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Power voltage | $V_{DD}$ | –0.3 ~ 6.0 | V |
| Input voltage | $V_I$ | –0.3 to $V_{DD}$+0.5 | V |
| Output voltage | $V_O$ | –0.3 to $V_{DD}$+0.5 | V |
| Output current/pin | $I_{OUT}$ | ±25(±50*1) | mA |
| Storage temperature | Tstg | –65 ~150 | °C |

*1: For cell of 24mA output current

## ■ RECOMMENDED OPERATING CONDITIONS

● Single power supply

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power voltage | $V_{DD}$ | 2.70<br>3.00<br>4.75<br>4.50 | 3.00<br>3.30<br>5.00<br>5.00 | 3.30<br>3.60<br>5.25<br>5.50 | V |
| Input voltage | $V_I$ | $V_{SS}$ | – | $V_{DD}$ | V |
| Operating temperature | Topr | 0<br>–40 | 25<br>25 | 70<br>85 | °C<br>°C |
| Normal input during input rise time | $t_{ri}$ | – | – | 50 | ns |
| Normal input during input fall time | $t_{fi}$ | – | – | 50 | ns |
| Schmitt input during input rise time | $t_{ri}$ | – | – | 5 | ms |
| Schmitt input during input fall time | $t_{fi}$ | – | – | 5 | ms |

● Dual power supply

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power voltage<br>(High voltage) | $HV_{DD}$<br>$HV_{DD}$ | 4.75<br>4.50 | 5.00<br>5.00 | 5.25<br>5.50 | V<br>V |
| Power voltage<br>(Low voltage) | $LV_{DD}$<br>$LV_{DD}$ | 2.70<br>3.00 | 3.00<br>3.30 | 3.30<br>3.60 | V<br>V |
| Input voltage | $HV_I$<br>$LV_I$ | $V_{SS}$<br>$V_{SS}$ | –<br>– | $HV_{DD}$<br>$LV_{DD}$ | V<br>V |
| Operating temperature | Topr | 0<br>–40 | 25<br>25 | 70<br>85 | °C<br>°C |
| Normal input during input rise time | $t_{ri}$ | – | – | 50 | ns |
| Normal input during input fall time | $t_{fi}$ | – | – | 50 | ns |
| Schmitt input during input rise time | $t_{ri}$ | – | – | 5 | ms |
| Schmitt input during input fall time | $t_{fi}$ | – | – | 5 | ms |

## ■ ELECTRICAL CHARACTERISTICS ($V_{DD}$=5V)

($V_{DD}$ = 5V, $V_{SS}$ = 0V, Ta =–40 to 85°C)

| Item | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Stand-by current * | $I_{DDS}$ | Stop position | | – | – | 400 | µA |
| Input leakage current | $I_{LI}$ | – | | –1 | – | 1 | µA |
| Off-state leakage current | $I_{OZ}$ | – | | –1 | – | 1 | µA |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = –0.1mA (Type S), –1mA (Type M), –4mA (Type 1), –8mA (Type 2), –12mA (Type 3, 4) $V_{DD}$ = Min. | | $V_{DD}$ –4 | – | – | V |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 0.1mA (Type S), 1mA (Type M), 4mA (Type 1), 8mA (Type 2), 12mA (Type 3), 24mA (Type 4) $V_{DD}$ = Min. | | – | – | 0.4 | V |
| High level input voltage | $V_{IH1}$ | CMOS level, $V_{DD}$ = Max. | | 3.5 | – | – | V |
| Low level input voltage | $V_{IL1}$ | CMOS level, $V_{DD}$ = Min. | | – | – | 1.0 | V |
| High level input voltage | $V_{T1+}$ | CMOS Schmitt, $V_{DD}$ = 5.0V | | – | – | 4.0 | V |
| Low level input voltage | $V_{T1-}$ | CMOS Schmitt, $V_{DD}$ = 5.0V | | 0.8 | – | – | V |
| Hysterisis voltage | $V_{H1}$ | CMOS Schmitt, $V_{DD}$ = 5.0V | | 0.3 | – | – | V |
| High level input voltage | $V_{IH2}$ | TTL level, $V_{DD}$ = Max. | | 2.0 | – | – | V |
| Low level input voltage | $V_{IL2}$ | TTL level, $V_{DD}$ = Min. | | – | – | 0.8 | V |
| High level input voltage | $V_{T2+}$ | TTL Schmitt, $V_{DD}$ = 5.0V | | – | – | 2.4 | V |
| Low level input voltage | $V_{T2-}$ | TTL Schmitt, $V_{DD}$ = 5.0V | | 0.6 | – | – | V |
| Hysterisis voltage | $V_{H2}$ | TTL Schmitt, $V_{DD}$ = 5.0V | | 0.1 | – | – | V |
| High level input voltage | $V_{IH3}$ | PCI level, $V_{DD}$ = Max. | | 2.0 | – | – | V |
| Low level input voltage | $V_{IL3}$ | PCI level, $V_{DD}$ = Min. | | – | – | 0.8 | V |
| High level output current | $I_{OH3}$ | Available for PCI , $V_{OH}$ = 1.4V, | | –44 | – | – | mA |
| | | $V_{DD}$ = Min., $V_{OH}$ = 3.1V, $V_{DD}$ = Max. | | – | – | –142 | mA |
| Low level output currrent | $I_{OL3}$ | Available for PCI , $V_{OL}$ = 2.2V, | | 95 | – | – | mA |
| | | $V_{DD}$ = Min., $V_{OL}$ = 0.71V, $V_{DD}$ = Max. | | – | – | 206 | mA |
| Pull-up resistor | $R_{PU}$ | $V_I$ = 0V | Type 1 | 25 | 50 | 100 | KΩ |
| | | | Type 2 | 50 | 100 | 200 | |
| Pull-down resistor | $R_{PD}$ | $V_I$ = $V_{DD}$ | Type 1 | 25 | 50 | 100 | KΩ |
| | | | Type 2 | 50 | 100 | 200 | |
| High level hold current | $I_{BHH1}$ | Available for bus holding, $V_{IN}$ = 3.5V (CMOS system) $V_{DD}$ = Max. | | – | – | –90 | µA |
| Low level hold current | $I_{BHL1}$ | Available for bus holding, $V_{IN}$ = 1.0V (CMOS system) $V_{DD}$ = Max. | | – | – | 60 | µA |
| High level hold current | $I_{BHH2}$ | Available for bus holding, $V_{IN}$ = 2.0V (TTL system) $V_{DD}$ = Max. | | – | – | –110 | µA |
| Low level hold current | $I_{BHL2}$ | Available for bus holding, $V_{IN}$ = 0.8V (TTL system) $V_{DD}$ = Max. | | – | – | 50 | µA |
| High level inversion current | $I_{BHHO}$ | Available for bus holding, $V_{DD}$ = Min. | | –900 | – | – | mA |
| Low level inversion current | $I_{BHLO}$ | Available for bus holding, $V_{DD}$ = Min. | | 530 | – | – | mA |
| Input pin capacitance | $C_I$ | f = 1MHz, $V_{DD}$ = 0V | | – | – | 12 | pF |
| Output pin capacitance | $C_O$ | f = 1MHz, $V_{DD}$ = 0V | | – | – | 12 | pF |
| I/O pin capacitance | $C_{IO}$ | f = 1MHz, $V_{DD}$ = 0V | | – | – | 12 | pF |

* Stand by current is a representative value of eresy series

## ■ ELECTRICAL CHARACTERISTICS ($V_{DD}$=3V)

($V_{DD}$ = 3V±0.3V, $V_{SS}$ = 0V, Ta = –40 to 85°C)

| Item | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Stand-by current* | $I_{DDS}$ | Stop position | | – | – | 260 | µA |
| Input leakage current | $I_{LI}$ | – | | –1 | – | 1 | µA |
| Off-state leakage current | $I_{OZ}$ | – | | –1 | – | 1 | µA |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = –0.05mA (Type S),<br>–0.5mA (Type M),<br>–1.8mA (Type 1),<br>–3.5mA (Type 2),<br>–5mA (Type 3, 4)<br>$V_{DD}$ = Min. | | $V_{DD}$<br>–0.3 | – | – | V |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 0.05mA (Type S),<br>0.5mA (Type M),<br>1.8mA (Type 1),<br>3.5mA (Type 2),<br>5mA (Type 3),<br>10mA (Type 4)<br>$V_{DD}$ = Min. | | – | – | 0.3 | V |
| High level input voltage | $V_{IH1}$ | CMOS level, $V_{DD}$ = Max. | | 2.0 | – | – | V |
| Low level input voltage | $V_{IL1}$ | CMOS level, $V_{DD}$ = Min. | | – | – | 0.8 | V |
| High level input voltage | $V_{T1+}$ | CMOS Schmitt, $V_{DD}$ = 3.0V | | – | – | 2.3 | V |
| Low level input voltage | $V_{T1-}$ | CMOS Schmitt, $V_{DD}$ = 3.0V | | 0.5 | – | – | V |
| Hysterisis voltage | $V_{H1}$ | CMOS Schmitt, $V_{DD}$ = 3.0V | | 0.1 | – | – | V |
| High level input voltage | $V_{IH3}$ | PCI level, $V_{DD}$ = Max. | | 1.58 | – | – | V |
| Low level input voltage | $V_{IL3}$ | PCI level, $V_{DD}$ = Min. | | – | – | 0.88 | V |
| High level output currrent | $I_{OH3}$ | Available for PCI, $V_{OH}$ = 0.81V,<br>$V_{DD}$ = Min., $V_{OH}$ = 2.31V, $V_{DD}$ = Max. | | –33<br>– | –<br>– | –<br>–105 | mA<br>mA |
| Low level output current | $I_{OL3}$ | Available for PCI, $V_{OL}$ = 1.62V,<br>$V_{DD}$ = Min., $V_{OL}$ = 0.60V, $V_{DD}$ = Max. | | 44<br>– | –<br>– | –<br>125 | mA<br>mA |
| Pull-up resistor | $R_{PU}$ | $V_I$ = 0V | Type 1 | 50 | 100 | 200 | KΩ |
| | | | Type 2 | 100 | 200 | 400 | |
| Pull-down resistor | $R_{PD}$ | $V_O$ = $V_{DD}$ | Type 1 | 50 | 100 | 200 | KΩ |
| | | | Type 2 | 100 | 200 | 400 | |
| High level hold current | $I_{BHH}$ | Available for bus holding, $V_{IN}$ = 2.0V<br>$V_{DD}$ = Max. | | – | – | –32 | µA |
| Low level hold current | $I_{BHL}$ | Available for bus holding, $V_{IN}$ = 0.8V<br>$V_{DD}$ = Max. | | – | – | 27 | µA |
| High level inversion current | $I_{BHHO}$ | Available for bus holding, $V_{DD}$ = Min. | | –290 | – | – | mA |
| Low level inversion current | $I_{BHLO}$ | Available for bus holding, $V_{DD}$ = Min. | | 170 | – | – | mA |
| Input pin capacitance | $C_I$ | f = 1MHz, $V_{DD}$ = 0V | | – | – | 12 | pF |
| Output pin capacitance | $C_O$ | f = 1MHz, $V_{DD}$ = 0V | | – | – | 12 | pF |
| I/O pin capacitance | $C_{IO}$ | f = 1MHz, $V_{DD}$ = 0V | | – | – | 12 | pF |

* Stand by current is a representative value of eresy series

## ■ ELECTRICAL CHARACTERISTICS ($V_{DD}$=3.3V)

($V_{DD}$ = 3.3V±0.3V, $V_{SS}$ = 0V, Ta = –40 to 85°C)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Stand-by current* | $I_{DDS}$ | Stop position | | – | – | 290 | µA |
| Input leakage current | $I_{LI}$ | – | | –1 | – | 1 | µA |
| Off-state leakage current | $I_{OZ}$ | – | | –1 | – | 1 | µA |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = –0.05mA (Type S), –0.5mA (Type M), –2mA (Type 1), –4mA (Type 2), –6mA (Type 3, 4) $V_{DD}$ = Min. | | $V_{DD}$ –0.3 | – | – | V |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 0.05mA (Type S), 0.5mA (Type M), 2mA (Type 1), 4mA (Type 2), 6mA (Type 3), 12mA (Type 4) $V_{DD}$ = Min. | | – | – | 0.3 | V |
| High level input voltage | $V_{IH1}$ | CMOS level, $V_{DD}$ = Max. | | 2.2 | – | – | V |
| Low level input voltage | $V_{IL1}$ | CMOS level, $V_{DD}$ = Min. | | – | – | 0.8 | V |
| High level input voltage | $V_{T1+}$ | CMOS Schmitt, $V_{DD}$ = 3.3V | | – | – | 2.4 | V |
| Low level input voltage | $V_{T1-}$ | CMOS Schmitt, $V_{DD}$ = 3.3V | | 0.6 | – | – | V |
| Hysterisis voltage | $V_{H1}$ | CMOS Schmitt, $V_{DD}$ = 3.3V | | 0.1 | – | – | V |
| High level input voltage | $V_{IH3}$ | PCI level, $V_{DD}$ = Max. | | 1.71 | – | – | V |
| Low level input voltage | $V_{IL3}$ | PCI level, $V_{DD}$ = Min. | | – | – | 0.98 | V |
| High level output current | $I_{OH3}$ | Available for PCI, $V_{OH}$ = 0.90V, | | –36 | – | – | mA |
| | | $V_{DD}$ = Min., $V_{OH}$ = 2.52V, $V_{DD}$ = Max. | | – | – | –115 | mA |
| Low level input current | $I_{OL3}$ | Available for PCI, $V_{OL}$ = 1.8V, | | 48 | – | – | mA |
| | | $V_{DD}$ = Min., $V_{OL}$ = 0.65V, $V_{DD}$ = Max. | | – | – | 137 | mA |
| Pull-up resistor | $R_{PU}$ | $V_I$ = 0V | Type 1 | 45 | 90 | 180 | KΩ |
| | | | Type 2 | 90 | 180 | 360 | |
| Pull-down resistor | $R_{PD}$ | $V_I$ = $V_{DD}$ | Type 1 | 45 | 90 | 180 | KΩ |
| | | | Type 2 | 100 | 200 | 360 | |
| High level hold current | $I_{BHH}$ | Available for bus holding, $V_{IN}$ = 2.0V $V_{DD}$ = Max. | | – | – | –40 | µA |
| Low level hold current | $I_{BHL}$ | Available for bus holding, $V_{IN}$ = 0.8V $V_{DD}$ = Max. | | – | – | 30 | µA |
| High level inversion current | $I_{BHHO}$ | Available for bus holding, $V_{DD}$ = Min. | | –350 | – | – | µA |
| Low level inversion current | $I_{BHLO}$ | Available for bus holding, $V_{DD}$ = Min. | | 210 | – | – | µA |
| Input pin capacitance | $C_I$ | f = 1MHz, $V_{DD}$ = 0V | | – | – | 12 | pF |
| Output pin capacitance | $C_O$ | f = 1MHz, $V_{DD}$ = 0V | | – | – | 12 | pF |
| I/O pin capacitance | $C_{IO}$ | f = 1MHz, $V_{DD}$ = 0V | | – | – | 12 | pF |

* Stand by current is a representative value of eresy series

## ■ ELECTRICAL CHARACTERISTICS (Stand-by Current)

● Single power supply (Ta= –40 to 85°C)

| Master | 5V±10% $I_{DDS}$ Max. | 3.3V±0.3V $I_{DDS}$ Max. | 3.0V±0.3V $I_{DDS}$ Max. | Unit |
|---|---|---|---|---|
| SLA3018/301T<br>SLA3030/303T<br>SLA3042/304T | 300 | 220 | 200 | µA |
| SLA3055/305T<br>SLA3075/307T<br>SLA3109/310T | 400 | 290 | 260 | µA |
| SLA3125/312T<br>SLA3216/321T | 600 | 430 | 400 | µA |

● Dual power supply (Ta= –40 to 85°C)

| Master | 5V±10% $HI_{DDS}$ Max. | 3.3V±0.3V $LI_{DDS}$ Max. | 5V±10% $HI_{DDS}$ Max. | 3.0V±0.3V $LI_{DDS}$ Max. | Unit |
|---|---|---|---|---|---|
| SLA3018/301T<br>SLA3030/303T<br>SLA3042/304T | 80 | 220 | 80 | 200 | µA |
| SLA3055/305T<br>SLA3075/307T<br>SLA3109/310T | 100 | 290 | 100 | 260 | µA |
| SLA3125/312T<br>SLA3216/321T | 160 | 430 | 160 | 400 | µA |

$HI_{DDS}$: Stand-by current between $HV_{DD}$ and $V_{SS}$.

$LI_{DDS}$: Stand-by current between $LV_{DD}$ and $V_{SS}$.

· In case of dual power supply, total stand-by current is the sum of $HI_{DDS}$ and $LI_{DDS}$.

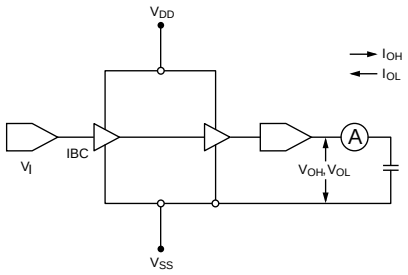
## ■ CHARACTERISTICS CURVES ($V_{DD}$=5V)

● Output Current Characteristics (5.0V±10%)

| Type number | Output Current | |
|---|---|---|
| | $I_{OH}$(mA) | $I_{OL}$(mA) |
| TypeS | –0.1 | 0.1 |
| TypeM | –1 | 1 |
| Type1 | –4 | 4 |
| Type2 | –8 | 8 |
| Type3 | –12 | 12 |
| Type4 | –12 | 24 |
| PCI | Conforms to PCI standard. | |

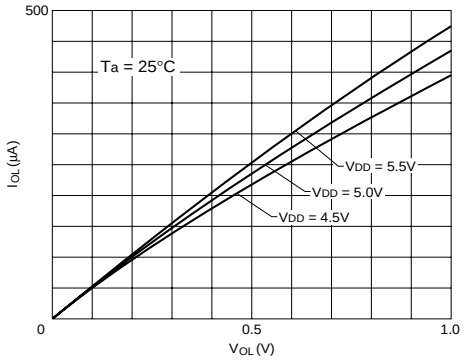
Letters S, M and 1 to 4 of "Type*" represent the numbers used for the output cell name (in format of "XX❑X").

Measurement Circuit

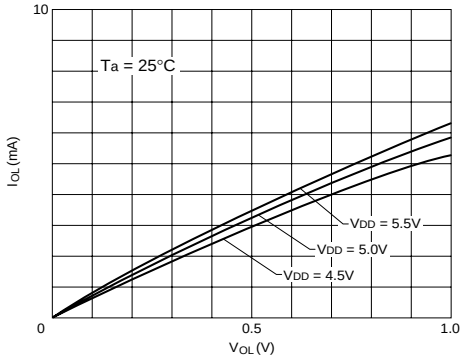


Low level output current

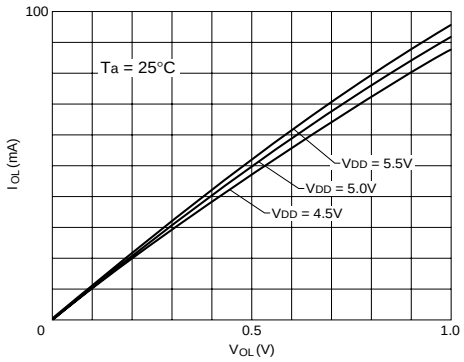
Type S



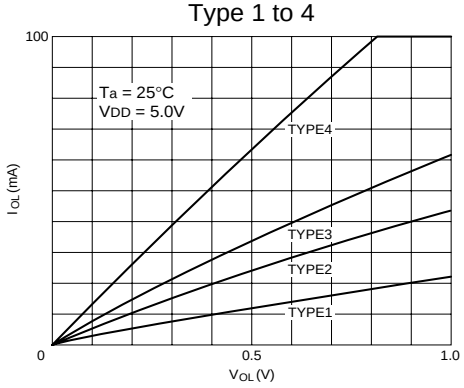

Type M




PCI

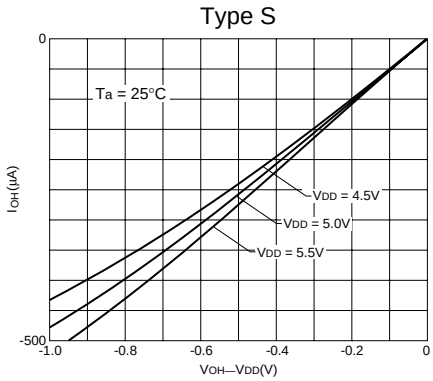



Type 1 to 4

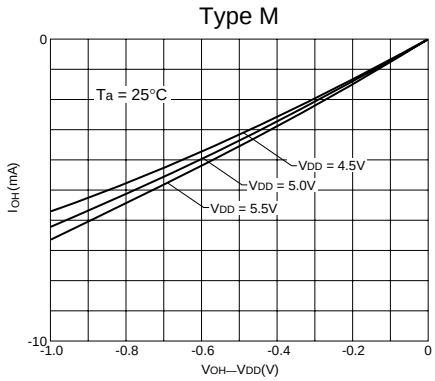



High level output current

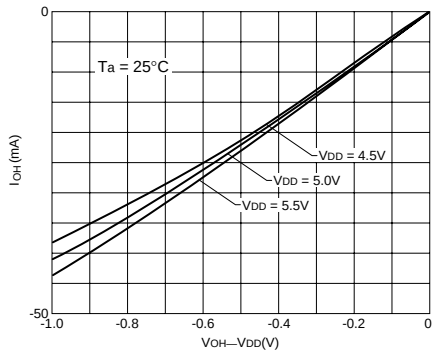
Type S



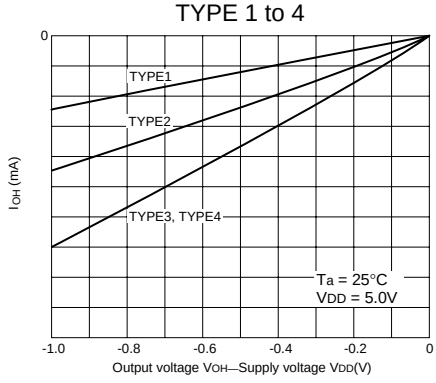

Type M




PCI



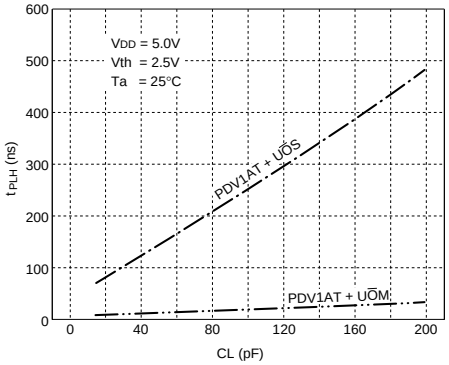

TYPE 1 to 4



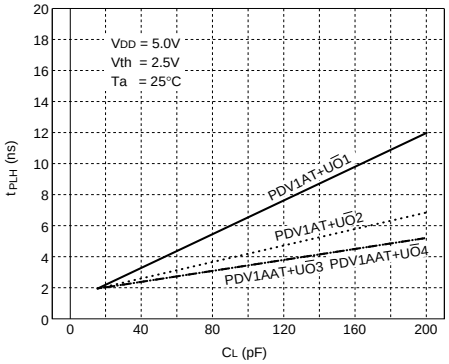
● tpd, tr, tf-CL

tpLH vs. CL

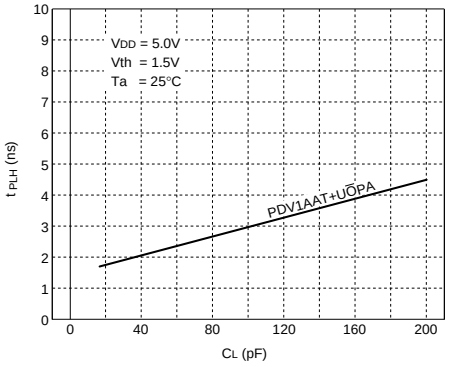
Type S, M




Type1 to 4

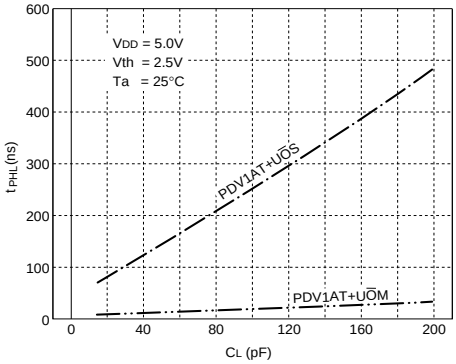



PCI

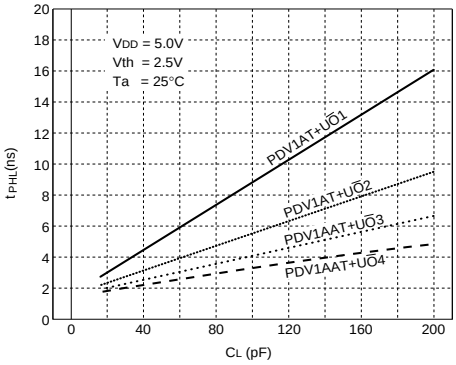



tpHL vs. CL

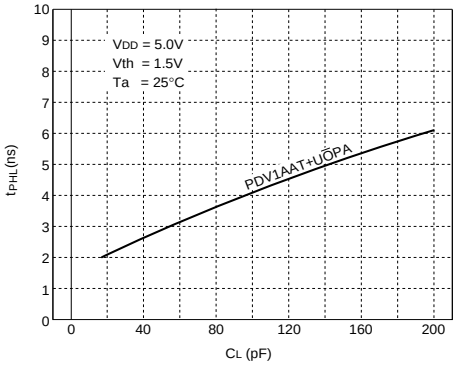
Type S, M




Type1 to 4



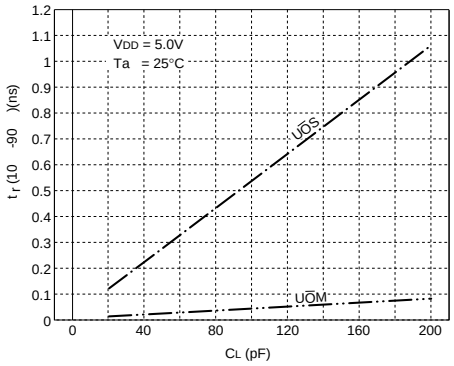

PCI



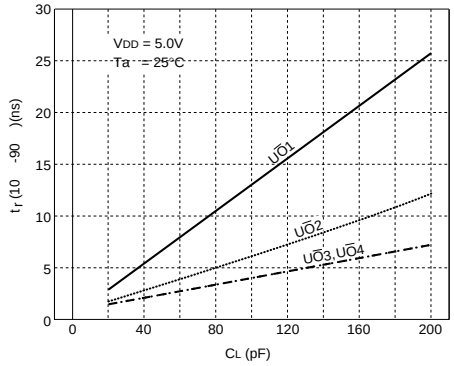
● tpd, tr, tf-CL

tr vs. CL

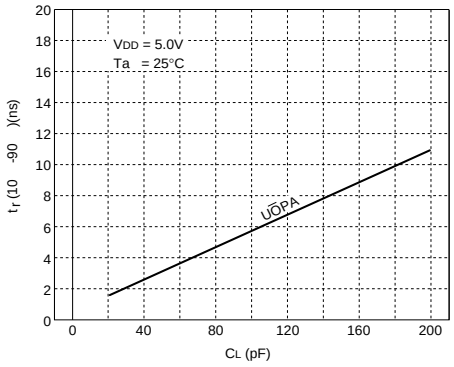
Type S, M




Type1 to 4

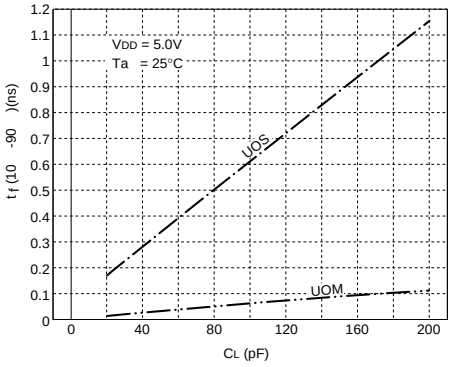



PCI

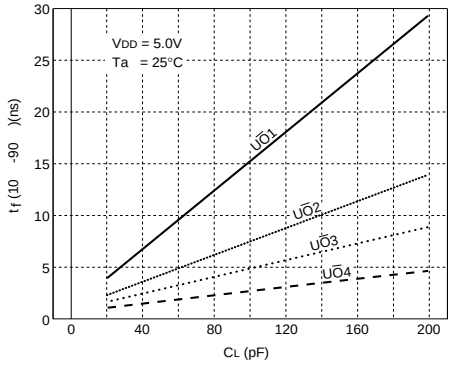



tf vs. CL

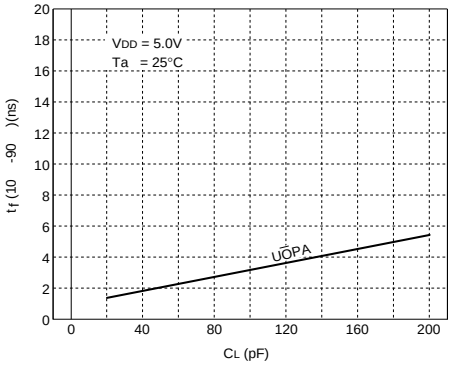
Type S, M




Type1 to 4

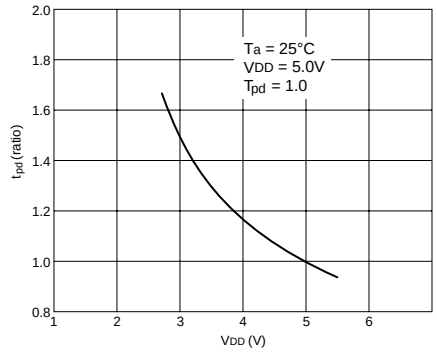



PCI

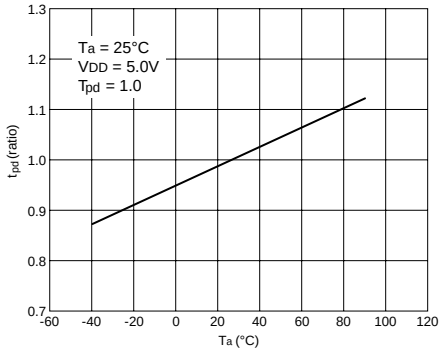


● Delay Time

Propagation delay(tpd) vs. supply voltage($V_{DD}$)




Propagation delay(tpd) vs. ambient temperature(Ta)




## ■ CHARACTERISTICS CURVES ($V_{DD}$=3.3V)

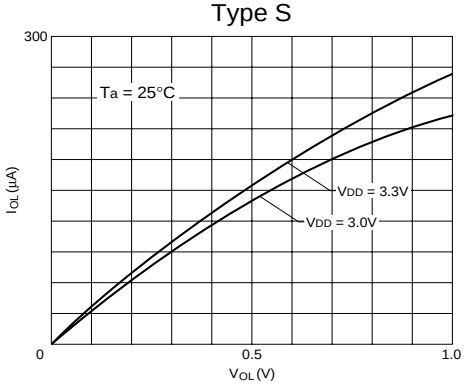
● Output Current (3.3V±0.3V)

| Type number | Output Current | |
|---|---|---|
| | $I_{OH}$(mA) | $I_{OL}$(mA) |
| TypeS | –0.05 | 0.05 |
| TypeM | –0.5 | 0.5 |
| Type1 | –2 | 2 |
| Type2 | –4 | 4 |
| Type3 | –6 | 6 |
| Type4 | –6 | 12 |
| PCI | Conforms to PCI standard. | |

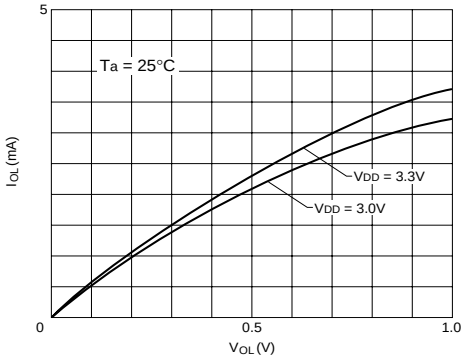
Letters S, M and 1 to 4 of "Type*" represent the numbers used for the output cell name (in format of "XX❑X").

Low level output current

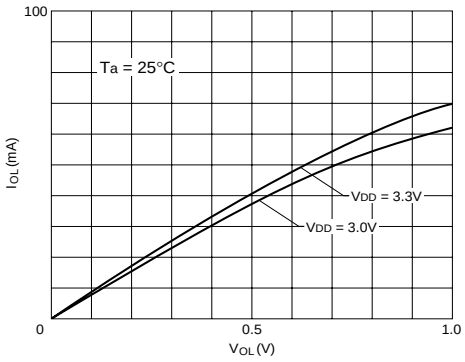
Type S



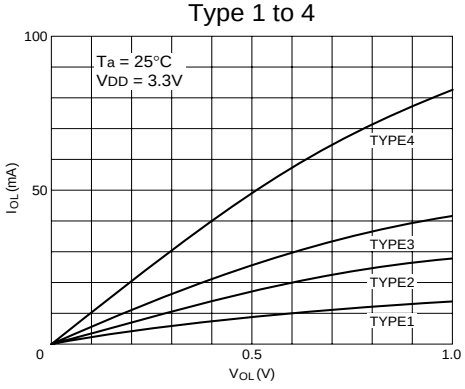

Type M




PCI

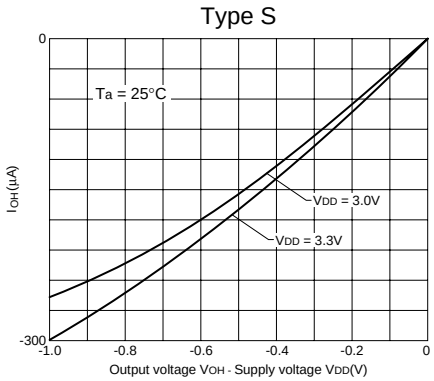



Type 1 to 4

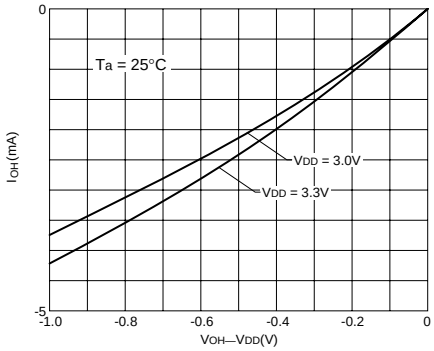



High level output current

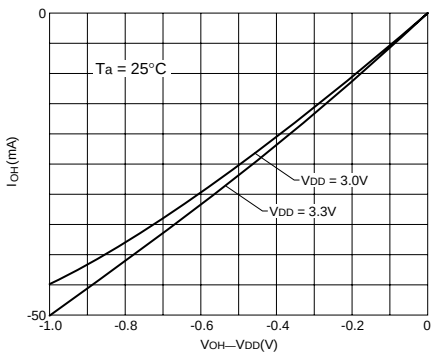
Type S



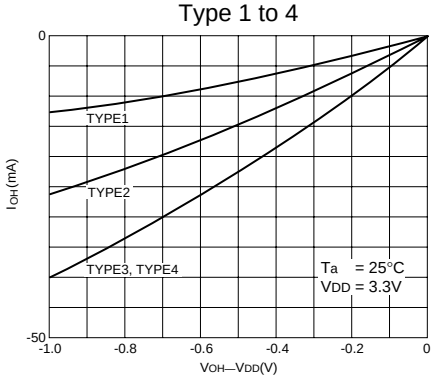

Type M




PCI



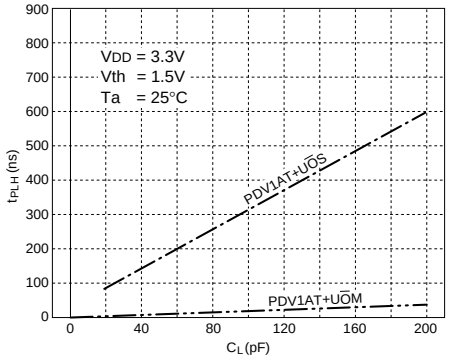

Type 1 to 4



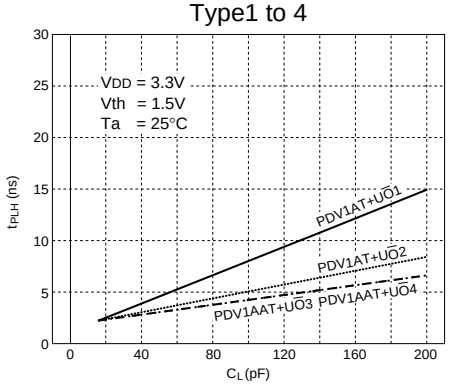
● tpd, tr, tf-CL

tpLH vs. CL

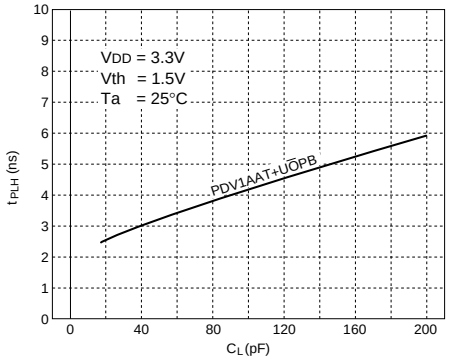
Type S, M




Type1 to 4

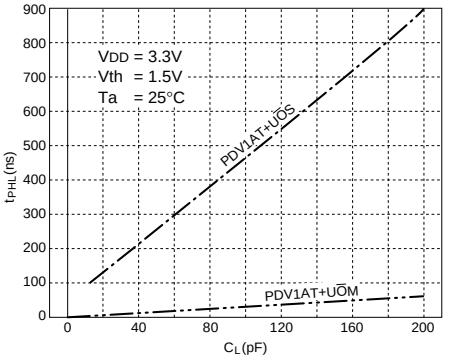



PCI

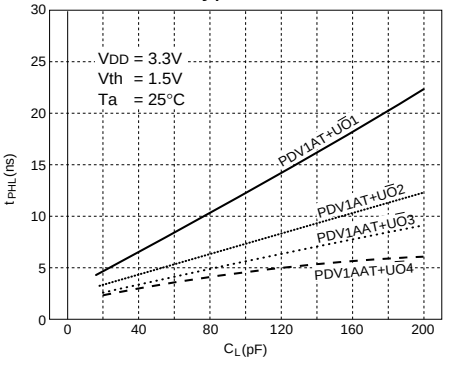



tpHL vs. CL

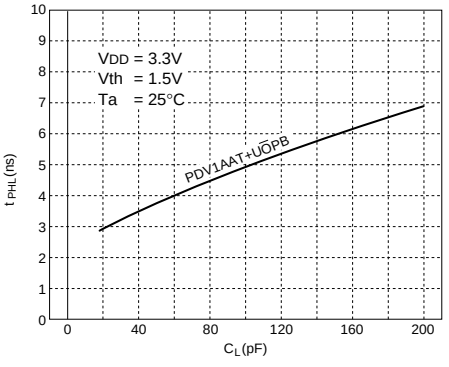
Type S, M




Type1 to 4



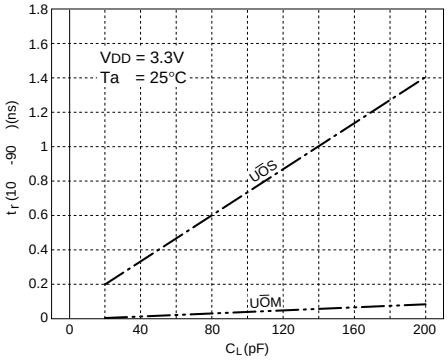

PCI



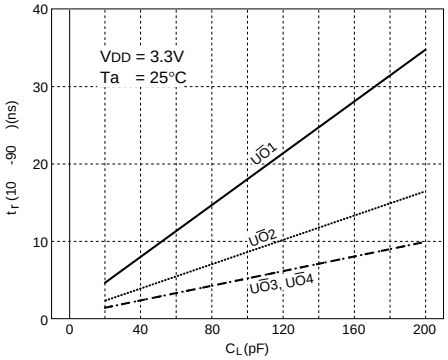
● tpd, tr, tf-CL

tr vs. CL

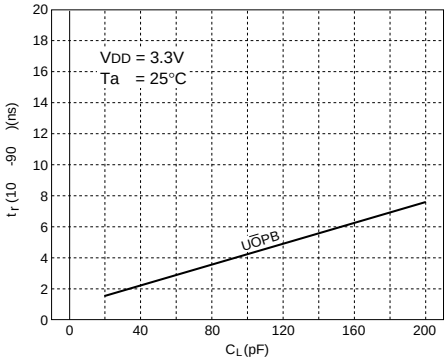
Type S, M




Type1 to 4

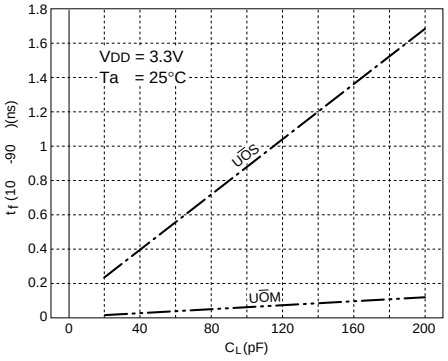



PCI

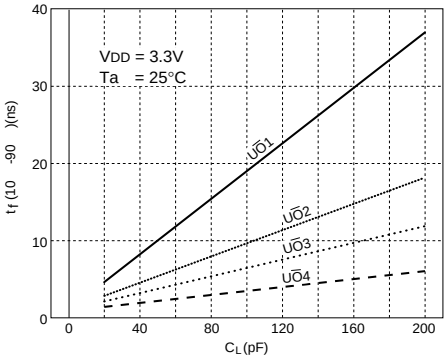



tf vs. CL

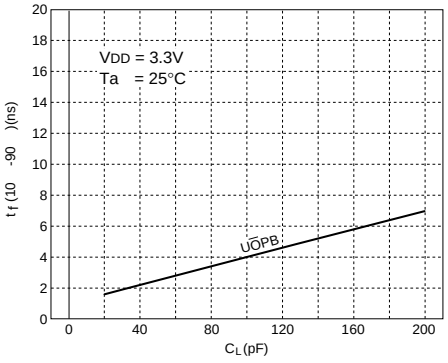
Type S, M




Type1 to 4




PCI



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Electric Device Information of EPSON WWW server

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