SED1630

CMOS DOT MATRIX
HIGH DUTY
LCD COMMON DRIVER

S-MOS Systems, Inc.
October, 1996
Version 1.0 (Preliminary)

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Table of Contents

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1.0 GENERAL DESCRIPTION

1.1 DESCRIPTION

The SED1630 is a 68 output dot matrix LCD common (row) driver for driving a high-capacity LCD panel at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of LCD driving voltages. Due to the architecture of the SED1630, the LCD driving voltage V_0 is isolated from V_{DD}. This provides the ability to adjust the offset bias independently of V_{DD}. These unique features allow the SED1610 to interface with a variety of LCD panels.

The SED1630 is used in conjunction with the SED1600 (80 segment driver) or the SED1601 (80 segment driver) or the SED1620 (128-bit segment driver) to drive a large-capacity dot matrix LCD panel.

1.2 FEATURES

- Low-power CMOS technology
- 68-bit common (row) driver
- Duty cycle . . . . . 1/64 to 1/300
- Display blanking available
- Shift clock frequency . . . . . 2MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Selectable output shift direction
- Wide range of LCD voltage . . . . 12V to 28V
- Supply voltage . . . . . 5.0V ± 10%
- Package . . . . . QFP5-80 pins (F_{0A})
  Die Al pad (D_{0A})

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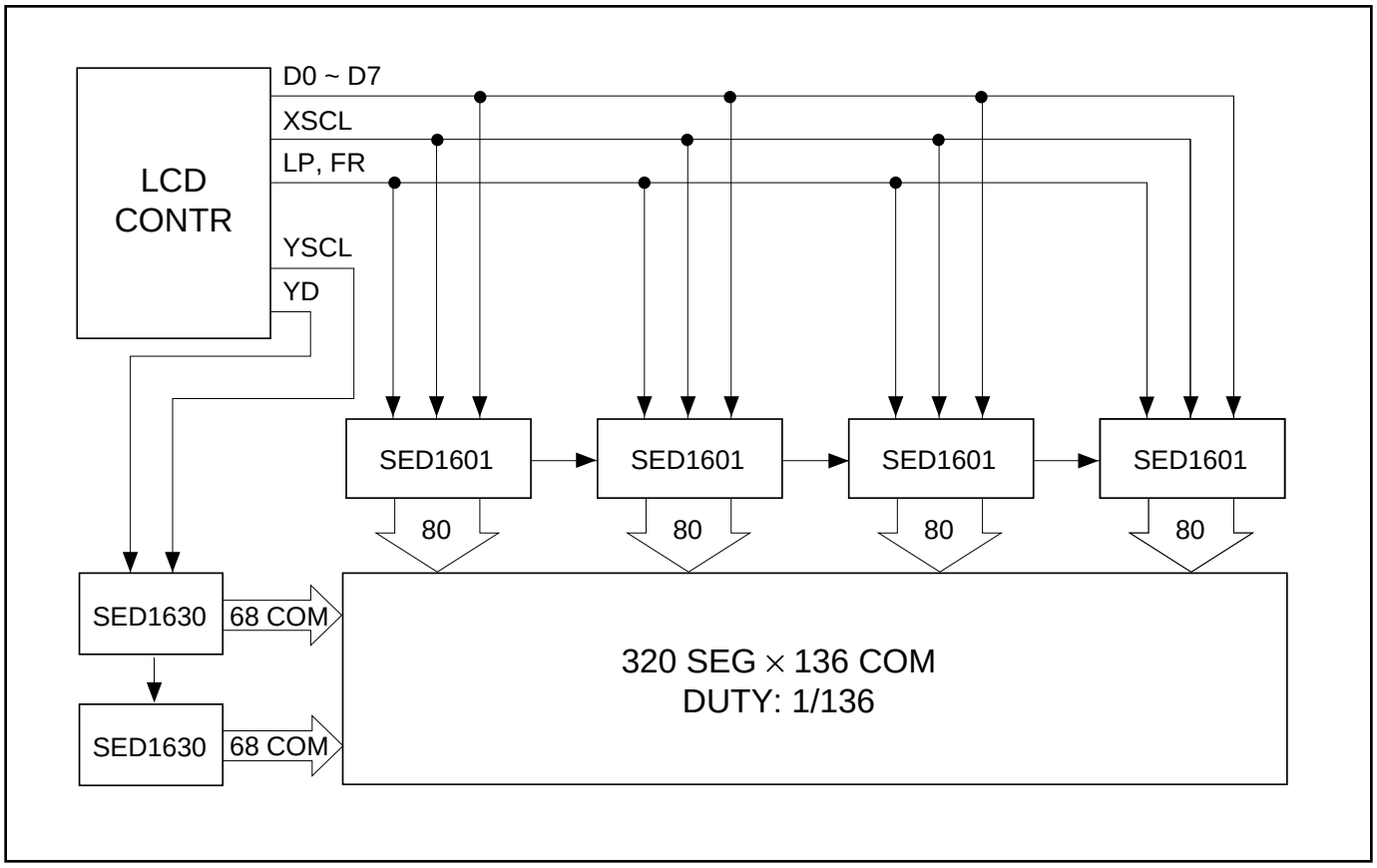
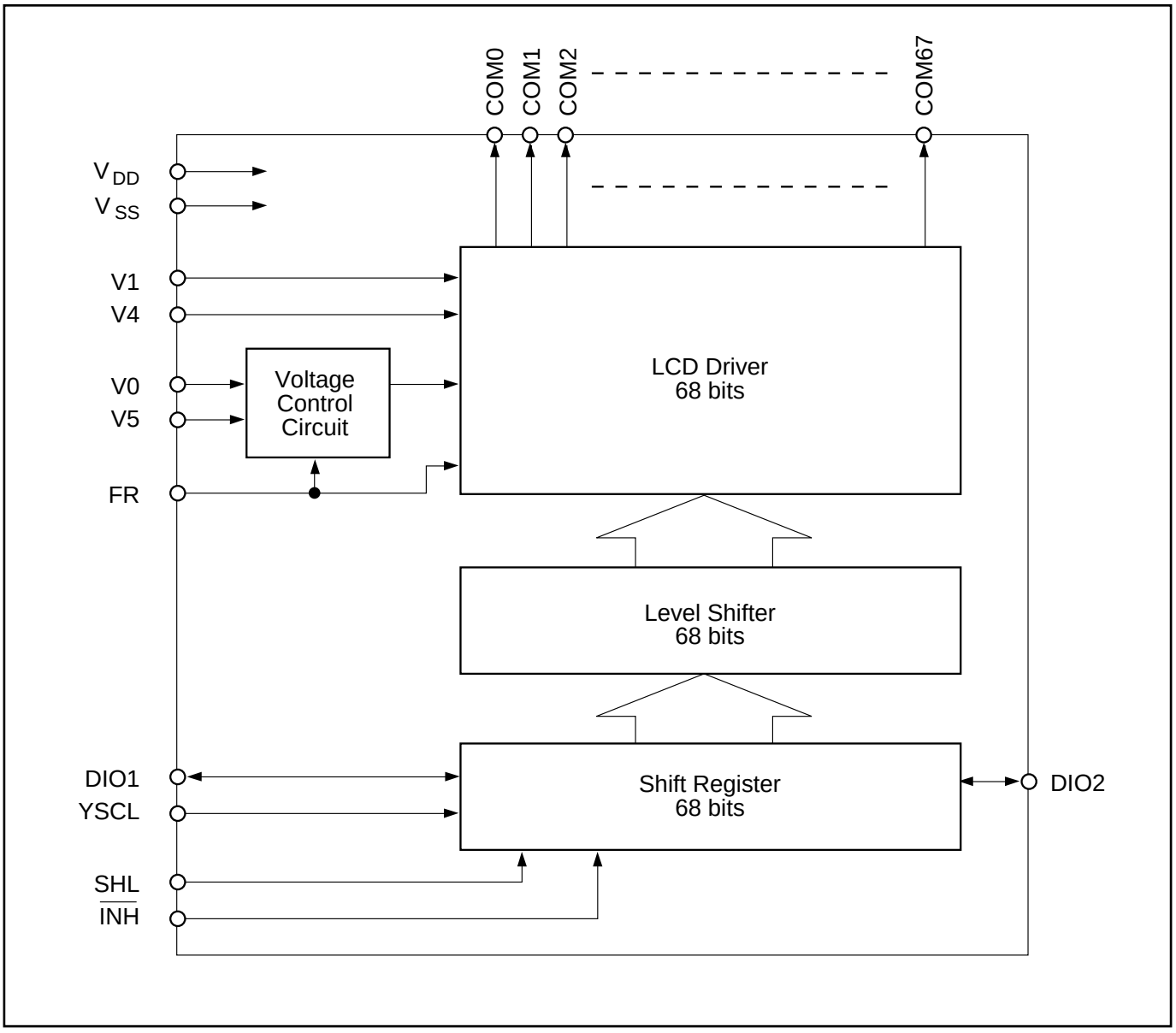
2.0 BLOCK DIAGRAMS

2.1 SYSTEM BLOCK DIAGRAM



2.2 BLOCK DIAGRAM



2.3 FUNCTIONS OF BLOCKS

2.3.1 Shift Register

Two-way shift register for transfer of common data.

2.3.2 Level Shifter

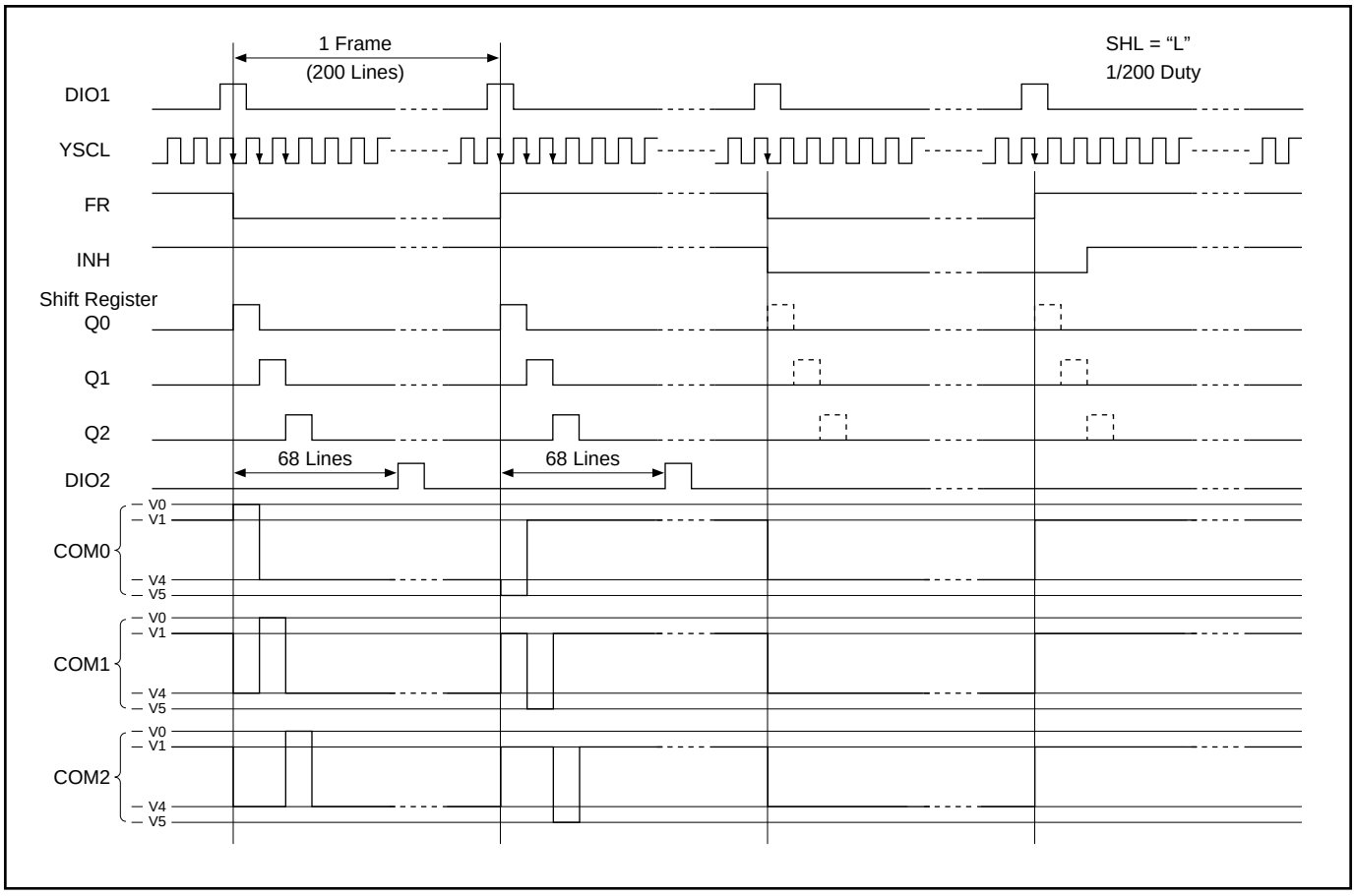
Interface circuit which converts the voltage of a signal from the logic level to the LCD driving level.

2.3.3 LCD Driver and Voltage Control

These circuits generate LCD display driving outputs. The relation between the display inhibit signal $\overline{INH}$, the contents of the shift register, the AC signal FR, and common outputs is shown below:

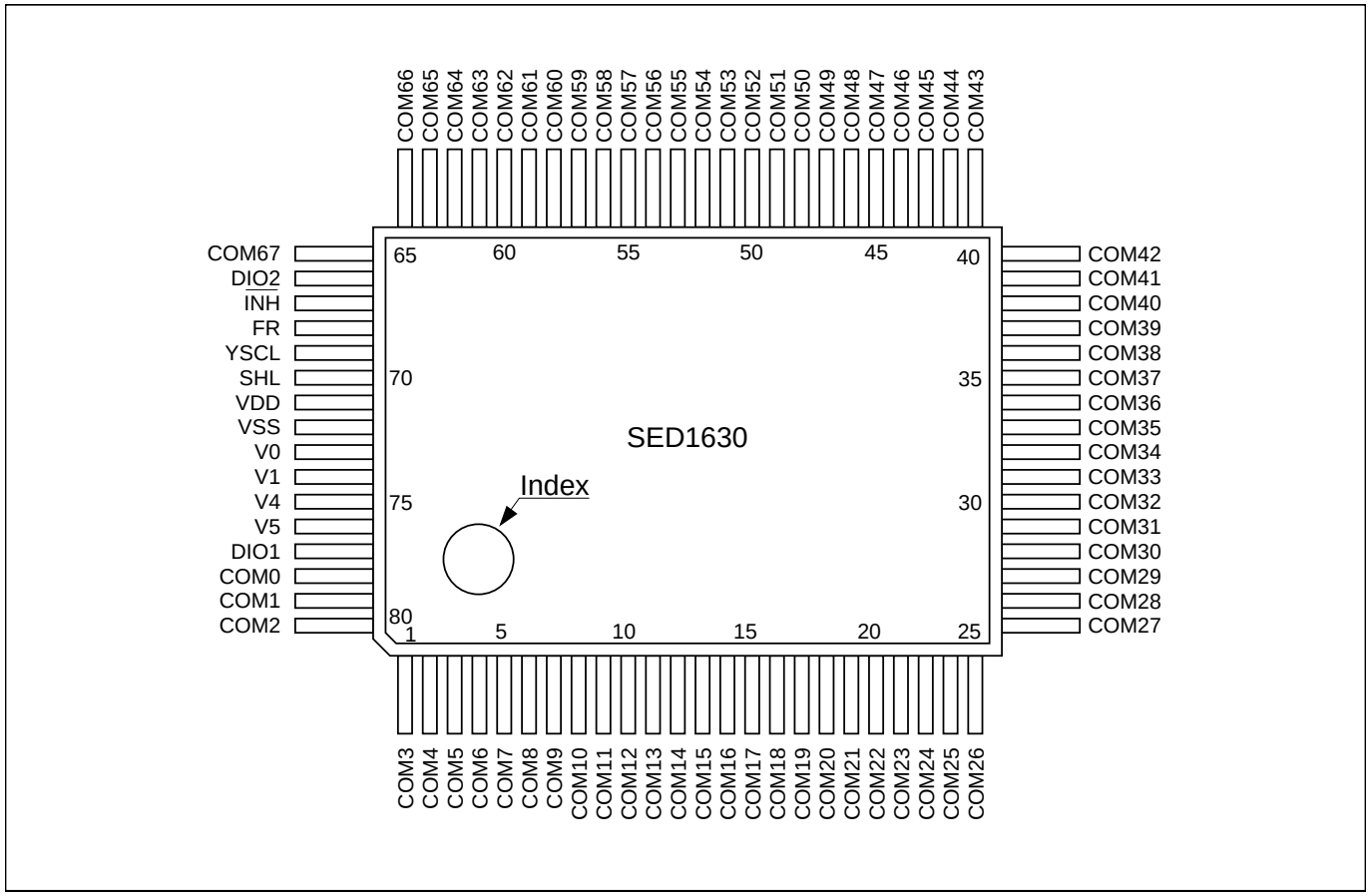
$\overline{INH}$	Contents of Shift Register	FR	COM Output Voltage	
H	H	H	V5	Select level
		L	V0	
	L	H	V1	Non-select level
		L	V4	
L	Don't care	H	V1	Non-select level
		L	V4	

2.3.4 Timing Chart



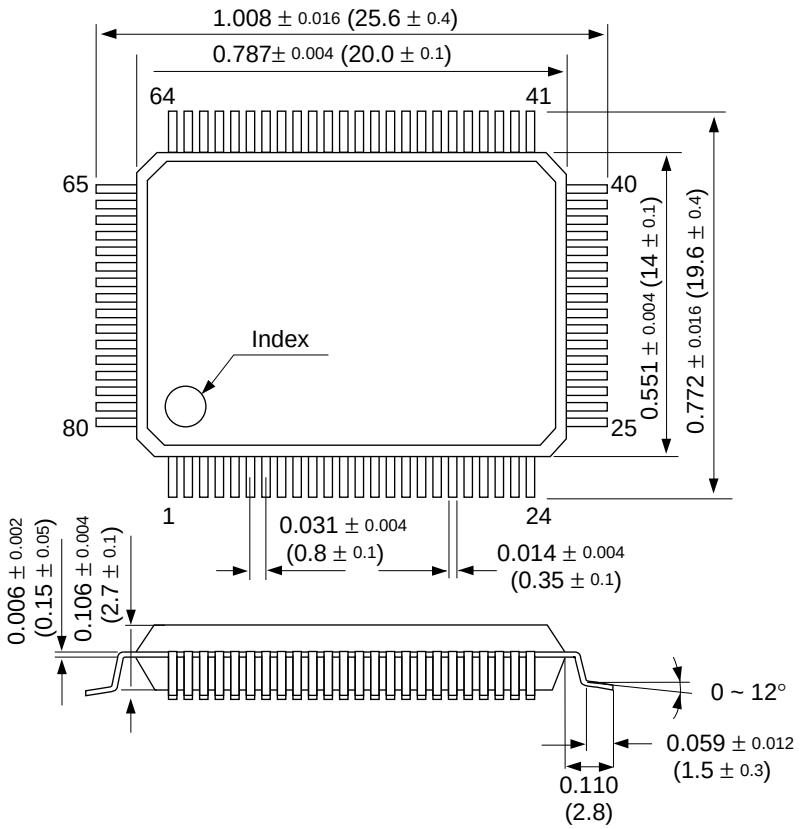
3.0 PIN CONFIGURATION

3.1 PIN CONFIGURATION



3.2 DIMENSIONS

unit: inches(mm)



3.3 PIN FUNCTIONS

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>COM0 – COM67</td><td>O</td><td>LCD driving common (row) outputs. Each output changes at the falling edge of YSCL.</td><td>68</td></tr>
<tr><td>INH</td><td>I</td><td>Blanking control input of LCD XXX Controls all common outputs to non-select level (V4 when FR = L, V1 when FR = H) (low active).</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Shift clock of serial data (falling edge trigger).</td><td>1</td></tr>
<tr><td>DIO1, DIO2</td><td>I/O</td><td>Serial transfer data I/O, which is controlled by SHL input. Output changes at falling edge of YSCL.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and DIO pin control.
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">COM output shift direction</th><th colspan="2">DIO</th></tr>
<tr><th>1</th><th>2</th></tr>
<tr><td>L</td><td>67 ← 0</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>67 ← 0</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>AC signal of LCD driving outputs</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supplies</td><td>Logic circuit power.
V_{DD}: 0V (GND)
V_{SS}: –5.0V</td><td>2</td></tr>
<tr><td>V_0, V_1, V_4, V_5</td><td>Power supplies</td><td>LCD driving power.
V_5: –12 to –28V
$V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$</td><td>4</td></tr>
</table>

Total 80

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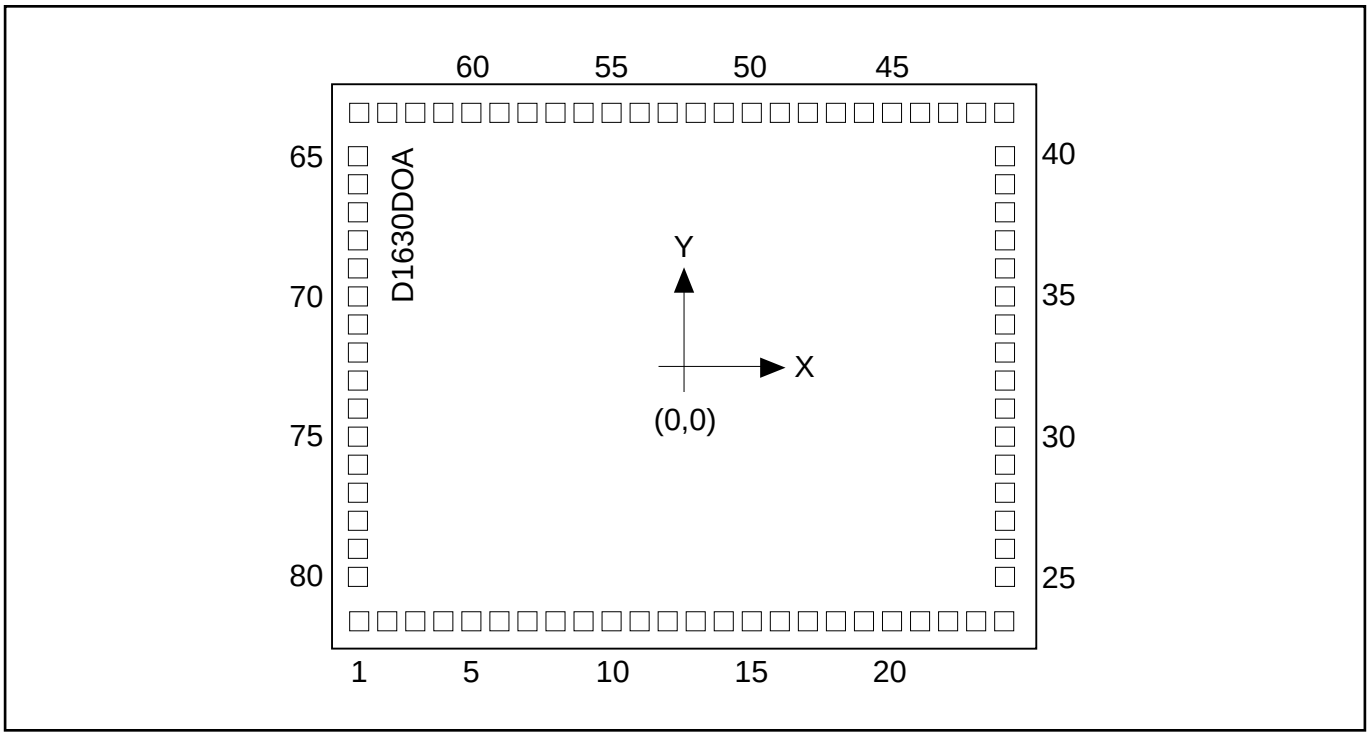
4.0 DIE CONFIGURATION

4.1 PAD LAYOUT



Chip size: 4.56mm × 3.96mm
Chip thickness: 526µm (TYP)
Hole in Pad: 107µm × 107µm

4.2 PAD COORDINATES

Unit: μm

Pad		X	Y	Pad		X	Y	Pad		X	Y
Number	Name			Number	Name			Number	Name		
1	COM3	–2120	–1820	28	COM30	2120	–924	55	COM57	–424	1820
2	COM4	–1880	–1820	29	COM31	2120	–700	56	COM58	–600	1820
3	COM5	–1680	–1820	30	COM32	2120	–500	57	COM59	–776	1820
4	COM6	–1496	–1820	31	COM33	2120	–300	58	COM60	–952	1820
5	COM7	–1312	–1820	32	COM34	2120	–100	59	COM61	–1128	1820
6	COM8	–1128	–1820	33	COM35	2120	100	60	COM62	–1312	1820
7	COM9	–952	–1820	34	COM36	2120	300	61	COM63	–1496	1820
8	COM10	–776	–1820	35	COM37	2120	500	62	COM64	–1680	1820
9	COM11	–600	–1820	36	COM38	2120	700	63	COM65	–1880	1820
10	COM12	–424	–1820	37	COM39	2120	924	64	COM66	–2120	1820
11	COM13	–254	–1820	38	COM40	2120	1148	65	COM67	–2120	1628
12	COM14	–85	–1820	39	COM41	2120	1388	66	DIO2	–2120	1388
13	COM15	85	–1820	40	COM42	2120	1628	67	$\overline{\text{INH}}$	–2120	1148
14	COM16	254	–1820	41	COM43	2120	1820	68	FR	–2120	924
15	COM17	424	–1820	42	COM44	1880	1820	69	YSCL	–2120	700
16	COM18	600	–1820	43	COM45	1680	1820	70	SHL	–2120	500
17	COM19	776	–1820	44	COM46	1496	1820	71	V_{DD}	–2120	300
18	COM20	952	–1820	45	COM47	1312	1820	72	V_{SS}	–2120	100
19	COM21	1128	–1820	46	COM48	1128	1820	73	V_0	–2120	–100
20	COM22	1312	–1820	47	COM49	952	1820	74	V_1	–2120	–300
21	COM23	1496	–1820	48	COM50	776	1820	75	V_4	–2120	–500
22	COM24	1680	–1820	49	COM51	600	1820	76	V_5	–2120	–700
23	COM25	1880	–1820	50	COM52	424	1820	77	DIO1	–2120	–924
24	COM26	2120	–1820	51	COM53	254	1820	78	COM0	–2120	–1148
25	COM27	2120	–1628	52	COM54	85	1820	79	COM1	–2120	–1388
26	COM28	2120	–1388	53	COM55	–85	1820	80	COM2	–2120	–1628
27	COM29	2120	–1148	54	COM56	–254	1820				

5.0 ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (2)	V_0, V_1, V_4	V_5 –0.3 to +0.3	V
Input pin voltage	V_I	V_{SS} –0.3 to +0.3	V
Output pin voltage (1)	V_O	V_{SS} –0.3 to +0.3	V
Output pin current (1)	I_O	20	mA
Output pin current (2)	I_{OSEG}	20	mA
Operating temperature	T_{OPR}	–20 to +75	°C
Storage temperature	T_{STG}	–65 to +150	°C
Soldering temperature · time	T_{SOL}	260 · 10	°C·sec
Allowable power dissipation	P_D	300	mW

Notes:

1. All listed voltages are based on V_{DD} = 0V.
2. Voltages V_0, V_1 and V_4 must always satisfy the condition: $V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$
3. Do not allow the logic circuit voltage to float with the LCD driving power being applied, which could otherwise lead to permanent damage to the LSI. This is especially important at system power-on or -off.
4. Generally, a flat package like the SED1610F will deteriorate in moisture resistance when immersed in solder. When installing the flat package on a board, use a way which is most unlikely to allow thermal stress on the package resin.

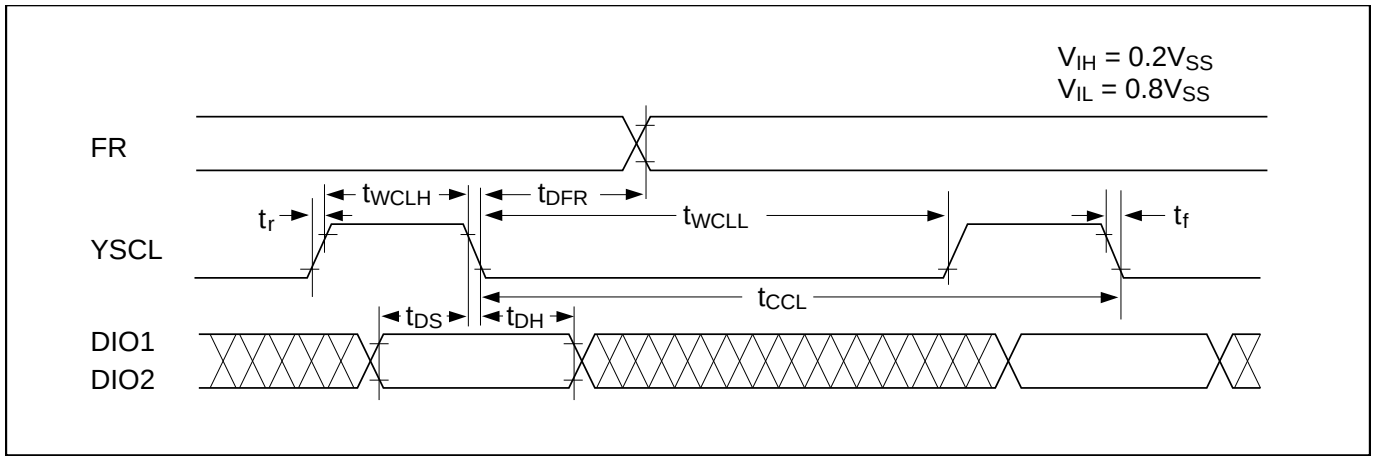
5.2 DC CHARACTERISTICS

Unless otherwise specified, V_{DD} = V_0 = 0V, V_{SS} = –5.0V ± 10%, and Ta = –20 to 75°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Pin
Supply voltage (1)	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
Recommended operating voltage	V_5			–28.0		–12.0	V	V_5
Min. operating voltage	V_5					–8.0	V	V_5
Supply voltage (3)	V_0	Recommended value		–2.5		0	V	V_0
Supply voltage (4)	V_1	Recommended value		2/9 · V_5		V_{DD}	V	V_1
Supply voltage (5)	V_4	Recommended value		V5		7/9·V_5	V	V_4
"H" input voltage	V_{IH}			0.2V_{SS}			V	DIO1,DIO2 YSCL, SHL, INH, FR
"L" input voltage	V_{IL}					0.8V_{SS}	V	
"H" output voltage	V_{OH}	I_{OH} = –0.3 mA		–0.4			V	DIO1, DIO2
"L" output voltage	V_{OL}	I_{OL} = 0.3 mA			V_{SS} + 0.4	V		
Input, I/O leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$				2.0	µA	YSCL, SHL, $\overline{INH}$, FR
	$I_{LI/O}$	$V_{SS} \le V_{IH} \le 0V$				5.0	µA	DIO1, DIO2
Static current	I_{DDS}	V_5 = –12.0 to –28.0V V_{IH} = V_{DD}, V_{IL} = V_{SS}				25	µA	V_{DD}
Output resistance	R_{COM}	| ΔVon| = 0.5V	V_5 = –20V V_5 = –14.0V V_5 = –8.0V	V_1, V_4, level output	0.40 0.50 0.60	0.80 1.00 1.20	KΩ	COM0 to COM57
			V_5 = –20.0V V_5 = –14.0V V_5 = –8.0V	V_0, V_5 level output	0.60 0.70 0.90	1.20 1.40 1.80		
Current dissipation (1)	I_{SSO1}	V_{SS} = –5.0V V_{IH} = V_{DD}, V_{IL} = V_{SS} f_{YSCL} = 12KHz Frame frequency = 60Hz Input data: "H" every 1/200 duty No-load			7	15	µA	V_{SS}
Current dissipation (2)	I_{SS02}	V_{SS} = –5.0V, V_1 = –2.0V V_4 = –18.0V, V_5 = –20.0V All other conditions are same as I_{SS1}		7	15	µA	V5	
Input, I/O pin capacitance	CI	Ta = 25°C				8	pF	YSCL, SHL $\overline{INH}$, FR
	CI/O					15	pF	DIO1, DIO2

5.3 AC CHARACTERISTICS

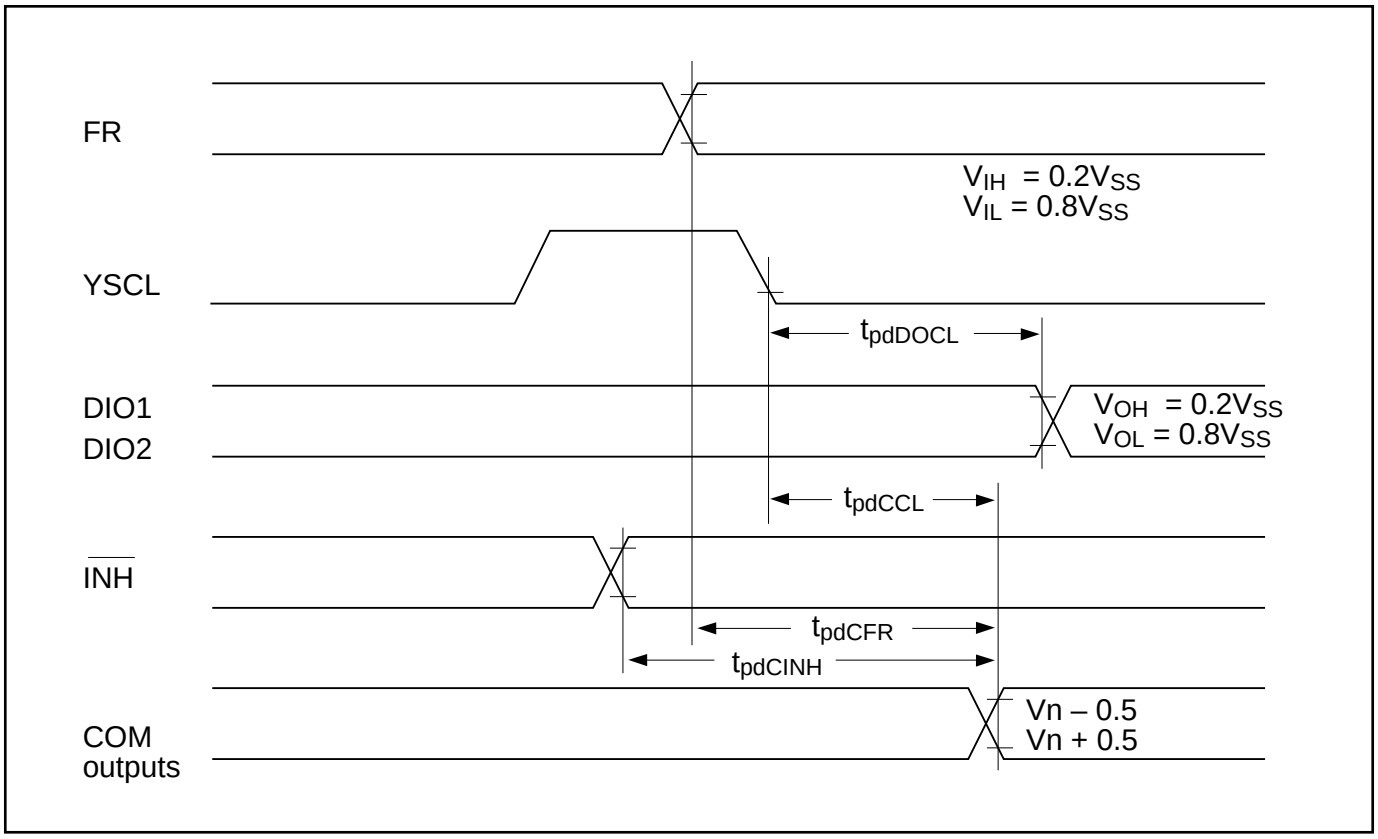
5.3.1 Input Timing



Ta = –20 to 75°C, V_{SS} = –5.0V ± 10%

Parameter	Symbol	Condition	Min.	Max.	Unit
YSCL period	t_{CCL}		500		ns
YSCL “H” pulse width	t_{WCLH}		70		ns
YSCL “L” pulse width	t_{WCLL}		330		ns
Data setup time	t_{DS}		100		ns
Data hold time	t_{DH}		10		ns
Allowable FR delay time	t_{DFR}		–500	500	ns
Input signal rise time	t_r			50	ns
Input signal fall time	t_f			50	ns

5.3.2 Output Timing



Ta= –20 to 75°C, V_{SS} = –5.0V ± 10%

Parameter	Symbol	Condition	Min.	Max.	Unit
(YSCL-fall to DIO) delay time	tpdDOCL	CL = 15pF	30	300	ns
(YSCL-fall to COM output) delay time	tpdOCL	V5 = –12.0 to –28.0V CL = 100pF		3.0	µs
(INH to COM output) delay time	tpdCINH				
(FR to COM output) delay time	tpdCFR			3.0	µs

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6.0 LCD DRIVING POWER SUPPLY

6.1 FORMING VOLTAGE LEVELS

The simplest way of obtaining each voltage level for driving LCDs is to apply resistance division technique. Each voltage level must be sufficiently accurate and stable to provide high-quality display. For this, the divided resistance must be set to as low a value as possible within the capacity of system power.

Especially where low power dissipation is of primary concern, it is recommended to have each level driven by an operational amplifier in the form of a voltage follower rather than setting a high divided resistance. To allow for using an operational amplifier for the above purpose, the highest voltage level V_0 for LCD driving in the SED1610F is isolated from V_{DD}. However, it is recommended to use $V_{DD} – V_0$ in the range 0 to 2.5V because the larger the potential difference between V_{DD} and V_0, the lower the LCD driving output capability. The circuit $V_0 – V_{DD}$ must be shorted if no operational amplifier is used.

6.2 POWER-ON/-OFF

The SED1610F LSI uses high voltages to drive LCDs. If a high voltage is applied to the LCD driving circuit with the logic circuit power held floating, a large current will flow into the LSI, sometimes causing damage to it.

Be sure to take the following procedure when turning power on or off:

Power-on: Logic circuit on $\rightarrow$ LCD drive circuit on, or both circuits on at the same time.

Power-off: LCD drive circuit off $\rightarrow$ logic circuit off, or both circuits off at the same time.

Connect a protection resister of more than 200 Ω in series to V_5 to prevent overcurrent.

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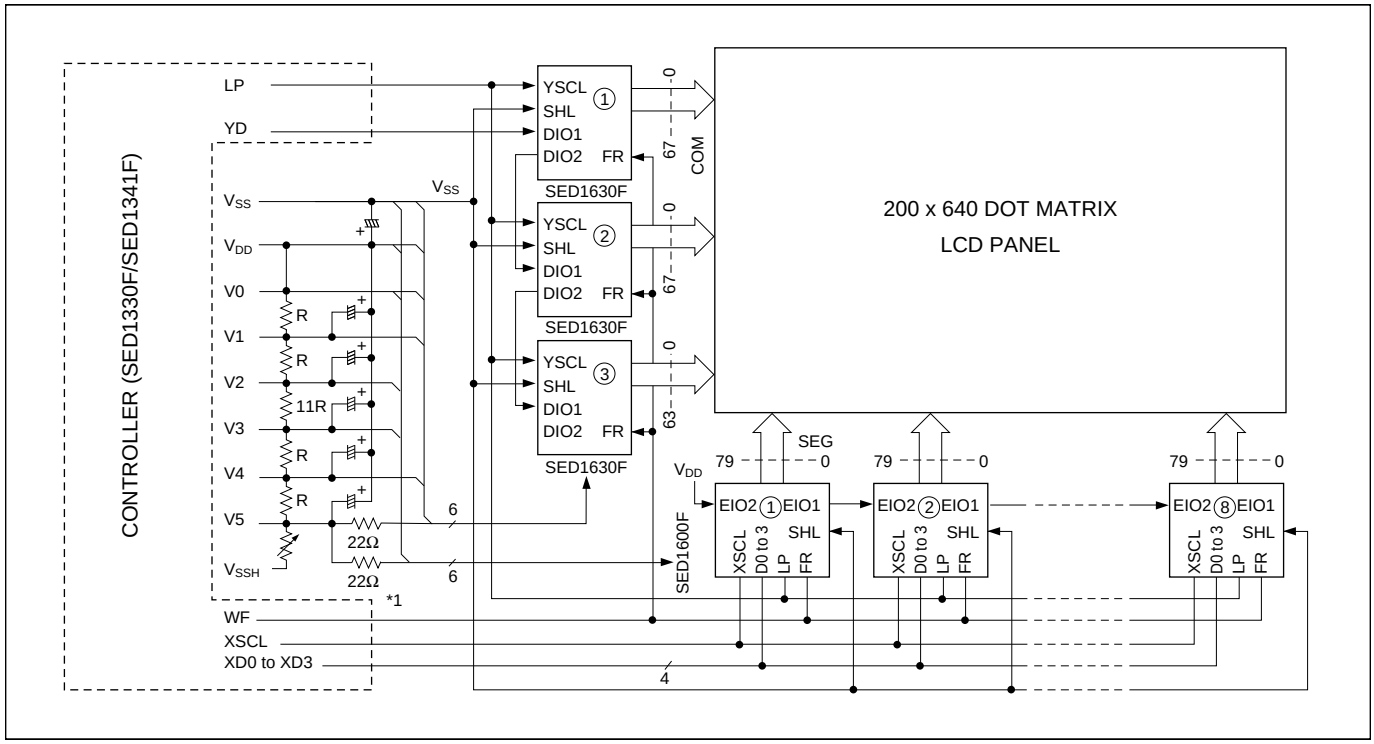
7.0 TYPICAL CONNECTION

7.1 200 × 640 DOT MATRIX LCD



Note: * Be sure to connect an overcurrent protection resistor. Also, connect bypass capacitors (c) (0.01 μF) near pins V_{SS} and V_5 of each LSI for noise protection.

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