SED1753

CMOS LCD COMMON DRIVER

■ DESCRIPTION

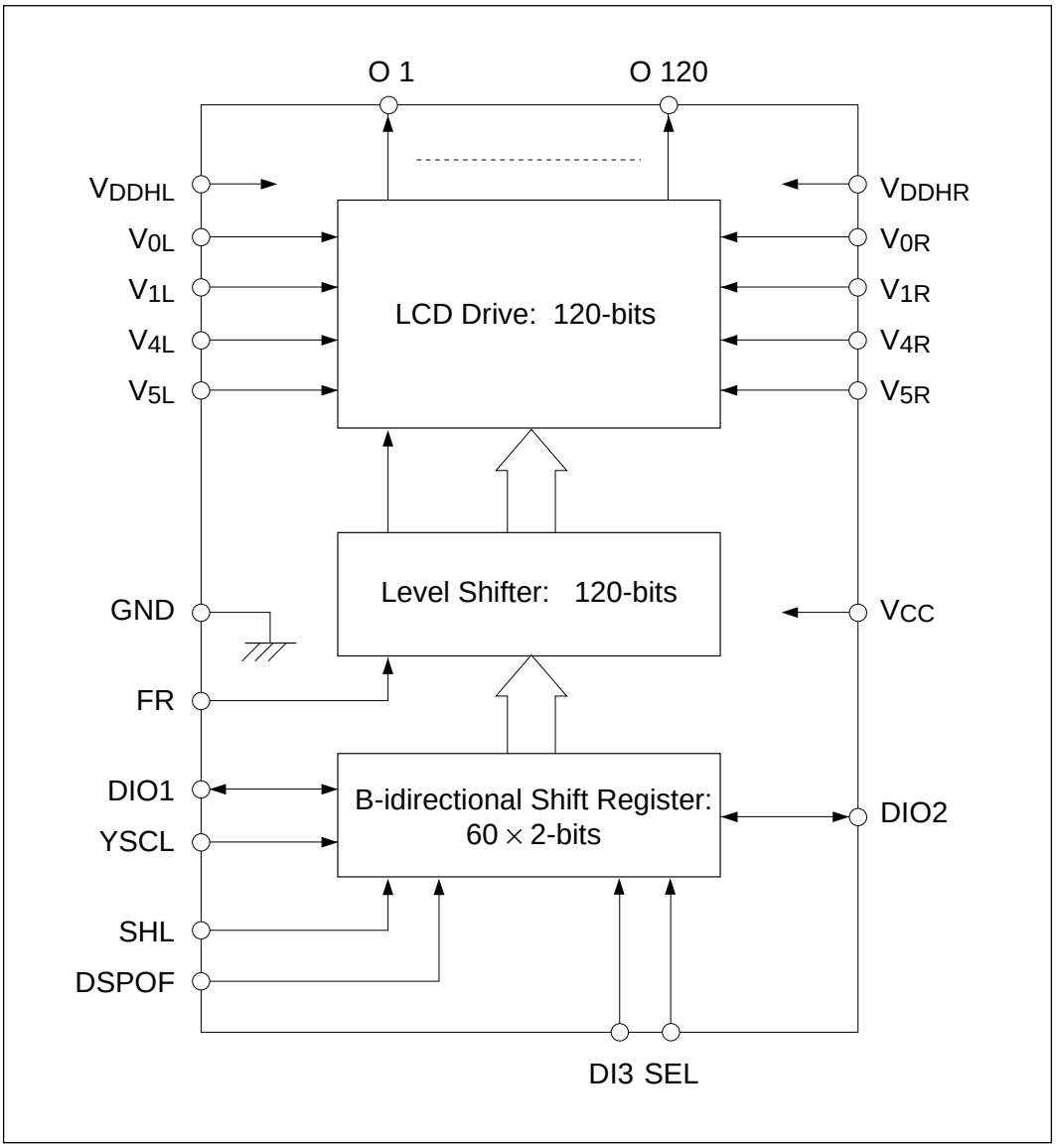
The SED1753 is an LCD common (row) driver designed for extremely high-capacity dot matrix liquid crystal panels. It incorporates 120 high-voltage, low-impedance common drivers in a 2×60 format, enabling high driver effectiveness with displays of 1/240, 1/300 and 1/480 duty cycles. It is designed for use in conjunction with the SED1752 and SED1758 segment (column) drivers.

The SED1753 features a wide range of liquid crystal drive voltages, an LCD display of high quality and slim configuration to minimize the LCD panel. It offers a wide range of applications.

■ FEATURES

- 120 (60×2) LCD common drive outputs
- 0.3KΩ (typ.) low output impedance
- High-duty drive available 1/480
- Pin-selectable output shift direction
- Zero-bias display disable function
- Slim configuration
- Adjustable LCD drive voltage
- Liquid crystal drive in wide range of voltage: 8 to 42V
- 2.7 to 5.5V supply
- Package: ..... D0B ..... Au bump die
  T0A ..... TAB package

■ **BLOCK DIAGRAM**



■ FUNCTIONS

● Shift Register

This is a bi-directional shift register for transmitting common data. The shift register has a 60 × 2 bit structure, and a 60 × 2 bit or 120-bit structure can be selected depending on the state of SEL.

When a 60 × 2 bit structure is selected, the lower-stage 60-bit shift register input becomes DI3.

● Level Shifter

This is a voltage level interface circuit for converting the signal voltage level from a logic-system level to an LCD drive-system level.

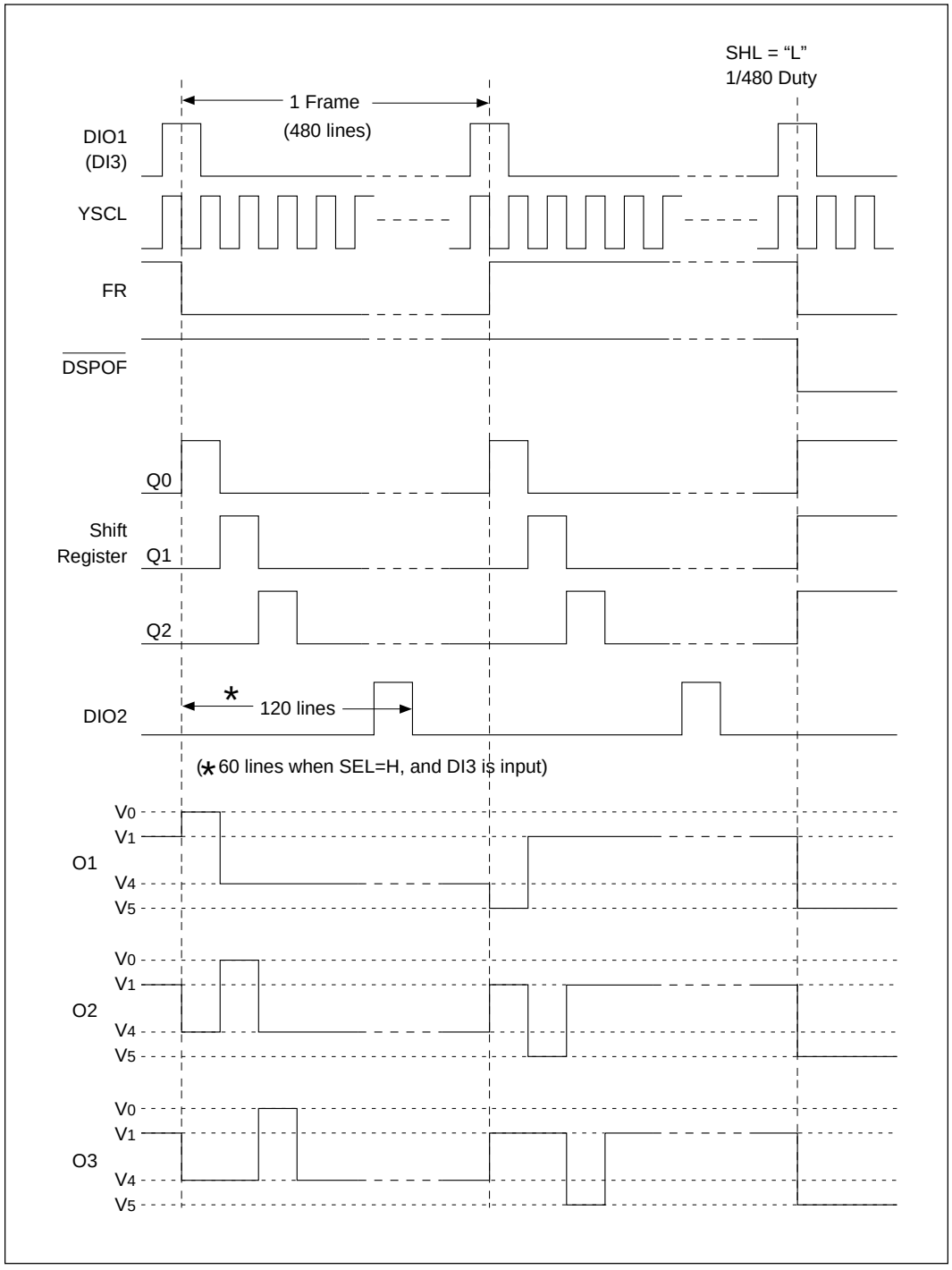
● LCD Driver

These output the LCD driver voltages.

The relationship between the display blanking signal $\overline{DSPOF}$, the contents of the shift register, the alternating signal FR, and the common output voltage is as shown below:

$\overline{DSPOF}$	Contents of Shift Register	FR	ON Output Voltage	
H	H	H	V_5	(Selected level)
		L	V_0	
	L	H	V_1	(Non-selected level)
		L	V_4	
L	—	—	V_5	—

■ **TIMING CHART**



■ EXPLANATION OF TERMINALS

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>No. of Terminals</th></tr>
<tr><td>O 1 to
O 120</td><td>O</td><td>LCD drive common (row) output.
Changes on the falling edge of YSCL</td><td>120</td></tr>
<tr><td>DIO1
DIO2</td><td>I/O</td><td>Set to input or to output by the scanning pulse SHL Input
of the 60 x 2 bit bi-directional shift register.
The output changes on the falling edge of YSCL</td><td>2</td></tr>
<tr><td>DI3</td><td>I</td><td>DI3 is a scan pulse input when a 60 x 2 structure is used.
When SEL = L, DI3 is connected to ground.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Bi-directional shift register operating mode select input.
H: 60 x 2 (DI3 input); L: 120</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input.
The scan data is shifted with the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and DIO terminal input/output
control output
<table>
<tr><th>SHL</th><th>0 Ouput Shift Direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>H</td><td>1 → 60 61 → 120</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>120 → 61 60 → 1</td><td>Output</td><td>Input</td></tr>
</table></td><td></td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>LCD display blanking control input.
When “L”, all common outputs are set to the V5 level.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output alternating signal input.</td><td>1</td></tr>
<tr><td>GND, V_{CC}</td><td>Power supply</td><td>Power supply for logic: GND: 0V V_{CC} + 2.7 to 5.5V</td><td>2</td></tr>
<tr><td>V_{OL}, V_{IL}, V_{4L},
V_{5L}, V_{DDH},
V_{OR}, V_{1R}, V_{4R},
V_{5R}, V_{DDHR},</td><td>Power supply</td><td>Power supply LCD drive
GND: 0V, V_{DDH}: 8V to 42V
$V_{DDH} \geq V0 \geq 8/9V_{DDH}$
$1/9V_{DDH} \leq V4 \geq V5 \geq GND$
*1</td><td>10</td></tr>
<tr><td></td><td></td><td>Total</td><td>140 pins</td></tr>
</table>

*1. V_{DDH} and V_0 to V_5 pairs must be connected to their respective LC power supplies. The LC drive circuit power supply voltage ranges are specification recommended values.

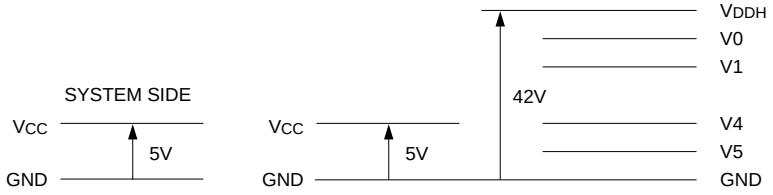
■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Rating

Parameters	Symbol	Rating	Units
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Power supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Power supply voltage (3)	V_0, V_1, V_4, V_5	GND – 0.3 to V_{DDH} +0.3	V
Input voltage	V_I	GND – 0.3 to V_{CC} +0.3	V
Output voltage	V_O	GND – 0.3 to V_{CC} +0.3	V
DIO output current	I_{O1}	20	mA
Operating temperature	Topr	–40 to +85	°C
Chip storage temperature	Tstg[1]	–65 to +150	°C
TCP product storage temperature	Tstg[2]	–55 to +125	°C

Note 1. All the above voltages are based on GND = 0V.

Note 2. V_0, V_1, V_4 and V_5 voltages must always fulfill the following relationship: $V_{DDH} \geq V_0 \geq V_1 \geq V_4 \geq V_5 \geq GND$



Note 3. Permanent damage to the LSI may result if the logic power supply is floating or falls below V_{CC} = 2.6V when the LCD drive power supply is supplied. Special caution is required during the System Power OFF and System Power ON sequencing.

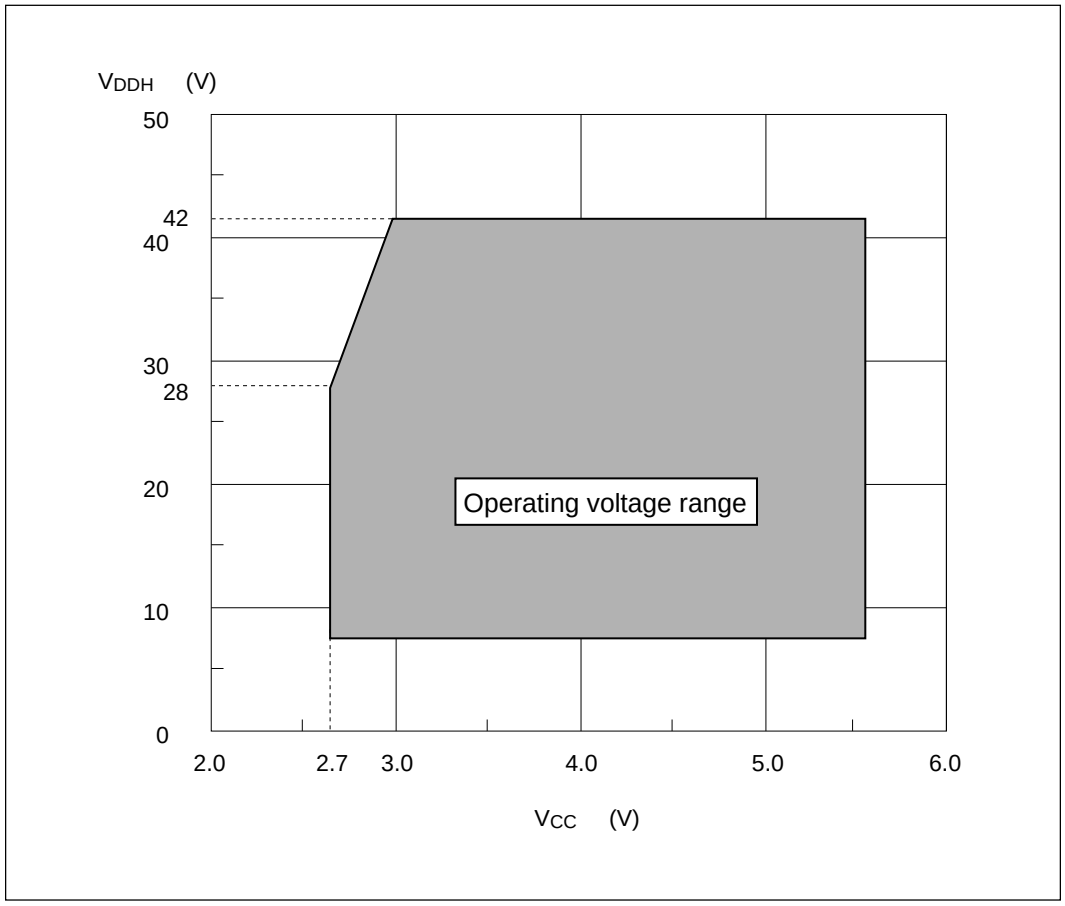
- **DC Characteristics**

Unless otherwise designated, GND = V_5 = 0V, V_{CC} = 5.0V ± 10%, T_a = –40 to 85°C

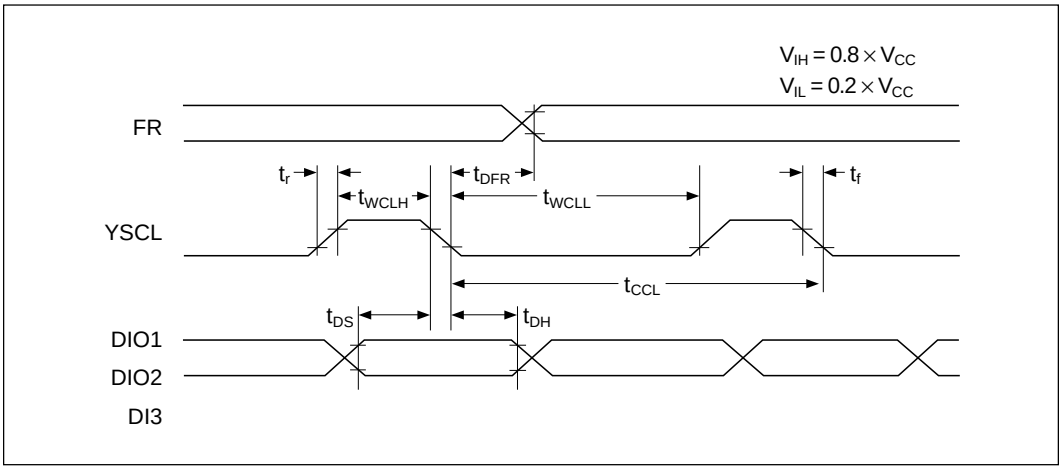
Parameter	Symbol	Condition		Applicable Pin	Min	Typ	Max	Unit
Electrical voltage (1)	V_{CC}	—		V_{CC}	2.7	5.0	5.5	V
Recommended working voltage	V_{DDH}	V_{CC} = 2.7 to 5.5 V		V_{DDHL}, V_{DDHL}	14.0	—	40.0	V
Possible operating voltage	V_{DDH}	Function		V_{0L}, V_{OR}	8.0	—	42.0	V
Power supply voltage (2)	V_1	Recommended value		V_1L, V_1R	8/9 V_{DDH}	—	V_{DDH}	V
Power supply voltage (3)	V_4	Recommended value		V_4L, V_4R	GND	—	1/9 V_{DDH}	V
High level input voltage	V_{IH}	V_{CC}= 2.7~ 5.5V		DIO1,DIO2, FR	0.8 V_{CC}	—	—	V
Low level input voltage	V_{IL}			YSCL, SHL, DI3 $\overline{DSPOF}$, SEL	—	—	0.2 V_{CC}	V
High level output voltage	V_{OH}	V_{CC} = 2.7~5.5V	I_{OH} = –0.3mA	EIO1, EIO2,	V_{CC}–0.4	—	—	V
Low level output voltage	V_{OL}		I_{OL} = 0.3mA		—	—	GND+0.4	V
Input leakage current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		YSCL, SHL, DI3 $\overline{DSPOF}$, FR, SEL	—	—	2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		EIO1, EIO2	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = 14.0 ~ 42.0V V_{IH} = V_{CC}, V_{IL} = GND		GND	—	—	25	µA
Output resistance	R_{COM}	ΔV_{ON} = 0.5V Ta = 25°C	V_{DDH} = +36.0V, 1/24	O1~ O120	—	0.29	0.48	KΩ
			V_{DDH} = +26.0V, 1/20		—	0.3	0.5	
Resistance chip-internal BIOS	ΔR_{COM}	V_{DDH} = +36.0V, 1/24			—	—	50	Ω
Average operating current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC} V_{IL} = GND, f_{YSCL} = 33.6KHz f_{LP} = 70Hz, Input data: 1/480 Ta = 25°C No load		V_{CC}	—	TBD	TBD	µA
		V_{CC} = +3.0V All other conditons are the same as with V_{CC} = –5.0V			—	TBD	TBD	
Average operating current consumption (2)	I_{DDH}	V_{DDH} = V_0 = 30.0V V_1 = 28.0V V_4 = 2.0V, V_5 = 0.0V, V_{CC} = 5.0V Other conditions are the same as with the item I_{CC}.		V_{DDHL}, V_{DDHR}	—	TBD	TBD	µA
Input terminal capacity	CI	Freq. = 1 MHz Ta = 25°C Chips alone	YSCL, SHL, $\overline{DSPOF}$, FR, DI3, SEL		—	—	8	pF
I/O terminal capacity	$C_{I/O}$		DIO1, DIO2		—	—	15	pF

- **Range of Operating Voltages: V_{CC} – V_{DDH}**

  It is necessary to set the voltage for V_{DDH} within the V_{CC} – V_{DDH} operating voltage range shown in the diagram below.



- **AC Characteristics**
  - **Input Timing Characteristics**



V_{CC} = +5.0V ± 10%, T_a = –40 to 85°C

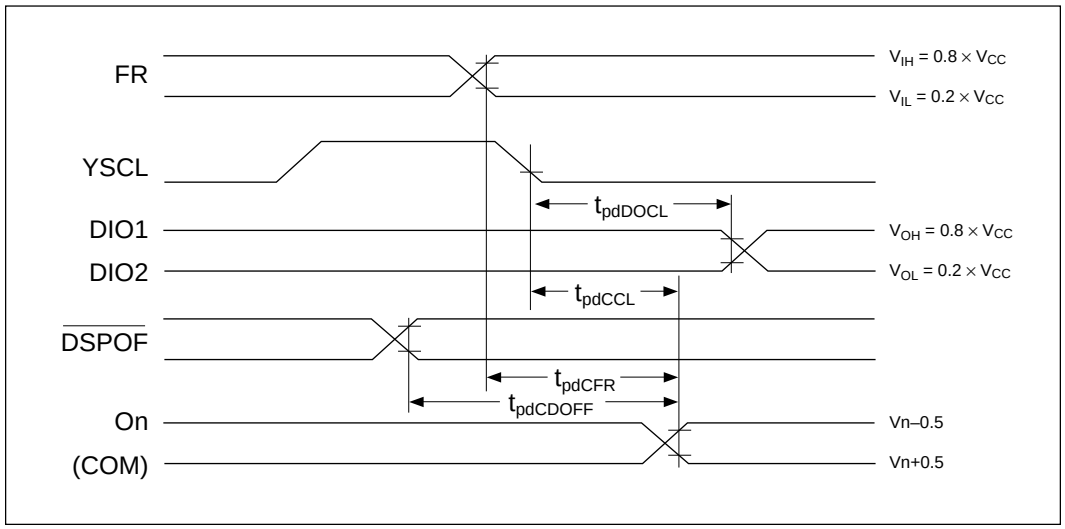
Parameter	Symbol	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}	—	400	—	ns
YSCL high level pulse duration	t_{WCLH}	—	60	—	ns
YSCL low level pulse duration	t_{WCLL}	—	330	—	ns
Data setup time	t_{DS}	—	50	—	ns
Data hold time	t_{DH}	—	40	—	ns
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns

V_{CC} = 2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}	—	800	—	ns
YSCL high level pulse duration	t_{WCLH}	—	80	—	ns
YSCL low level pulse duration	t_{WCLL}	—	660	—	ns
Data setup time	t_{DS}	—	90	—	ns
Data hold time	t_{DH}	—	70	—	ns
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns

Note: *1. The timing for the FR signal transition point (t_{DFR}: FR) and the LP signal falling edge is, essentially, 0 ns; set these in a range where the ON output wave form is not distorted.

○ **Output Timing Characteristics**



V_{CC} = 5.0V ± 10%, V_{DDH} = 14.0 to 42.0V, ta = –40 to +85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
Delay time from YSCL falling edge to DIO	t_{pdDOCL}	C_L = 15 pf	—	100	ns
Delay time from YSCL falling edge to ON output	t_{pdCCL}	C_L = 100 pf	—	200	ns
Delay time from $\overline{DSPOF}$ to ON output	$t_{pdCDOFF}$				
Delay time from FR to ON output	t_{pdCFR}		—	300	ns

V_{CC} = 2.7V to 4.5V, V_{DDH} = 14.0 to 28.0V, ta = –40 to +85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
Delay time from YSCL falling edge to DIO	t_{pdDOCL}	C_L = 15 pf	—	200	ns
Delay time from YSCL falling edge to ON output	t_{pdCCL}	C_L = 100 pf	—	400	ns
Delay time from $\overline{DSPOF}$ to ON output	$t_{pdCDOFF}$				
Delay time from FR to ON output	t_{pdCFR}		—	600	ns

Notes: *1. The input signal t_r, t_f is fixed to 20ns.

*2. High speed operation of the shift clocks (XSCL) should be made only under a condition of t_r or $t_f \leq \{t_C - (t_{DCL} + t_{SUE})\}/2$.

■ THE LIQUID CRYSTAL DRIVE POWER SUPPLY

● Forming the Various Voltage Levels

The most appropriate method for obtaining the various voltage levels for driving the LCD is to use resistive voltage dividers for the voltage levels between V_{DDH} and GND, and to drive the voltage levels using voltage followers employing op amps.

Considering the use of the op amp, V_{DDH} and V_0, the lowest voltage level for driving the LCD, and GND and V_5, the lowest voltage for driving the LCD, are separated from each other and given separate pins.

Normally, V_0 and V_{DDH} are connected, as are V_5 and GND, and V_1 and V_4 are driven using voltage followers. When V_0 is driven using a voltage follower, the ability of the LSI to drive the LCD outputs diminishes when the level of V_0 is higher than that of V_{DDH} and the difference in the voltage levels is great; thus the voltage difference between V_{DDH} and V_0 should be kept in the range of 0V to 2.5V.

When there is a serial resistance between the GND and V_{DDH} power supply lines, the voltage between GND and V_{DDH} is reduced at the LSI power terminals because of the I_{DDH} when the signals change, which may lead to permanent damage to the LSI if the relationships between the LCD voltage levels does not follow the formula: $V_{DDH} \geq V_0 \geq V_1 \geq V_4 \geq V_5 \geq GND$.

When a guard resistance is used, it is necessary to stabilize the voltage with a capacitor.

● Power Supply Stabilization

When necessary to prevent the effects of noise arising from the power supply signal line leads in packaging on the circuit board, a bypass capacitor between the power supplies (GND – V_{CC}, GND – V_{DDH}) may be required in order to stabilize the voltages.

● Cautions Regarding Turning the Power Supply ON and OFF

Because the voltage in the LCD drive system of this LSI is high, the LSI may be permanently damaged by an overcurrent situation when LCD drive signals are output before the LCD drive system applied voltage is stabilized, or when the LCD drive system high-voltage is applied while the logic system power supply is floating or when V_{CCS} is less than 2.6V. It is recommended that the display OFF function $\overline{DSPOFF}$ be used until the LCD drive system voltage stabilized, and that the LCD drive output voltage level be at the V_5 level.

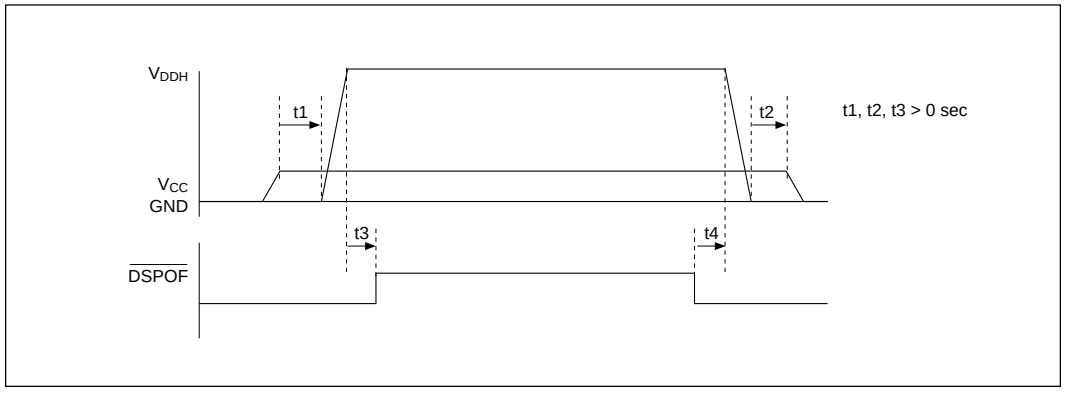
Please follow the following sequences when turning the power supplies ON and OFF:

Power Supply ON:

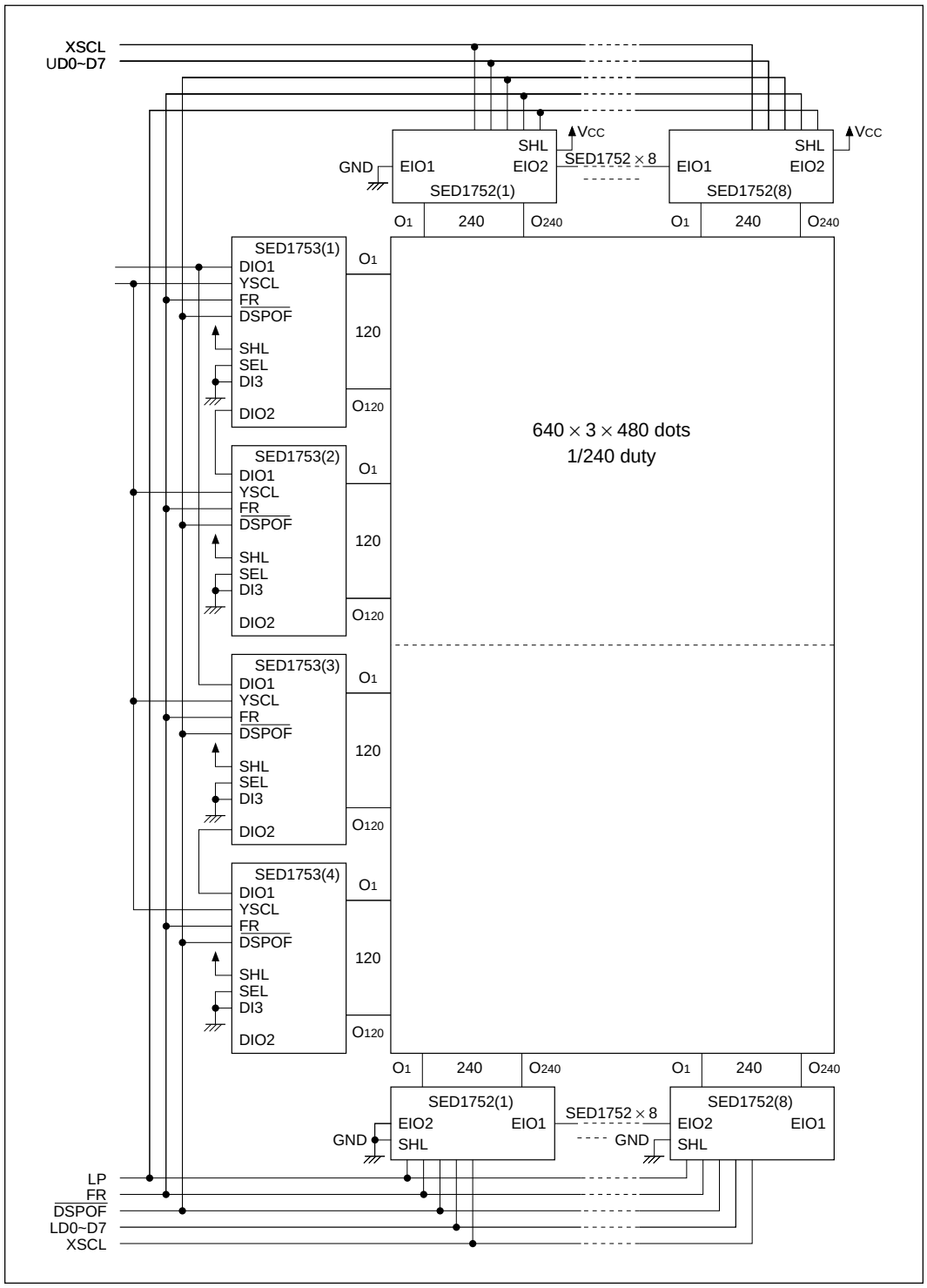
Logic system ON → LCD drive system ON (or simultaneous)

Power Supply OFF:

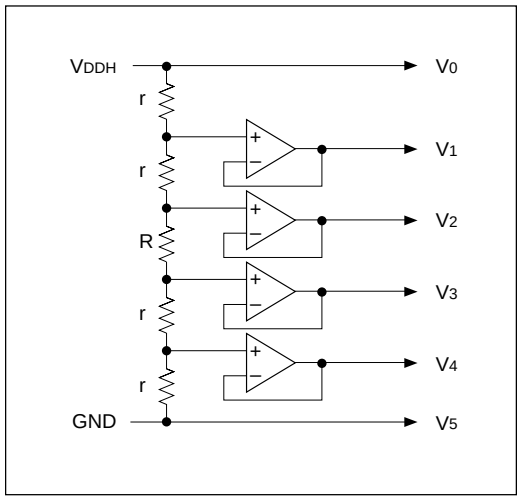
LCD drive system OFF → Logic system OFF (or simultaneous)



■ **EXAMPLE OF REFERENCE CIRCUIT**

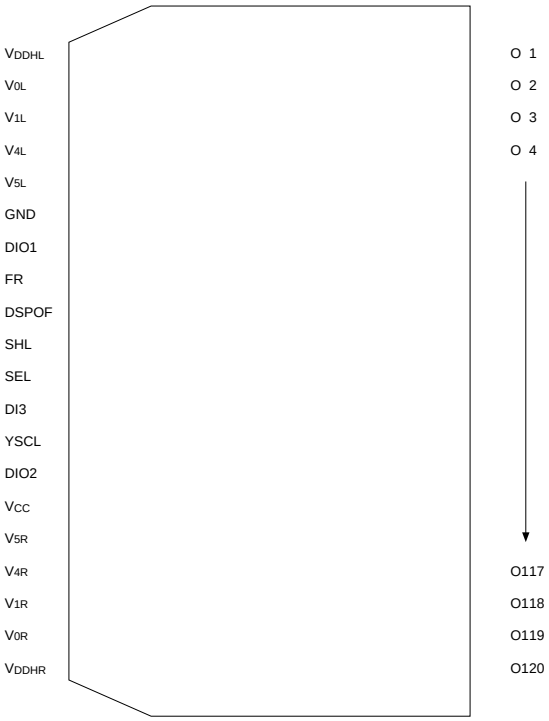


- **Example of LCD Power Supply Circuits**



- The LCD drive power supply (V_0 – V_5) requires the addition of smoothing capacitors on the appropriate places in the LCD module.
- V_0, V_1, V_4 and V_5 are supplied to SED1753, and V_0, V_2, V_3 and V_5 are supplied to SED1752.
- The logic power supply V_{CC} is supplied to all ICs.
- It is necessary to add bypass capacitors to the appropriate locations between GND – V_{CC} and GND – V_{DDH} to eliminate noise, thereby stabilizing the power supply voltage. It is recommended that the power supplies for high-voltage application (GNDR, GNDL) use a different system than the lines for the power supplies for logic (GND).

- **TCP**
  - **An SED1753T** TCP Pinout Example**



Note: The external dimensions of the TCP are not specified.

- **External Dimension Diagram**