SED1733

- **CMOS 100-Bit Common Driver**
- **High-Voltage LCD Driver**

■ DESCRIPTION

The SED1733 is a 100-bit output LCD common (row) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of LCD drive voltages.

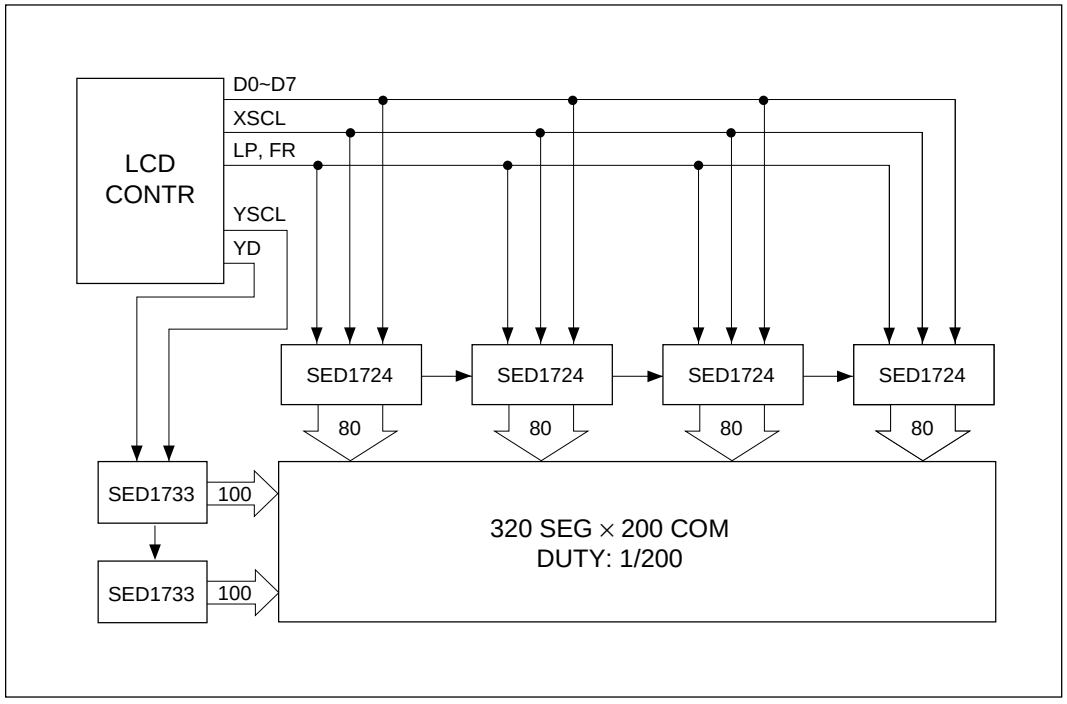
The device uses a high-speed daisy-chain enable system which decreases power consumption and eliminates the need for separate signals for each driver.

The SED1733 is used in conjunction with the SED1722 or SED1724 segment drivers to support a large-capacity dot matrix LCD panel.

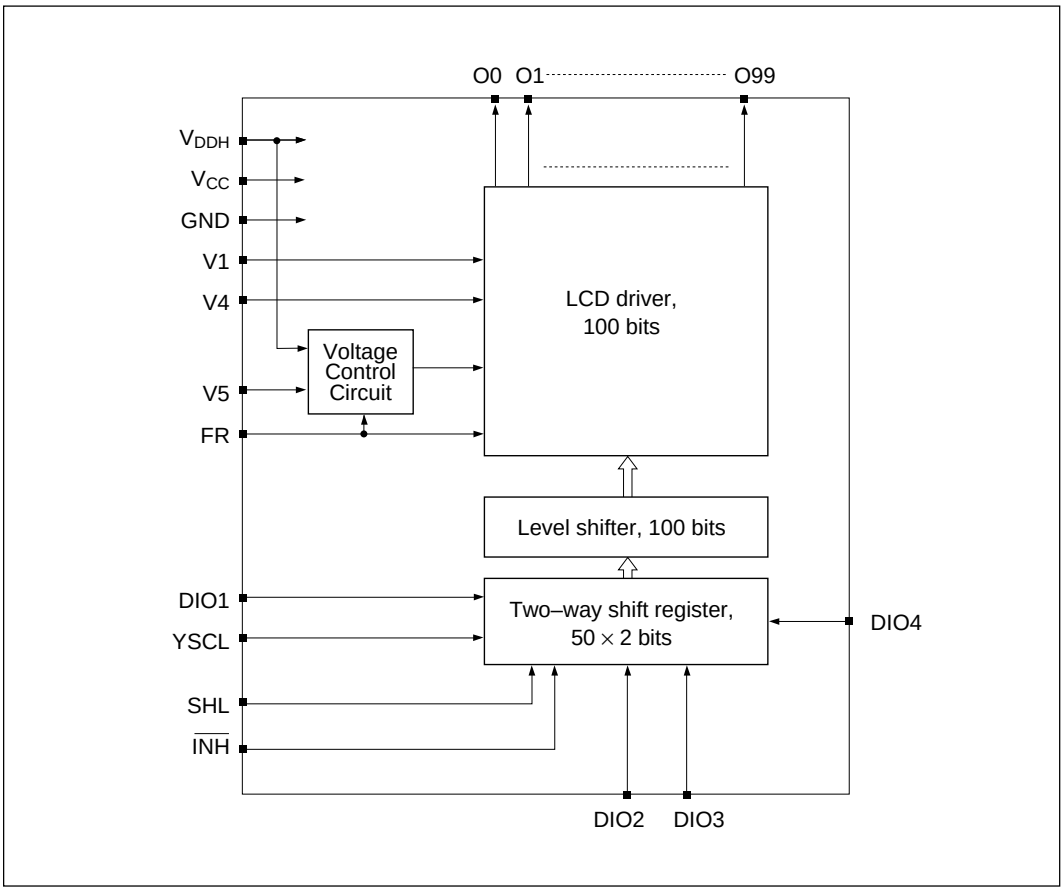
■ FEATURES

- Low-power high-speed CMOS technology
- 100-bit common (row) driver
- Duty cycle ..... 1/100 to 1/500
- Adjustable LCD drive voltages
- Selectable output shift direction
- Supports display blanking
- Supports high-speed data transfer
- Low output resistance
- Ability to adjust offset bias of the LCD source from V_{DD}
- Wide range of LCD voltage .... 14 to 40V
- Supply voltage ..... 4.5 to 5.5V
- Package ..... QFP-5 128 pins (F_{OA})
  Al pad (D_{OA})

■ SYSTEM BLOCK DIAGRAM



■ **BLOCK DIAGRAM**



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Q'ty</th></tr>
<tr><td>O0 to O99</td><td>O</td><td>LCD crystal common (row) outputs
The output changes at the YSCL fall edge.</td><td>100</td></tr>
<tr><td>DIO1, DIO2
DIO3, DIO4</td><td>I/O</td><td>To input and output serial data of 50 × 2 bits two-way shift register.
Input or output is set by SHL input. Output changes at the YSCL fall edge.</td><td>4</td></tr>
<tr><td>YSCL</td><td>I</td><td>To input shift clock of serial data. Scanning data is shifted at the fall edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>To input the selection of shift direction and input-output control of DIO terminal.
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">O (Output shift direction)</th><th colspan="2">DIO</th></tr>
<tr><th>1,3</th><th>2,4</th></tr>
<tr><td>L</td><td>0 → 99</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>99 → 0</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>To input blanking control of liquid crystal display.
Low level input brings all common outputs to non-section level.
<table>
<tr><th>$\overline{INH}$</th><th>FR</th><th>O0 to O99</th></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>To Input AC signal of liquid crystal driving output.</td><td>1</td></tr>
<tr><td>V_{CC}, GND</td><td>Power Supply</td><td>Logic power supply. GND: 0 V; V_{CC}: +5.0 V</td><td>2</td></tr>
<tr><td>V1, V4, V5,
V_{DDH}</td><td>Power Supply</td><td>Power supply for liquid crystal driving
V_{DDH}: +14 V to +40 V; $V_{DDH} \geq V1 \geq 8/9\ V_{DDH}$; $1/9\ V_{DDH} \geq V4 \geq V5 \geq V_{DDH}$,
V_{DDH}, V5: Selection level, V1, V4: Non-selection level</td><td>4</td></tr>
</table>

Total: 114 pins

■ FUNCTIONAL DESCRIPTION

- **Shift Register**

  Bidirectional data shift register.

- **Level Shifter**

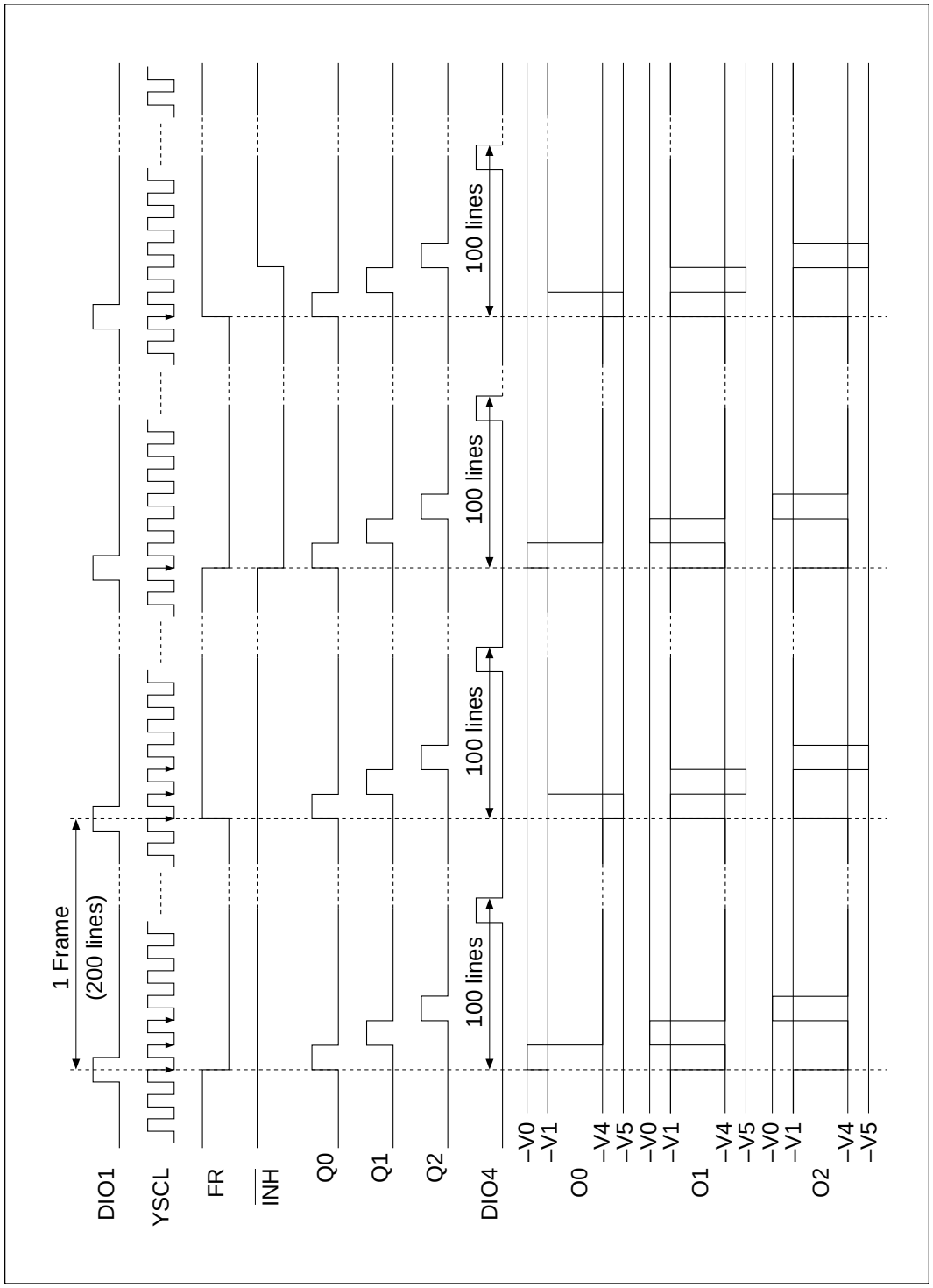
  The level shifter converts the logic-level signals from the latch to the voltage levels required by the LCD drivers.

- **LCD Drivers and Voltage Control Circuit**

  The LCD drivers drive individual columns of the display matrix with the voltage determined by the inhibit signal /INH, the frame signal FR, and the latched display data. This is shown in the table below.

/INH	Data	FR	SEG Output Voltage	
H	H	H	V5	Selected
		L	VDDH	
	L	H	V1	Deselected
		L	V4	
L	—	H	V1	Deselected
		L	V4	

■ **TIMING CHART**

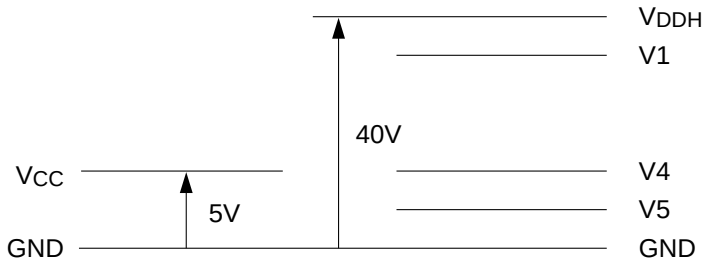


■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V1, V4, V5	–0.3 to V_{DDH} +0.3	V
Input voltage	V_I	–0.3 to V_{CC} +0.3	V
Output voltage	V_O	–0.3 to V_{CC} +0.3	V
DIO output current	I_{O1}	20	mA
LCD circuit output current	I_{O2}	20	mA
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–65 to +150	°C

Note 1. Let the V_{DDH}, V1, V4 and V5 voltages maintain the condition, $V_{DDH} \geq V1 \geq V4 \geq V5 \geq GND$, all the time.



Note 2. If the logic circuit power supply comes to float while voltage is applied to the power supply of the liquid crystal driving circuit, the LSI may be broken permanently. So, prevent the logic circuit power supply from floating. Pay special attention to the power supply sequence when the system is switched on or off.

● **DC Electrical Characteristics**

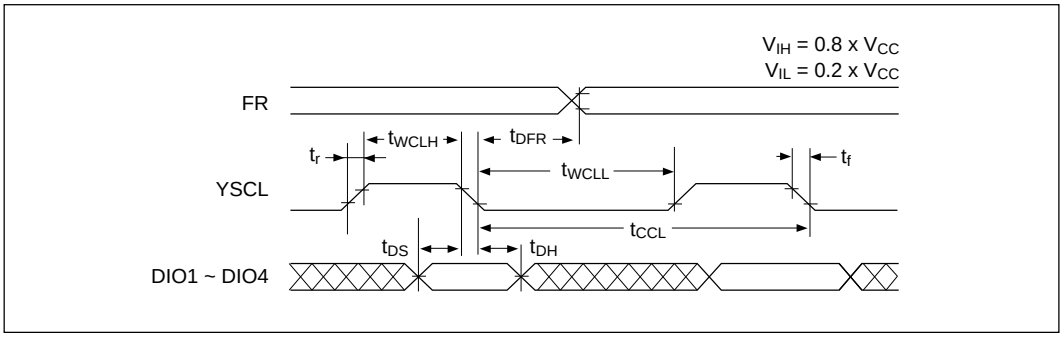
(Unless otherwise specified, GND = 0 V, V_{CC} = +5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Applicable Terminal	Min	Typ	Max	Unit
Supply voltage (1)	V_{CC}		V_{CC}	4.5	5.0	5.5	V
Recommended supply voltage	V_{DDH}		V_{DDH}	14.0	—	40.0	V
Operable voltage	V_{DDH}	Function	V_{DDH}	8.0	—	—	V
Supply voltage (2)	V1	Recommendation value	V1	8/9V_{DDH}	—	V_{DDH}	V
Supply voltage (3)	V4, V5	Recommendation value	V4, V5	GND	—	1/9V_{DDH}	V
High level input voltage	V_{IH}		DIO1 to DIO4	0.8V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}		FR, YSCL, $\overline{INH}$, SHL	GND	—	0.2V_{CC}	V
High level output voltage	V_{OH}	I_{OH} = –0.3 mA	DIO1 to DIO4	V_{CC} –0.4	—	V_{CC}	V
Low level output voltage	V_{OL}	I_{OL} = 0.3 mA		GND	—	0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	FR, YSCL, $\overline{INH}$, SHL	—	—	2.0	µA
Input–output leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}	DIO1 to DIO4	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = 14.0 to 40.0 V V_{IH} = V_{CC}, V_{IL} = GND	GND	—	—	25	µA
Output resistance	R_{COM}	ΔV_{ON} = 0.5V, V_{DDH}=+30.0V	*1 O0 to O99	—	0.7	1.8	kΩ
		ΔV_{ON} = 0.5V, V_{DDH}=+20.0V		—	0.8	2.2	
		ΔV_{ON} = 0.5V, V_{DDH}=+14.0V		—	1.0	2.6	
Current consumed (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC}, V_{IL} = GND, f_{YSCL} =33.6 kHz, f_{FR} =70 Hz; Input data: 1/480, "H" is input every duty. Common has no load.	V_{CC}	—	30	60	µA
Current consumed (2)	I_{DDH}	V_{CC} = +5.0 V, V4 = +4.0 V, V1 = +26.0 V, V_{DDH} =+30.0V, Other conditions are same as those of I_{DD}	V_{DDH}	—	45	120	µA
Input terminal capacity	C_I	Freq.=1 MHz, T_a = 25°C Solid chip	FR, YSCL, $\overline{INH}$, SHL	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		DIO1 to EIO4	—	—	15	pF

*1 The output resistance is specified within the ranges of the supply voltages (2) and (3).

● **AC Electrical Characteristics**

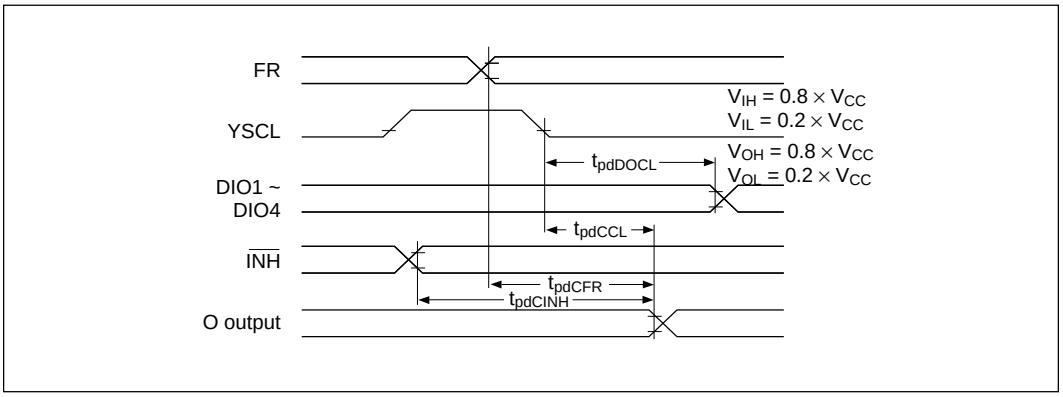
○ **Input Timing Characteristics**



(V_{CC} = 5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input signal rise time	t_r		—	—	50	ns
Input signal rise time	t_f		—	—	50	ns
YSCL cycle time	t_{CCL}		400	—	—	ns
YSCL high level pulse width	t_{WCLH}		70	—	—	ns
YSCL low level pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		40	—	—	ns
FR delay allowable time	t_{DFR}		–300	—	300	ns

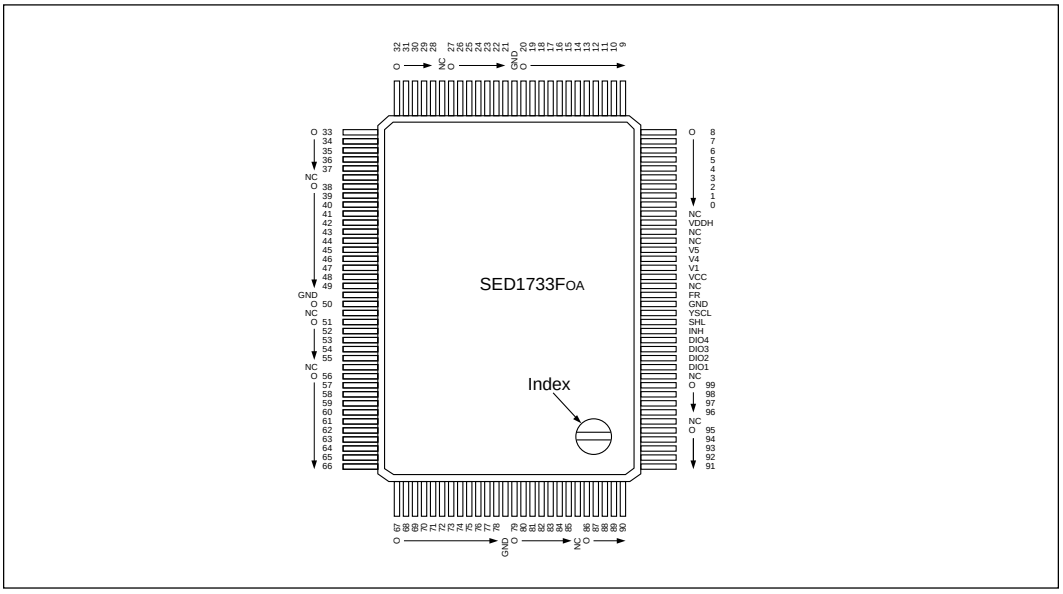
○ **Output Timing Characteristics**



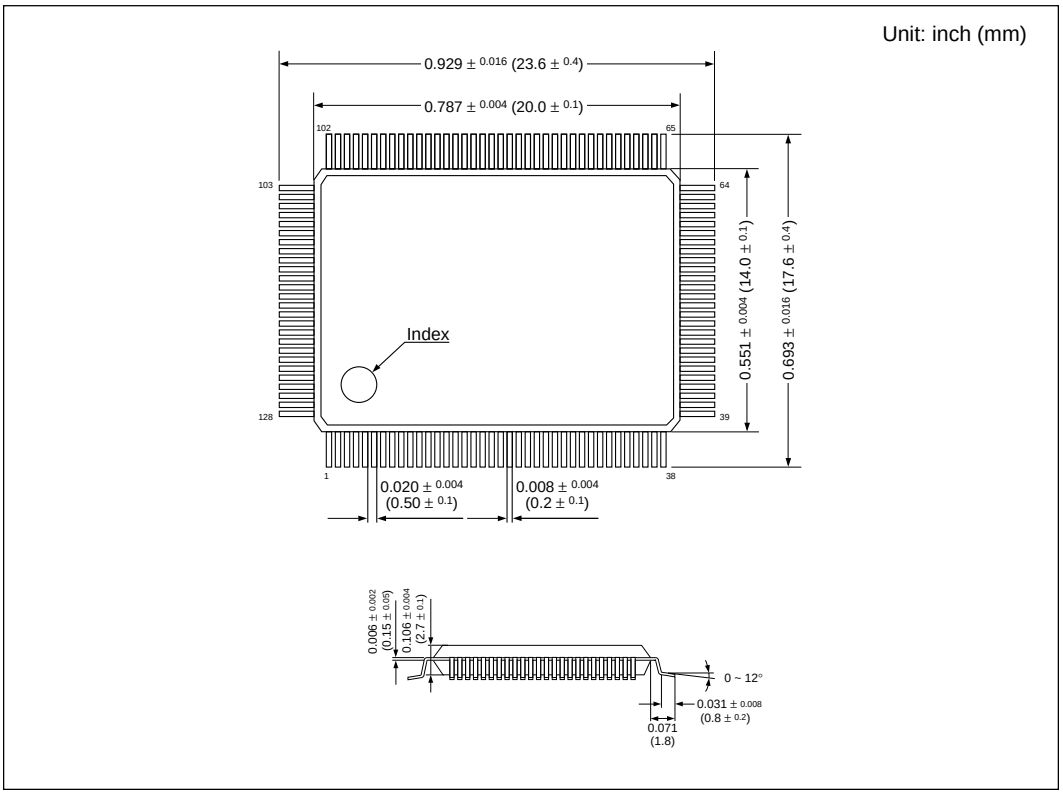
(V_{CC} = +5.0 V ±10%, V_{DDH} = +40.0 V, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL fall to DIO delay time	t_{pdDOCL}	C_L = 15 pF	—	—	300	ns
YSCL fall to O delay time	t_{pdCCL}		—	—	0.7	µs
$\overline{INH}$ to O output delay time	t_{pdCINH}	C_L = 100 pF	—	—	0.7	µs
FR to O output delay time	t_{pdCFR}		—	—	0.7	µs

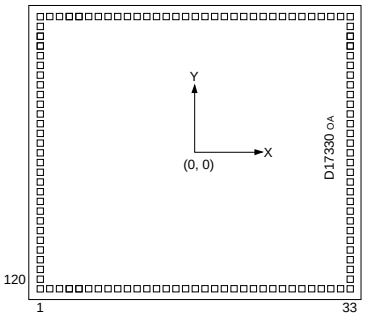
■ PACKAGE DIMENSIONS (SED1733F$_{0A}$)



■ PLASTIC QFP5-128PIN-S1



■ PAD LAYOUT



Chip Dimensions	6.10 mm × 5.30 mm
Pad pitch	0.170 mm (Min.)
Chip thickness	0.400 ±0.025 mm
Aluminum pad opening	100 μm × 100 μm (all terminals)

■ PAD COORDINATES

Pad Number	Pad Name	X (μm)	Y (μm)
1	O 92	–2882	–2482
2	O 93	–2620	–2482
3	O 94	–2420	–2482
4	O 95	–2230	–2482
5	O 96	–2050	–2482
6	O 97	–1870	–2482
7	O 98	–1700	–2482
8	O 99	–1530	–2482
9	NC	–1360	–2482
10	DIO1	–1190	–2482
11	DIO2	–1020	–2482
12	DIO3	–850	–2482
13	DIO4	–680	–2482
14	$\overline{INH}$	–510	–2482
15	SHL	–340	–2482
16	YSCL	–170	–2482
17	GND	0	–2482
18	FR	170	–2482
19	V_{CC}	340	–2482
20	V1	510	–2482
21	V4	680	–2482
22	V5	850	–2482
23	NC	1020	–2482
24	V_{DDH}	1190	–2482
25	NC	1360	–2482
26	O 0	1530	–2482
27	O 1	1700	–2482
28	O 2	1870	–2482
29	O 3	2050	–2482
30	O 4	2230	–2482
31	O 5	2420	–2482
32	O 6	2620	–2482
33	O 7	2882	–2482
34	O 8	2882	–2482
35	O 9	2882	–2060
36	O 10	2882	–1880
37	O 11	2882	–1700
38	O 12	2882	–1530
39	O 13	2882	–1360
40	O 14	2882	–1190
41	O 15	2882	–1020
42	O 16	2882	–850
43	O 17	2882	–680
44	O 18	2882	–510
45	O 19	2882	–340
46	O 20	2882	–170
47	GND	2882	0
48	O 21	2882	170
49	O 22	2882	340
50	O 23	2882	510
51	O 24	2882	680
52	O 25	2882	850
53	O 26	2882	1020
54	O 27	2882	1190
55	O 28	2882	1360
56	O 29	2882	1530
57	O 30	2882	1700
58	O 31	2882	1880
59	O 32	2882	2060
60	O 33	2882	2250
61	O 34	2882	2482
62	O 35	2620	2482
63	O 36	2420	2482
64	O 37	2230	2482
65	O 38	2050	2482
66	O 39	1870	2482
67	O 40	1700	2482
68	O 41	1530	2482
69	O 42	1360	2482
70	O 43	1190	2482
71	O 44	1020	2482
72	O 45	850	2482
73	O 46	680	2482
74	O 47	510	2482
75	O 48	340	2482
76	O 49	170	2482
77	GND	0	2482
78	O 50	–170	2482
79	O 51	–340	2482
80	O 52	–510	2482
81	O 53	–680	2482
82	O 54	–850	2482
83	O 55	–1020	2482
84	O 56	–1190	2482
85	O 57	–1360	2482
86	O 58	–1530	2482
87	O 59	–1700	2482
88	O 60	–1870	2482
89	O 61	–2050	2482
90	O 62	–2230	2482
91	O 63	–2420	2482
92	O 64	–2620	2482
93	O 65	–2882	2482
94	O 66	–2882	2250
95	O 67	–2882	2060
96	O 68	–2882	1880
97	O 69	–2882	1700
98	O 70	–2882	1530
99	O 71	–2882	1360
100	O 72	–2882	1190
101	O 73	–2882	1020
102	O 74	–2882	850
103	O 75	–2882	680
104	O 76	–2882	510
105	O 77	–2882	340
106	O 78	–2882	170
107	GND	–2882	0
108	O 79	–2882	–170
109	O 80	–2882	–340
110	O 81	–2882	–510
111	O 82	–2882	–680
112	O 83	–2882	–850
113	O 84	–2882	–1020
114	O 85	–2882	–1190
115	O 86	–2882	–1360
116	O 87	–2882	–1530
117	O 88	–2882	–1700
118	O 89	–2882	–1880
119	O 90	–2882	–2060
120	O 91	–2882	–2250

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