

SED1610

CMOS 86 ROWS LCD DRIVER

■ DESCRIPTION

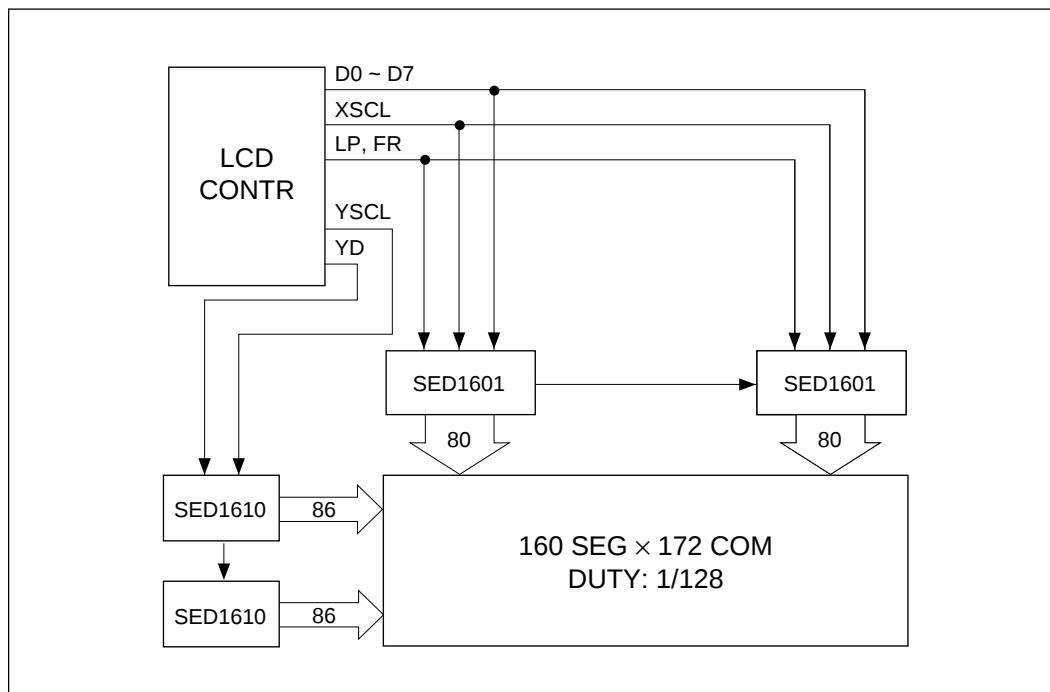
The SED1610 is an 86 output dot matrix LCD common (row) driver for driving a high-capacity LCD panel at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of LCD driving voltages. Due to the architecture of the SED1610, the LCD driving voltage V_0 is isolated from V_{DD} . This provides the ability to adjust the offset bias independently of V_{DD} . These unique features allow the SED1610 to interface with a variety of LCD panels.

The SED1610 is used in conjunction with the SED1600 (80 segment driver) or the SED1601 (80 segment driver) to drive a large-capacity dot matrix LCD panel.

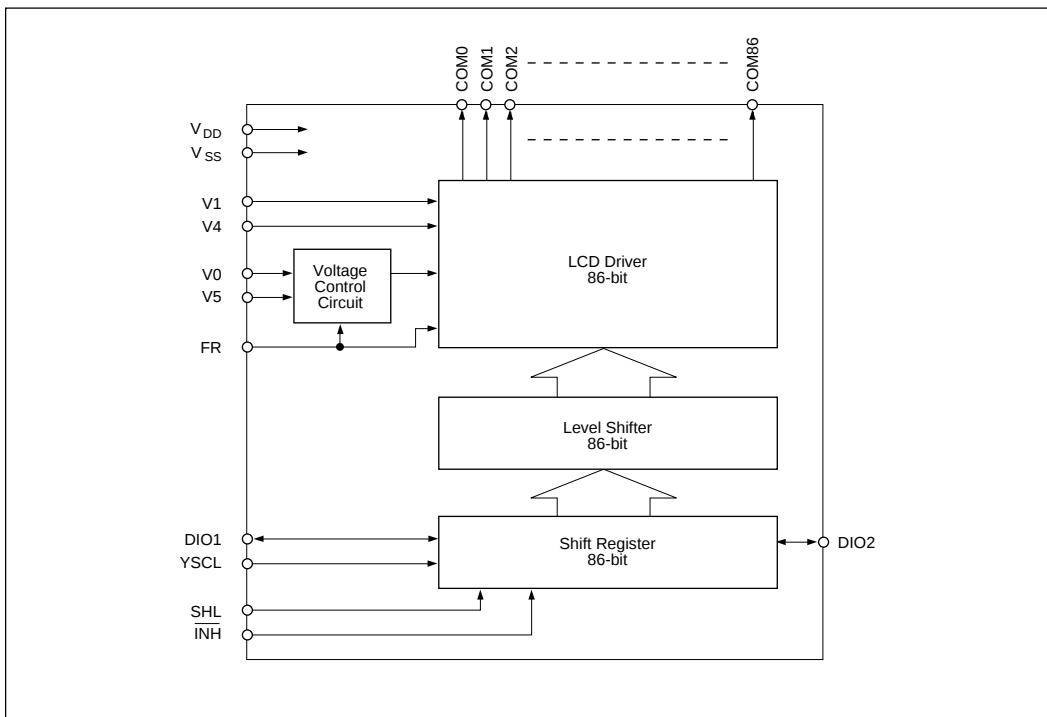
■ FEATURES

- Low-power CMOS technology
- 86-bit common (row) driver
- Duty cycle 1/64 to 1/300
- Display blanking available
- Shift clock frequency 2MHz max.
- Ability to adjust offset bias of the LCD source from V_{DD}
- Selectable output shift direction
- Wide range of LCD voltage -12 to -28V
- Supply voltage 5.0V $\pm$ 10%
- Package QFP5-100 pins (FAA)

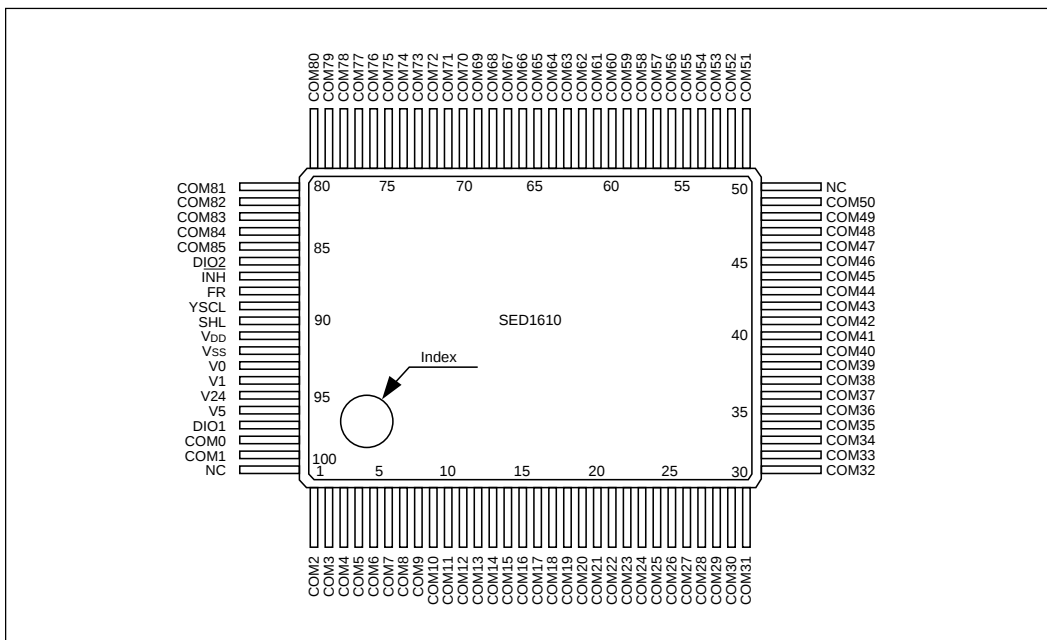
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



■ PIN DESCRIPTION

Pin name	Functions
COM0 to COM 85	LCD driving common (row) outputs. Each output changes at the falling edge of YSCL.
$\overline{\text{INH}}$	Controls all common outputs to nonselect level (V4 when FR = L, V1 when FR = H) (low active)
YSCL	Shift clock of serial data (falling edge trigger).
DIO1, DIO2	Serial transfer data I/O, which is controlled by SHL input. Output changes at falling edge of YSCL.
SHL	Shift direction selection and DIO pin control.
	SHL COM output shift direction
	1 2
	L 85 ← 0 Input Output R 85 → 0 Output Input
FR	AC signal of LCD driving outputs.
V _{DD} , V _{SS}	Logic circuit power. V _{DD} : 0 V (GND) V _{SS} : -5.0 V
V0, V1, V4, V5	LCD driving power. V5: -12 to -28 V V _{DD} ≥ V0 > V1 > V4 > V5

INH	Contents of Shift Register	FR	COM0 ~ 85	
H	H	H	V5	(Select level)
		L	V0	
	L	H	V1	(Non select level)
		L	V4	
L	Fixed to "L"	H	V1	(Non select level)
		L	V4	

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V _{SS}	-7.0 to +0.3	V
Supply voltage (2)	V5	-30.0 to +0.3	V
Supply voltage (2)	V0, V1, V4	V5 -0.3 to +0.3	V
Input voltage (1)	V _i	V _{SS} -0.3 to +0.3	V
Output voltage (1)	V _o	V _{SS} -0.3 to +0.3	V
Output current (1)	I _o	20	mA
Output current (2)	I _{OSEG}	20	mA
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-65 to +150	°C
Soldering temperature, time	T _{sol}	260°C, 10 s (at lead)	—
Allowable power dissipation	P _D	300	mW

● DC Electrical Characteristics

(Unless otherwise specified, $V_{DD} = V_0 = 0\text{ V}$, $V_{SS} = -5.0\text{ V} \pm 10\%$, $T_a = -20\text{ to }75^\circ\text{C}$)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Operating voltage (1)	V_{SS}		V_{SS}	-5.5	-5.0	-4.5	V
Recommended operating voltage	V_5		V_5	-28.0	—	-12.0	V
Minimum operating voltage						-8.0	
Operating voltage (2)	V_0		V_0	-2.5	—	0	V
"H" input voltage	V_{IH}		DI01, DI02, YSCL, FR, SHL, INH	0.2 V_{SS}	—	—	V
"L" input voltage	V_{IL}			—	—	0.8 V_{SS}	V
"H" output voltage	V_{OH}	$I_{OH} = -0.6\text{ mA}$	DI01, DI02	-0.4	—	—	V
"L" output voltage	V_{OL}	$I_{OL} = 0.6\text{ mA}$		—	—	$V_{SS} + 0.4$	V
Input leakage current	I_{LI}	$V_{SS} \leq V_i \leq 0\text{ V}$	YSCL, SHL, INH, FR	—	—	2.0	μA
	$I_{LI/O}$	$V_{SS} \leq V_i \leq 0\text{ V}$	DI01, DI02	—	—	5.0	μA
Stand-by current	I_{DDS}	$V_5 = -12.0\text{ to }-28.0\text{ V}$ $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	V_{DD}	—	—	25	μA
Output resistance	R_{SEG}	$ \Delta V_{ON} = 0.5\text{ V}$	V_5	-20.0V	—	1.1	$k\Omega$
				-14.0V	—	1.2	
				-8.0V	—	2.0	
Current dissipation (1)	I_{SSO1}	$V_{SS} = -5.0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, $f_{YSCL} = 7.7\text{ kHz}$, Frame period = 60 Hz; Input data: "H" every $1/128$ duty No-load	V_{SS}	—	7	15.0	μA
Current dissipation (2)	I_{SSO2}	$V_{SS} = -5.0\text{ V}$, $V_1 = -2.0\text{ V}$ $V_4 = -18.0\text{ V}$, $V_5 = -20.0\text{ V}$ All other conditions are same as I_{SSO1}	V_5	—	7	15.0	μA
Input capacitance	C_i	$T_a = 25^\circ\text{C}$	YSCL, SHL, INH, FR	—	—	8.0	pF
	$C_{I/O}$		DI01, DI02	—	—	15.0	pF

● AC Characteristics

○ Input Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL period	t_{CCL}		500	—	—	ns
YSCL "H" pulse width	t_{WCLH}		70	—	—	ns
YSCL "L" pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		10	—	—	ns
Allowable FR delay time	t_{DFR}		-500	—	500	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns

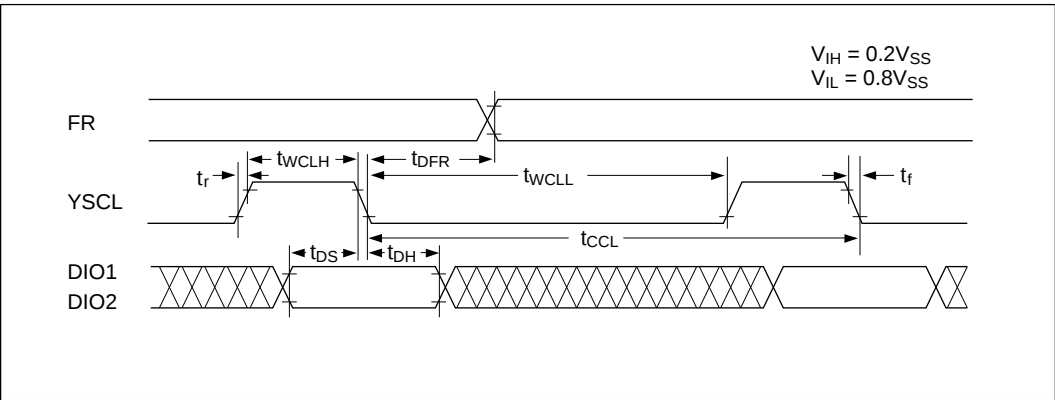
○ Output Timing

(V_{SS} = -5.0 V ±10%, T_a = -20 to 75°C)

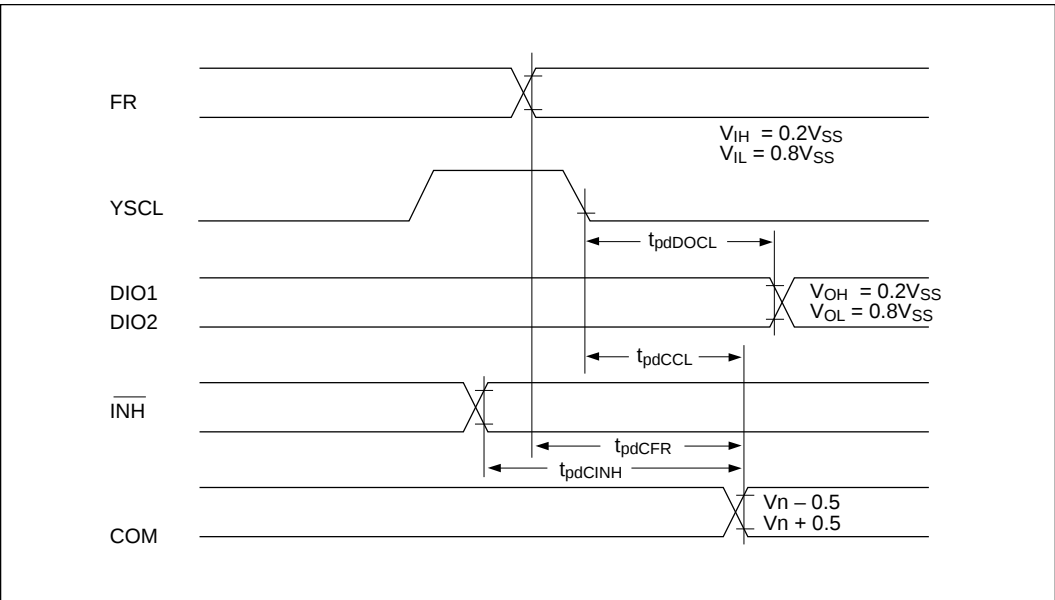
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(YSCL-fall to DIO) Delay time	t _{pdDOCL}	C _L = 15 pF	30	—	300	ns
(YSCL-fall to COM output) Delay time	t _{pdCCL}	V ₅ = -12.0 to -28.0 V C _L = 100 pF	—	—	3.0	μs
($\overline{\text{INH}}$ to COM output) Delay time	t _{pdCINH}					
(FR to COM output) Delay time	t _{pdCFR}					

● Timing Chart

○ Input Timing

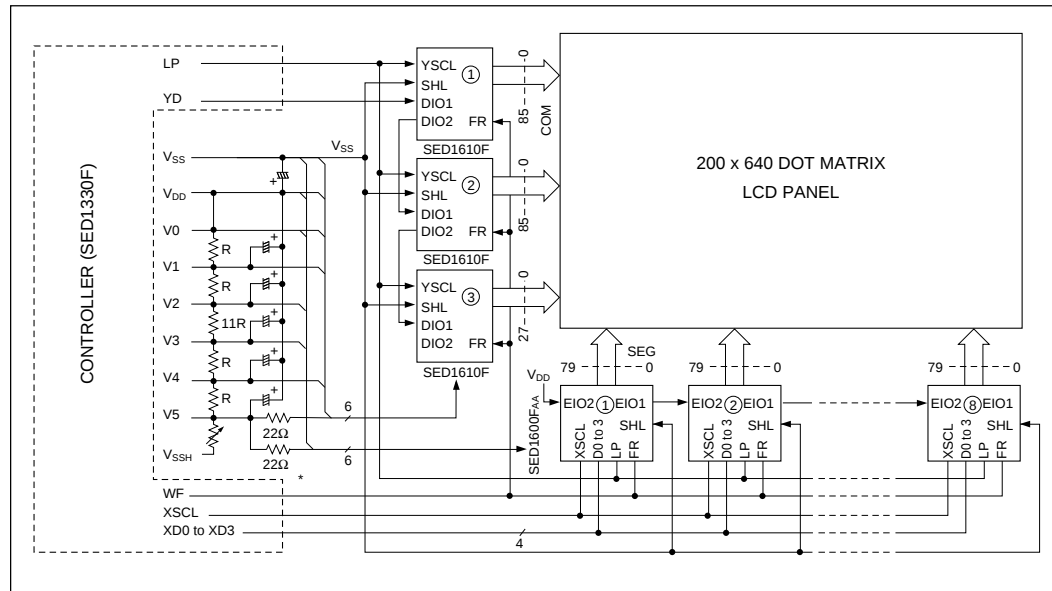


○ Output Timing



■ EXAMPLE OF APPLICATION (SED1610FAA)

(for 200 × 640 DOT MATRIX LCD)



Note: * Be sure to connect a current limiter resistor. Also, connect decoupling capacitors (0.01 μF) near pins Vss and V5 of each LSI for noise protection.