SED1770/71

CMOS LCD DRIVER

■ DESCRIPTION

The SED1770 and the SED1771 are 160-bit output LCD segment (column) analog drivers for driving high-capacity active matrix LCD MIM- or TFT-type panels. These devices take 3-bit analog input (VA, VB, VC) which are (R, G, B) signals, and can support duty cycle higher than 1/100 (up to 1/500). Also, the LSI features a wide range of LCD voltages from 5 to 17V.

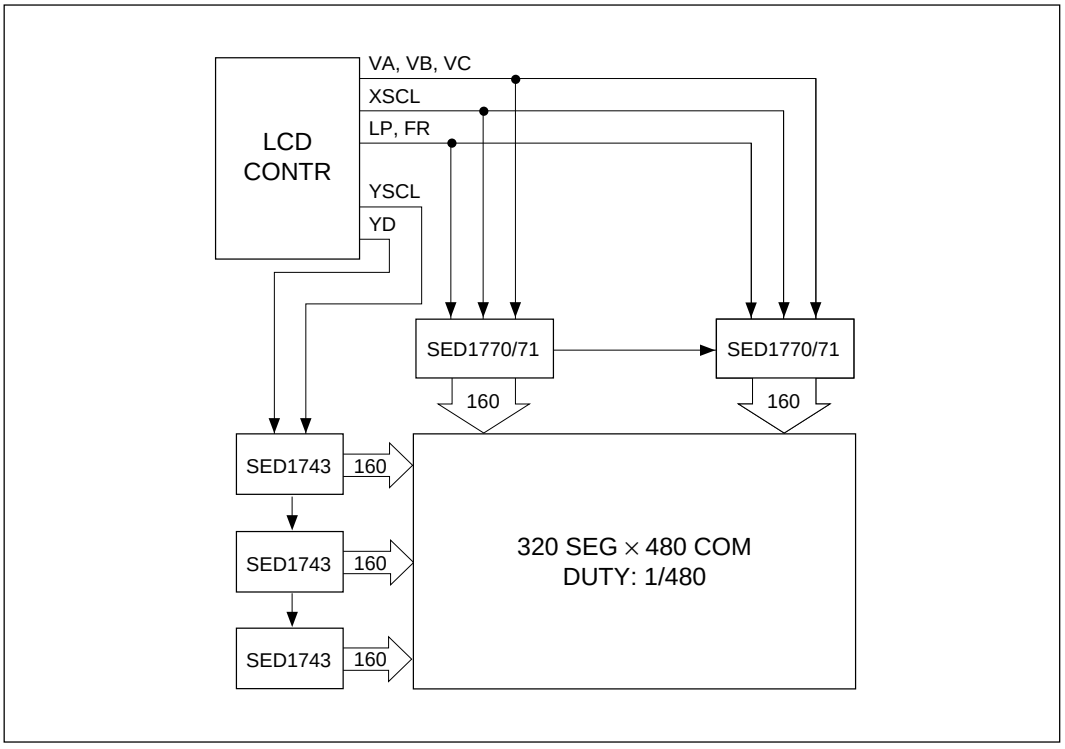
The device uses a high-speed daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1770/71 is used in conjunction with the SED1743F common drivers to support a large-capacity TFT/MIM active matrix LCD panel.

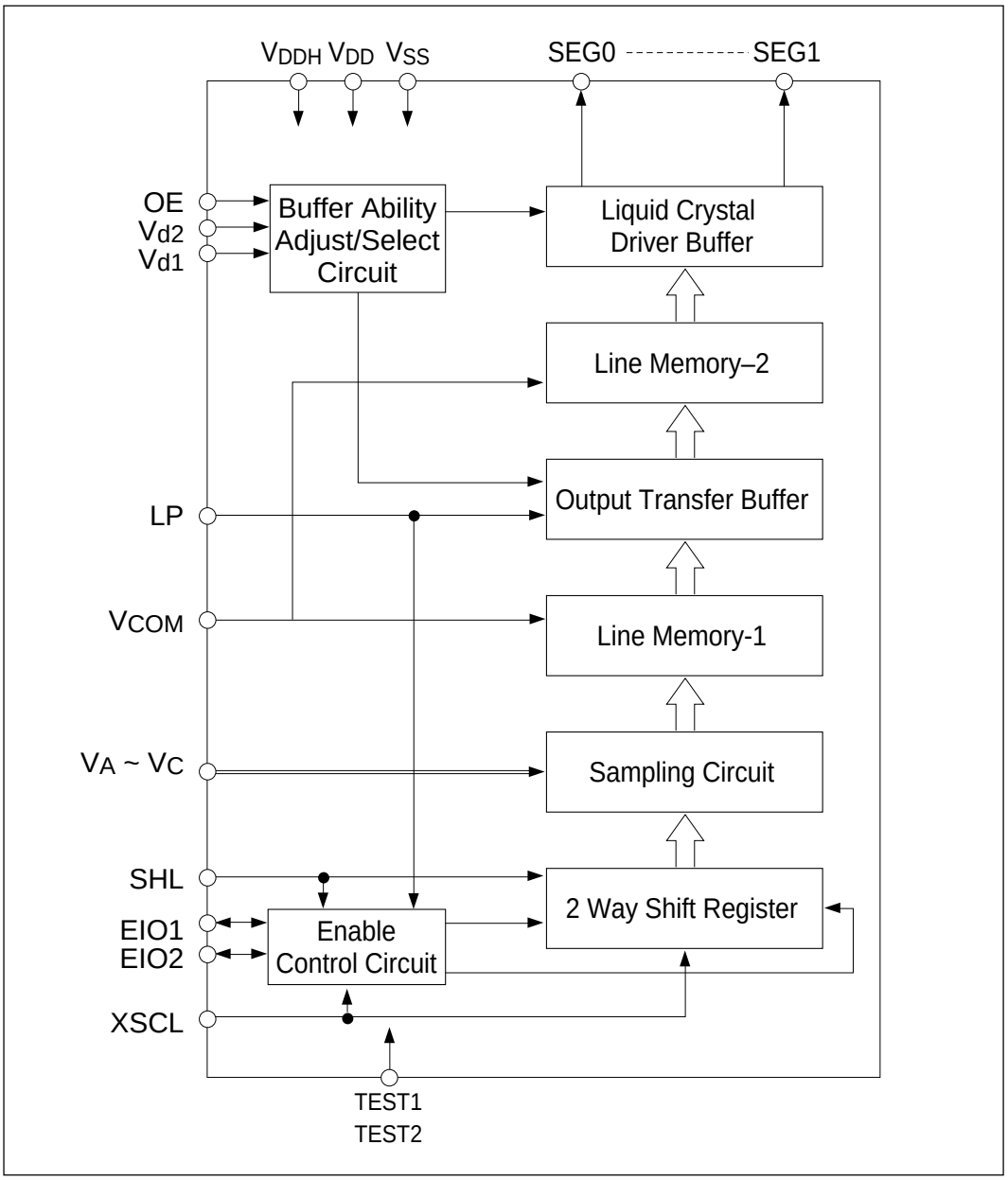
■ FEATURES

- Low-power, high-speed CMOS technology
- LCD driver output 160 (SED1770)
  162 (SED1771)
- High-speed data transfer 10MHz
- Support high-speed daisy-chain data transfer which reduces power consumption
- Takes 3-bit video inputs (VA, VB, VC)
- Built-in high-speed sampling circuitry
- Selectable output shift direction
- Low output resistance
- Wide range of LCD voltage .... 5 to 17V
- Supply voltage ..... 4.5 to 5.5V
- Package ..... TAB (2-sided)
  Al pad (D_{OA})

■ SYSTEM BLOCK DIAGRAM



■ **BLOCK DIAGRAM**



■ FUNCTIONS OF BLOCKS

- **Enable control circuit**

  If the enable signal is in the disable status, the internal clock signal is fixed to "L" and placed in the POWER SAVE mode.

  When using multiple segment drivers, the EIO terminals of the drivers should be cascade-connected while the EIO terminal of the front driver is connected to V_{SS}. In this case, the sampling of the front driver starts from XSCL's initial rising. As the enable control circuit automatically detects that sampling of data of the portion of 160 outputs has been finished thus automatically transferring the enable signal, the control signal by the control LSI is not necessary.

  The EIO output is reset by LP input.

- **Shift register**

  The shift register shifts the sampling signal by shift clock input. And it selects the shift direction by SHL input.

- **Sampling circuit**

  The sampling circuit samples analog input signals sequentially by means of the sampling signals from the shift register. At this time, input/output are corresponded as follows: V_A with SEG0, 3, 6 --- 159; V_B with SEG1, 4, 7 ---157; and V_C with SEG2, 5, 8 --- 158.

- **Line memory - 1**

  The line memory-1 stores the analog data sampled by the sampling circuit.

- **Output transfer buffer**

  With the rising of LP, the output transfer buffer transfers the data of line memory-1 to line memory-2 and at the same time switches over to another liquid crystal drive output. When LP = H, make sure that XSCL = L. While sampling the data, make sure that LP = L. The ability of this buffer can be adjusted by V_{d1}.

- **Line memory - 2**

  The line memory-2 holds the voltage of the liquid crystal drive output for the period until the next switching.

- **Liquid crystal drive buffer**

  The crystal drive buffer outputs the liquid crystal drive voltage. The ability of this buffer can be adjusted by V_{d2} and switched over by OE.

- **Buffer ability adjustment and switching circuit**

  This circuit performs two types of buffer ability adjustment and switching. The buffer abilities of both V_{d1} and V_{d2} reach their lowest level when they are equivalent to V_{DDH}; the respective abilities can be increased by lowering the electric potential, thus enabling them to cope with various liquid crystal panels.

  The ability (output current) of the liquid crystal drive buffer is switched over by the OE to be used. With the time of writing data in the panel set at OE = "H", the large current is used to drive the buffer; after writing the data, the small current is used to drive the buffer at OE = "L". This not only improves the data write ability but also prevents the leakage of the hold time, thus making it possible to save power.

■ PIN DESCRIPTION

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Power</th><th>Number of Terminals</th></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Shift register data input/output;
Connected to the lower-stage EIO in cascade connection;
Changes at XSCL's rising edge</td><td>V_{DD}
~
V_{SS}</td><td>2</td></tr>
<tr><td>XSCL</td><td>I</td><td>Clock signal input;
Shift register operation at rising and falling edges</td><td>↑</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch signal input; switches the output data at rising edge.</td><td>↑</td><td>1</td></tr>
<tr><td>OE</td><td>I</td><td>Liquid crystal drive buffer ability switching signal input:
H: Large current drive
L: Small current drive</td><td>↑</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select signal input of shift register
<table>
<tr><th>SHL</th><th>EIO1</th><th>EIO2</th><th>SEG Output</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td><td>01-> 1 -> 2 --- -> 158 -> 159</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td><td>159 -> 158 -> --- -> 2 -> 1 -> 0</td></tr>
</table></td><td>↑</td><td>1</td></tr>
<tr><td>TEST1
TEST2</td><td>I</td><td>Test input: Normally L.
Pulldown is not built in.</td><td>↑</td><td>2</td></tr>
<tr><td>V_{d1}
V_{d2}</td><td>I</td><td>Buffer ability adjustment input:
The buffer ability for output transfer and that for liquid crystal drive can be varied by the voltage applied to the terminal.
V_{d1}: Output transfer buffer ability adjustment
V_{d2}: Liquid crystal drive buffer ability adjustment</td><td>V_{DDH}
~
V_{SS}</td><td>2</td></tr>
<tr><td>V_A
V_B
V_C</td><td>I</td><td>Analog signal input:
Inputs image signals (R, G, and B).</td><td>↑</td><td>3</td></tr>
<tr><td>SEG0
~
SEG159*</td><td>O</td><td>Liquid crystal drive segment output:
Outputs the level, based on the analog signal input (V_A, V_B and V_C) data as a sample holder.
The input/output are corresponded as
V_A ->SEG0, 3, 6···, V_B -> SEG1, 4, 7···, V_C -> SEG2, 5, 8 ···.</td><td>↑</td><td>160</td></tr>
<tr><td>V_{COM}</td><td>I</td><td>Sample hold reference voltage input;
Reference power of the sample hold circuit;
To input the central electric potential of the analog signal input (V_A, V_B, V_C) is the standard.</td><td>↑</td><td>1</td></tr>
<tr><td>V_{DDH}</td><td>P</td><td>Power supply for high voltage LCD drive circuit.</td><td>—</td><td>2</td></tr>
<tr><td>V_{DD}</td><td>P</td><td>Power supply for logic circuit.</td><td>—</td><td>1</td></tr>
<tr><td>V_{SS}</td><td>P</td><td>LSI's common GND:
Shall be externally connected among V_{SS} terminals.</td><td>—</td><td>3</td></tr>
</table>

(*) In the case of SED1771DOA, this is up to 162 outputs and SEG 162, and the number of terminals increases by two.

Total: 183
(NC 3)

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +25.0	V
Input voltage *1	V_{ID}	–0.3 to V_{DD}+0.3	V
Input voltage *2	V_{IA}	–0.3 to V_{DDH}+0.3	V
Storage temperature	T_{stg}	–65 to +150	°C
Operating temperature	T_{opr}	–20 to +75	°C

Notes: 1. Applies to EIO1, EIO2, XSCL, LP, OE, SHL, TEST1, and TEST2.
2. Applies to V_A, V_B, V_C, V_{d1}, V_{d2}, and V_{COM}.

● DC Characteristics

(V_{SS}=0V, V_{DD}=5V±10%, V_{DDH}=15V, and T_a= –20 to +75°C unless otherwise noted)

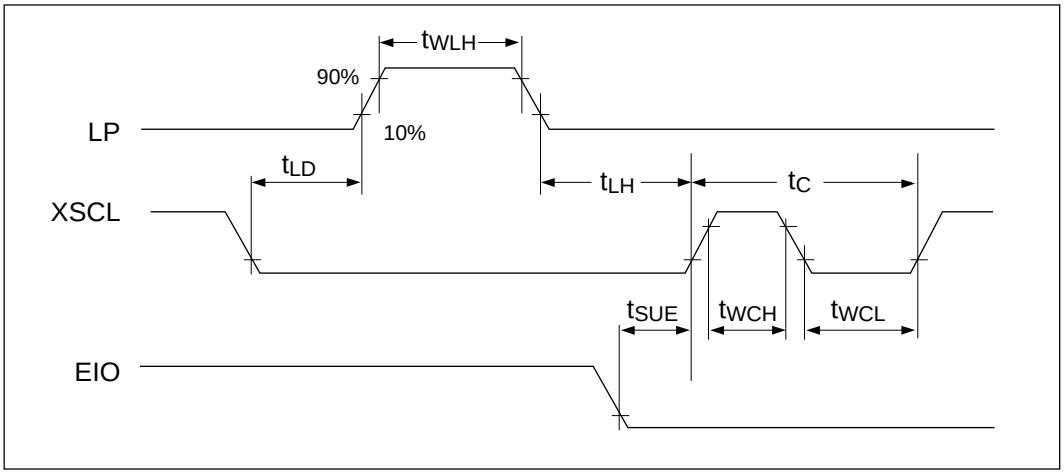
Parameter	Symbol	Condition	Applicable Signal	Rating			Unit
				Min	Typ	Max	
Supply voltage (1)	V_{DD}		V_{DD}	4.5	—	5.5	V
Supply voltage (2)	V_{DDH}		V_{DDH}	V_{DD}	—	17.0	V
“H” input voltage	V_{IH}		*1	0.8•V_{DD}	—	V_{DD}	V
“L” input voltage	V_{IL}			V_{SS}	—	0.2•V_{DD}	V
Input terminal capacity	CID	T_a = 25°	*2	—	—	8.0	pF
Input leak current	ILID	0 < VI < V_{DD}		—	—	2.0	µA
“H” output voltage	V_{OH}	I_{OH} = –0.4mA	EIO1 EIO2	V_{DD}–0.4	—	V_{DD}	V
“L” output voltage	V_{OL}	I_{OL} = 0.4mA		V_{SS}	—	0.4	V
Input/output terminal capacity	CI/O	T_a = 25°C		—	—	15.0	pF
Input/output leak current	ILI/O	0 < VI < V_{DD}		—	—	15.0	µA
Analog input voltage	V_{video}		V_A, V_B, V_C	V_{SS}+1.5	—	V_{DDH}–1.5	V
Analog input capacity	CIA			—	—	80	pF
Between-output voltage deviation	dVO		SEG 0 ~ SEG 161	MAX – MIN = 100			mV
Input/output gain	G_V			95	—	105	%
“1” output current	I_{OH}	*3		—	0.1	—	mA
“0” output current	I_{OL}	*4		—	0.1	—	mA
Current consumption (1)	I_{DD}	*5	—	—	—	5	mA
Current consumption (2)	I_{DDH}	*5	—	—	—	15	mA

Notes: 1. EIO1, EIO2, XSCL, LP, OE, SHL, TEST1, TEST2
2. XSCL, LP, OE, SHL, TEST1, TEST2
3. Vd2 = 12V, V_{video} = 13V, OE = H
4. Vd2 = 12V, V_{video}=2V, OE=H
5. f_{XSCL} = 10MHz, 1H = 63.5µs, V_{video}=+2~+13V, TOE (OE=H) = 10µs, without load

- **AC Characteristics**

  V_{SS} = 0V, V_{DD} = 5V±10%, V_{DDH} = 15V, and T_a = –20 to +75°C unless otherwise noted.

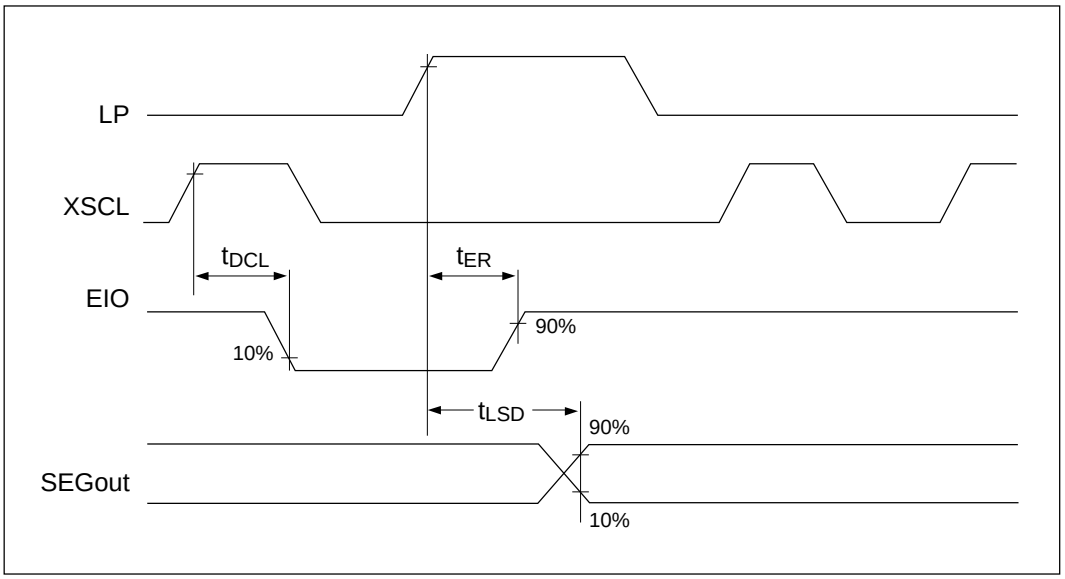
○ Input Timing Characteristics



Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
XSCL cycle	t_C		100	—	—	ns
XSCL “H” pulse width	t_{WCH}		40	—	—	ns
XSCL “L” pulse width	t_{WCL}		40	—	—	ns
XSCL-to-LP rise time	t_{LD}		40	—	—	ns
LP pulse width	t_{WLH}	*1	2.5	—	—	µs
LP-to-XSCL time	t_{LH}		1	—	—	µs
EIO setup time	t_{SUE}		50	—	—	ns

Notes: 1. Time of XSCL=L and LP=H.

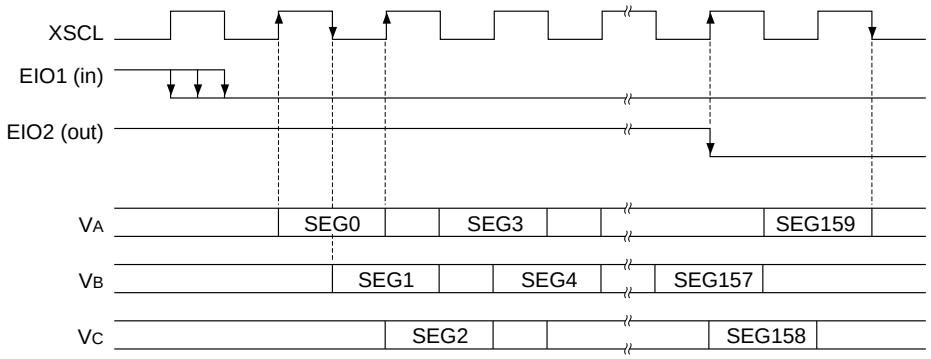
o Output Timing Characteristics



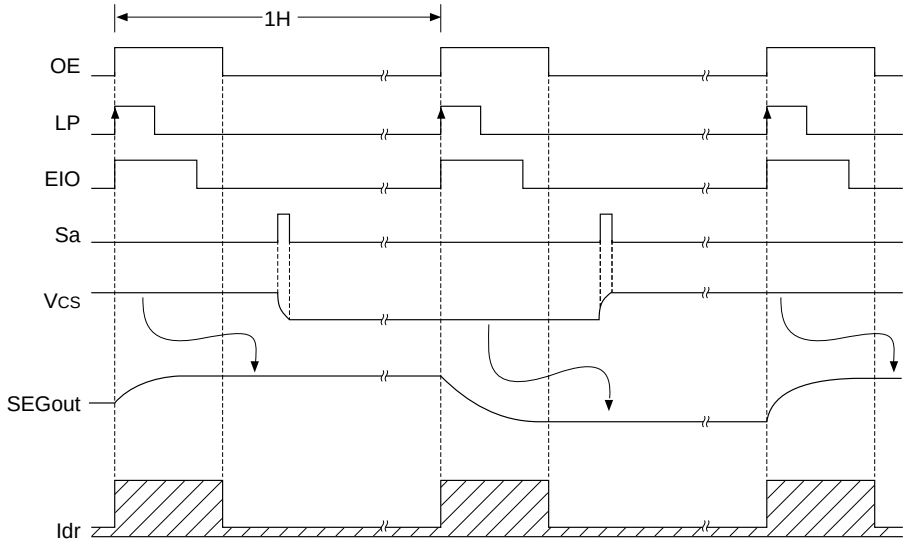
Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
EIO output delay time	t_{DCL}	CL = 15pF	—	—	40	ns
EIO output reset time	t_{ER}		—	—	12.0	ns
LP-to-SEGout delay time	t_{LSD}		Variable by V_{dl} and V_{d2}			
		*1	—	—	15	µs

Notes: 1. $V_{d1} = V_{d2} = 12V$, $V_{video} = 2\sim13V$, load capacity = 100pF, OE = “H”.

- **Signal Timing Example (with specifications of SHL = H, 160 outputs, 1:1 correspondence)**



Sampling is started from the rising edge of the next XSCL after EIO1 has fallen.



Sa : Analog switch input of the sampling circuit
VCS : Electric potential of the sampling capacitor
Idr : Size of the drive current

■ ALUMINUM MASTER SLICE OPTIONS

On this LSI, the following switchings are available by the aluminum master slice options.

- **Switching of number of output pins**

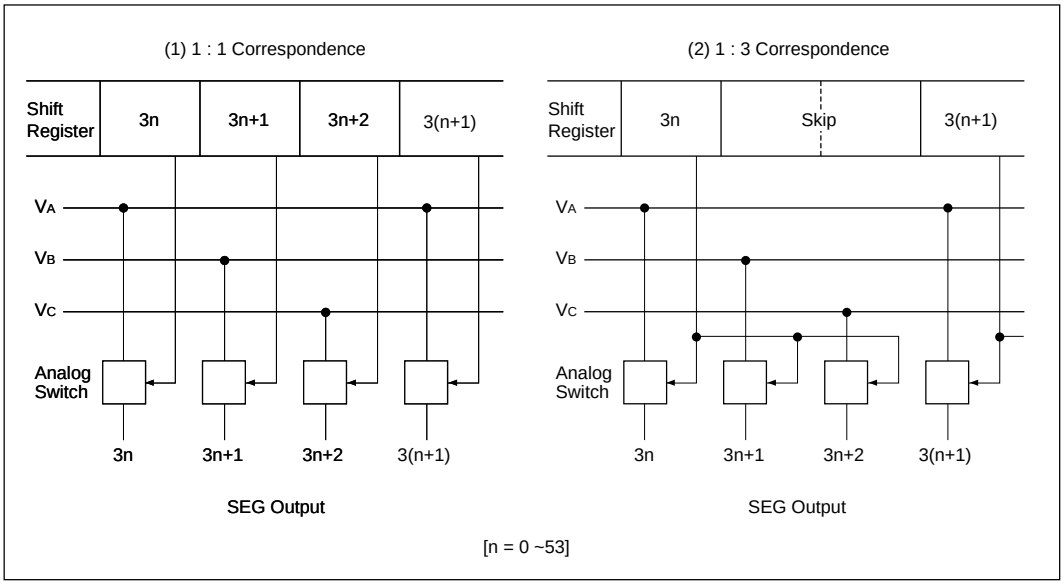
  (1) 160 outputs : Outputs EIO at the time of SEG158 sampling.
  At this time, the SEG160 and 161 terminals are placed in the NC status.

  (2) 162 outputs : Outputs EIO at the time of SEG160 sampling.

  Note: This applies if SHL = H. If SHL = L, the first output becomes SEG159 with (1), and SEG161 with (2).

- **Correspondence between the shift register and the sampling analog switch**

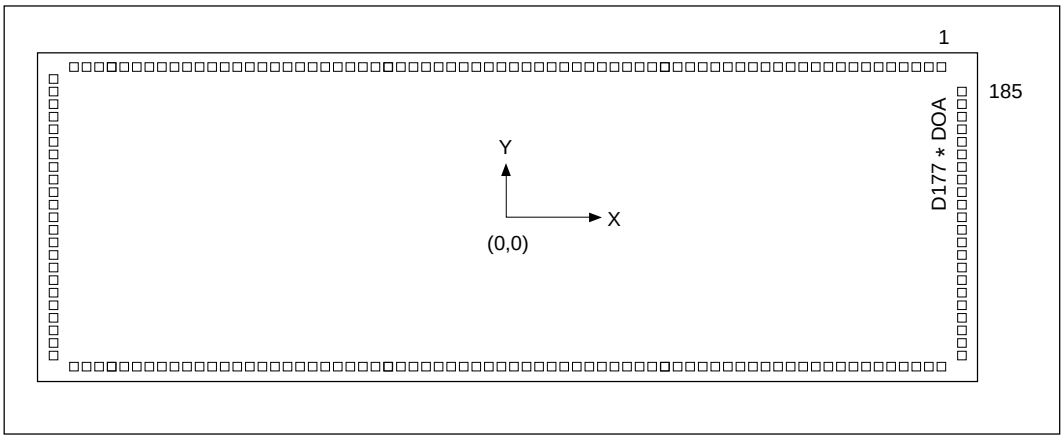
  (1) Shift registers and analog switches shall be corresponded at the ratio of 1:1.
  (2) One shift register stage shall be connected with three analog switches; and the shift register shall operate for every 3 stages.



- **Correspondence with product names**

  SED1770DOA: Selects 160 outputs for 1) and 1:1 correspondence for 1)
  SED1771DOA: Selects 162 outputs for 1) and 1:3 correspondence for 2)

■ PAD LAYOUT



	X	Y
Die size:	11.27mm × 3.79mm	
Pad pitch:	0.12mm (min)	

* Metallic bump specifications

Die thickness: 0.25mm ± 0.025mm

Bump Size	X Y	PAD No.
Bump size A	350µm × 150µm ± 20µm	23, 24, 28, 29, 30, 31
Bump size B	200µm × 150µm ± 20µm	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 32, 33, 34, 35, 36, 37
Bump size C	95µm × 150µm ± 20µm	Other than above

(The X in X and Y of the bump size shall be the direction parallel to the scribe line.)

■ PAD COORDINATES

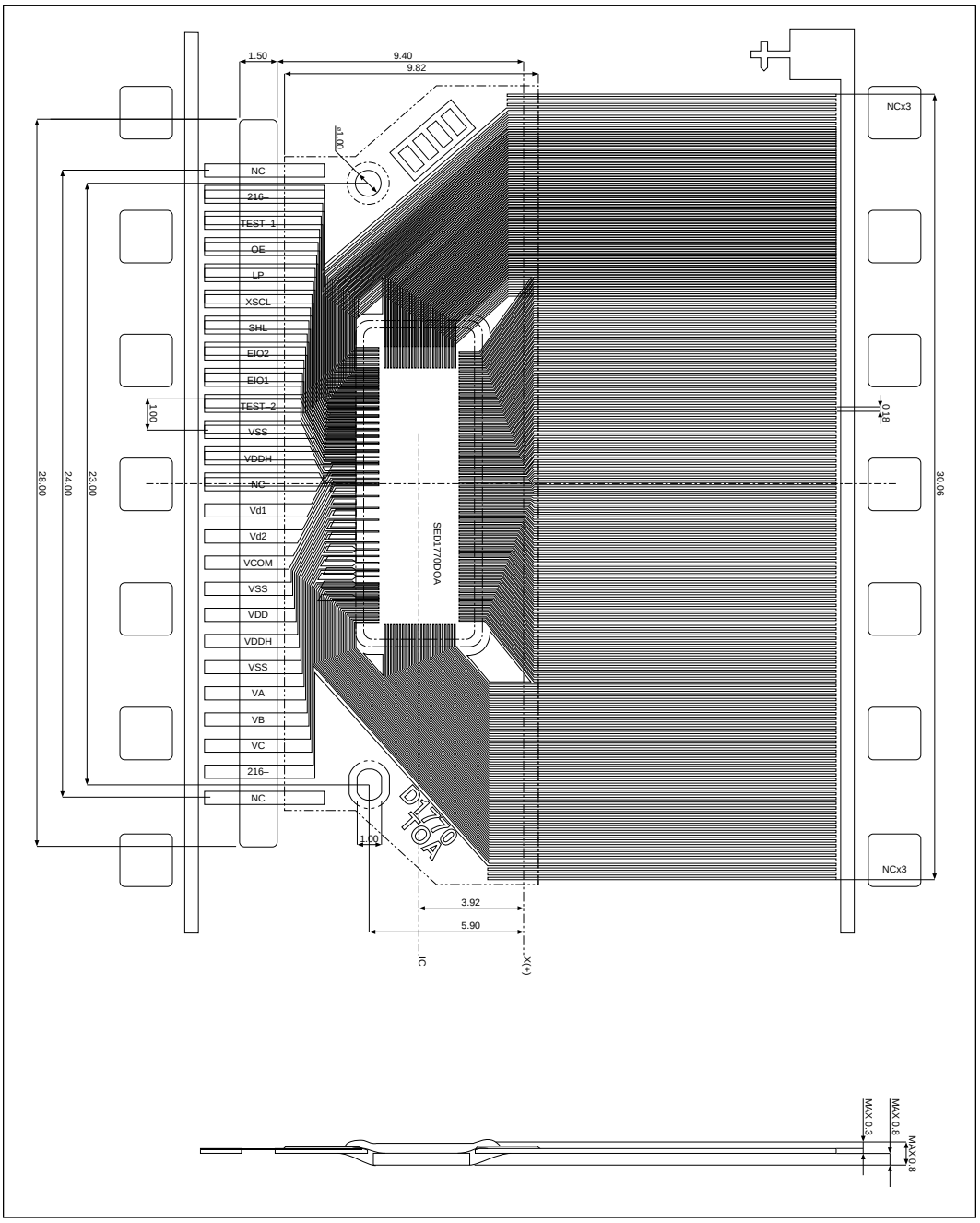
Unit = μm

Pad		X	Y	Pad		X	Y	Pad		X	Y
Number	Name			Number	Name			Number	Name		
1	SEG148	5210	1699	45	SEG7	–4490	1699	89	SEG51	–3540	–1699
2	SEG149	5090	1699	46	SEG8	–4610	1699	90	SEG52	–3420	–1699
3	SEG150	4970	1699	47	SEG9	–4730	1699	91	SEG53	–3300	–1699
4	SEG151	4850	1699	48	SEG10	–4850	1699	92	SEG54	–3180	–1699
5	SEG152	4730	1699	49	SEG11	–4970	1699	93	SEG55	–3060	–1699
6	SEG153	4610	1699	50	SEG12	–5090	1699	94	SEG56	–2940	–1699
7	SEG154	4490	1699	51	SEG13	–5210	1699	95	SEG57	–2820	–1699
8	SEG155	4370	1699	52	SEG14	–5436	1343	96	SEG58	–2700	–1699
9	SEG156	4250	1699	53	SEG15	–5436	1223	97	SEG59	–2580	–1699
10	SEG157	4130	1699	54	SEG16	–5436	1103	98	SEG60	–2460	–1699
11	SEG158	4010	1699	55	SEG17	–5436	983	99	SEG61	–2340	–1699
12	SEG159	3890	1699	56	SEG18	–5436	863	100	SEG62	–2220	–1699
13	SEG160*	3770	1699	57	SEG19	–5436	743	101	SEG63	–2100	–1699
14	SEG161*	3650	1699	58	SEG20	–5436	623	102	SEG64	–1980	–1699
15	TEST1	3400	1699	59	SEG21	–5436	503	103	SEG65	–1860	–1699
16	OE	3150	1699	60	SEG22	–5436	383	104	SEG66	–1740	–1699
17	LP	2900	1699	61	SEG23	–5436	263	105	SEG67	–1620	–1699
18	XSCL	2650	1699	62	SEG24	–5436	143	106	SEG68	–1500	–1699
19	SHL	2400	1699	63	SEG25	–5436	23	107	SEG69	–1380	–1699
20	EIO2	2150	1699	64	SEG26	–5436	–97	108	SEG70	–1260	–1699
21	EIO1	1900	1699	65	SEG27	–5436	–217	109	SEG71	–1140	–1699
22	TEST2	1650	1699	66	SEG28	–5436	–337	110	SEG72	–1020	–1699
23	V_{SS}	1270	1699	67	SEG29	–5436	–457	111	SEG73	–900	–1699
24	V_{DDH}	830	1699	68	SEG30	–5436	–577	112	SEG74	–780	–1699
25	V_{d1}	440	1699	69	SEG31	–5436	–697	113	SEG75	–660	–1699
26	V_{d2}	190	1699	70	SEG32	–5436	–817	114	SEG76	–540	–1699
27	VCOM	–60	1699	71	SEG33	–5436	–937	115	SEG77	–420	–1699
28	V_{SS}	–450	1699	72	SEG34	–5436	–1057	116	SEG78	–300	–1699
29	V_{DD}	–890	1699	73	SEG35	–5436	–1177	117	SEG79	–180	–1699
30	V_{DDH}	–1330	1699	74	SEG36	–5436	–1297	118	SEG80	–60	–1699
31	V_{SS}	–1770	1699	75	SEG37	–5436	–1417	119	SEG81	60	–1699
32	V_A	–2150	1699	76	SEG38	–5100	–1699	120	SEG82	180	–1699
33	(NC)	–2400	1699	77	SEG39	–4980	–1699	121	SEG83	300	–1699
34	V_B	–2650	1699	78	SEG40	–4860	–1699	122	SEG84	420	–1699
35	(NC)	–2900	1699	79	SEG41	–4740	–1699	123	SEG85	540	–1699
36	V_C	–3150	1699	80	SEG42	–4620	–1699	124	SEG86	660	–1699
37	(NC)	–3400	1699	81	SEG43	–4500	–1699	125	SEG87	780	–1699
38	SEG0	–3650	1699	82	SEG44	–4380	–1699	126	SEG88	900	–1699
39	SEG1	–3770	1699	83	SEG45	–4260	–1699	127	SEG89	1020	–1699
40	SEG2	–3890	1699	84	SEG46	–4140	–1699	128	SEG90	1140	–1699
41	SEG3	–4010	1699	85	SEG47	–4020	–1699	129	SEG91	1260	–1699
42	SEG4	–4130	1699	86	SEG48	–3900	–1699	130	SEG92	1380	–1699
43	SEG5	–4250	1699	87	SEG49	–3780	–1699	131	SEG93	1500	–1699
44	SEG6	–4370	1699	88	SEG50	–3660	–1699	132	SEG94	1620	–1699

Pad		X	Y	Pad		X	Y	Pad		X	Y
Number	Name			Number	Name			Number	Name		
133	SEG95	1740	–1699	151	SEG113	3900	–1699	169	SEG131	5436	–577
134	SEG96	1860	–1699	152	SEG114	4020	–1699	170	SEG132	5436	–457
135	SEG97	1980	–1699	153	SEG115	4140	–1699	171	SEG133	5436	–337
136	SEG98	2100	–1699	154	SEG116	4260	–1699	172	SEG134	5436	–217
137	SEG99	2220	–1699	155	SEG117	4380	–1699	173	SEG135	5436	–97
138	SEG100	2340	–1699	156	SEG118	4500	–1699	174	SEG136	5436	23
139	SEG101	2460	–1699	157	SEG119	4620	–1699	175	SEG137	5436	143
140	SEG102	2580	–1699	158	SEG120	4740	–1699	176	SEG138	5436	263
141	SEG103	2700	–1699	159	SEG121	4860	–1699	177	SEG139	5436	383
142	SEG104	2820	–1699	160	SEG122	4980	–1699	178	SEG140	5436	503
143	SEG105	2940	–1699	161	SEG123	5100	–1699	179	SEG141	5436	623
144	SEG106	3060	–1699	162	SEG124	5436	–1417	180	SEG142	5436	743
145	SEG107	3180	–1699	163	SEG125	5436	–1297	181	SEG143	5436	863
146	SEG108	3300	–1699	164	SEG126	5436	–1177	182	SEG144	5436	983
147	SEG109	3420	–1699	165	SEG127	5436	–1057	183	SEG145	5436	1103
148	SEG110	3540	–1699	166	SEG128	5436	–937	184	SEG146	5436	1223
149	SEG111	3660	–1699	167	SEG129	5436	–817	185	SEG147	5436	1343
150	SEG112	3780	–1699	168	SEG130	5436	–697				

(*) SEG160 and 161 become NC in the case of SED1770D$_{OA}$

■ EXTERNAL PACKAGE DIMENSIONS



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