

SFH6318T SFH6319T

Low Current, High Gain Optocoupler

FEATURES

- Industry Standard SOIC-8 Surface Mountable Package
- High Current Transfer Ratio, 800%
- Low Input Current, 0.5 mA
- High Output Current, 60 mA
- Isolation Test Voltage, 3000 V_{RMS}
- TTL Compatible Output, V_{OL}=0.1 V
- Adjustable Bandwidth—Access to Base
- Underwriters Lab File #E52744
-  VDE 0884 Available with Option 1

APPLICATIONS

- Logic Ground Isolation—TTL/TTL, TTL/CMOS, CMOS/CMOS, CMOS/TTL
- EIA RS 232C Line Receiver
- Low Input Current Line Receiver—Long Lines, Party Lines
- Telephone Ring Detector
- 117 VAC Line Voltage Status Indication—Low Input Power Dissipation
- Low Power Systems—Ground Isolation

DESCRIPTION

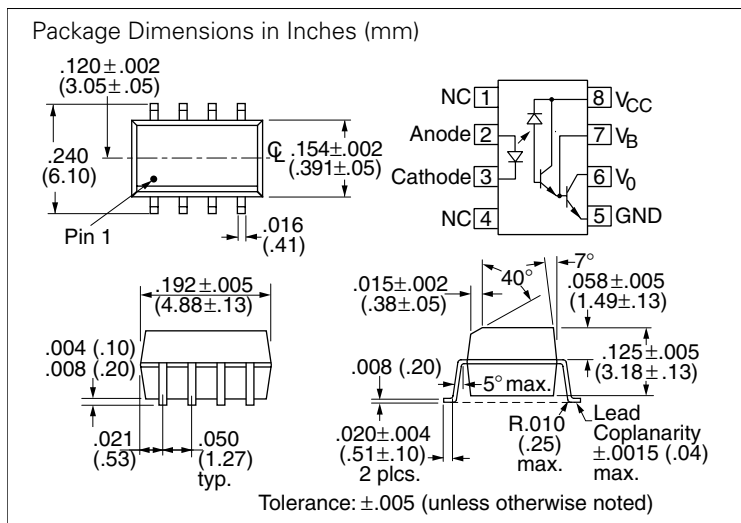
Very high current ratio together with 3000 V_{RMS} isolation are achieved by coupling an LED with an integrated high gain photodiode in a SOIC-8 package. Separate pins for the photodiode and output stage enable TTL compatible saturation voltages with high speed operation. Photodarlington operation is achieved by tying the V_{CC} and V_O terminals together. Access to the base terminal allows adjustment to the gain bandwidth.

The SFH6318T is ideal for TTL applications since the 300% minimum current transfer ratio with an LED current of 1.6 mA enables operation with one unit load-in and one unit load-out with a 2.2 k Ω pull-up resistor.

The SFH6319T is best suited for low power logic applications involving CMOS and low power TTL. A 400% current transfer ratio with only 0.5 mA of LED current is guaranteed from 0°C to 70°C.

Caution:

Due to the small geometries of this device, it should be handled with Electrostatic Discharge (ESD) precautions. Proper grounding would prevent damage further and/or degradation which may be induced by ESD.



Maximum Ratings (T_A=25°C)

Emitter

Reverse Input Voltage	3.0 V
Supply and Output Voltage, V _{CC} (pin 8-5), V _O (pin 6-5)	
SFH6318T	–0.5 to 7.0 V
SFH6319T	–0.5 to 18 V

Input Power Dissipation	35 mW
Derate Linearly above	50°C
Free Air Temperature	0.7 mW/°C
Average Input Current	20 mA
Peak Input Current	40 mA
(50% Duty Cycle-1.0 ms pulse width)	

Peak Transient Input Current	
(t _p ≤ 1.0 μs, 300 pps)	1.0 A

Detector (Si Photodiode + Photodarlington)

Output Current I _O (pin 6)	60 mA
Emitter-base Reverse Voltage (pin 5-7)	0.5 V
Output Power Dissipation	150 mW
Derate Linearly from 25°C	2.0 mW/°C

Package

Storage Temperature	–55°C to +125°C
Operating Temperature	–40°C to +85°C
Lead Soldering Temperature (t=10 s)	260°C
Junction Temperature	100°C
Ambient Temperature Range	–55°C to +100°C
Isolation Test Voltage between	

Emitter and Detector	3000 V _{RMS}
(refer to climate DIN 40046, part 2, Nov. 74)	

Pollution Degree (DIN VDE 0110)	2
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Creepage Distance	≥4.0 mm
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Clearance	≥4.0 mm
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Comparative Tracking Index	
per DIN IEC 112/VDE 0303, part 1	175

Isolation Resistance	
V _{IO} =500 V, T _A =25°C R _{ISOL}	≥10 ¹² Ω
V _{IO} =500 V, T _A =100°C R _{ISOL}	≥10 ¹¹ Ω

Electro-Optical Characteristics ($T_A=0^{\circ}\text{C}$ to 70°C , $T_A=25^{\circ}\text{C}$ —Typical, unless otherwise specified)

Parameter	Symbol	Device	Min	Typ	Max	Units	Test Conditions	Note
Current Transfer Ratio	CTR	SFH6318T	300	1600	2600	%	$I_F=1.6\text{ mA}$, $V_O=0.4\text{ V}$, $V_{CC}=4.5\text{ V}$	1,2
	—	SFH6319T	400 500	2000 1600	3500 2600		$I_F=0.5\text{ mA}$, $V_O=0.4\text{ V}$, $V_{CC}=4.5\text{ V}$ $I_F=1.6\text{ mA}$, $V_O=0.4\text{ V}$, $V_{CC}=4.5\text{ V}$	
Logic Low Output Voltage	V_{OL}	SFH6318T	—	0.1	0.4	V	$I_F=1.6\text{ mA}$, $I_O=4.8\text{ mA}$, $V_{CC}=4.5\text{ V}$	2
	—	SFH6319T		0.1 0.15 0.25	0.4 0.4 0.4		$I_F=1.6\text{ mA}$, $I_O=8.0\text{ mA}$, $V_{CC}=4.5\text{ V}$ $I_F=5.0\text{ mA}$, $I_O=15\text{ mA}$, $V_{CC}=4.5\text{ V}$ $I_F=12\text{ mA}$, $I_O=24\text{ mA}$, $V_{CC}=4.5\text{ V}$	
Logic High Output Current	I_{OH}	SFH6318T	—	0.1	250	μA	$I_F=0\text{ mA}$, $V_O=V_{CC}=7.0\text{ V}$	
		SFH6319T	—	0.05	100		$I_F=0\text{ mA}$, $V_O=V_{CC}=18\text{ V}$	
Logic Low Supply Current	I_{CCL}	—	—	0.2	1.5	mA	$I_F=1.6\text{ mA}$, $V_O=\text{OPEN}$, $V_{CC}=18\text{ V}$	
Logic High Supply Current	I_{CCH}	—	—	0.01	10	μA	$I_F=0\text{ mA}$, $V_O=\text{OPEN}$, $V_{CC}=18\text{ V}$	
Input Forward Voltage	V_F	—	—	1.4	1.7	V	$I_F=1.6\text{ mA}$, $T_A=25^{\circ}\text{C}$	—
Temperature Coefficient, Forward Voltage	$\Delta V_F/\Delta T_A$	—	—	−1.8	—	mV/ $^{\circ}\text{C}$	$I_F=1.6\text{ mA}$	
Input Capacitance	C_{IN}	—	—	25	—	pF	$f=1.0\text{ MHz}$, $V_F=0$	
Resistance (Input-Output)	R_{I-O}	—	—	10^{12} 10^{11}	—	Ω	$V_{IO}=500\text{ VDC}$, $T_A=25^{\circ}\text{C}$ $V_{IO}=500\text{ VDC}$, $T_A=100^{\circ}\text{C}$	3
Capacitance (Input-Output)	C_{I-O}	—	—	0.6	—	pF	$f=1.0\text{ MHz}$	3

Switching Specifications ($T_A=25^{\circ}\text{C}$)

Parameter	Symbol	Device	Min	Typ	Max	Units	Test Conditions	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	SFH6318T	—	2.0	10	μs	$I_F=1.6\text{ mA}$, $R_L=2.2\text{ k}\Omega$	
		SFH6319T	—	6.0 0.6	25 1.0		$I_F=0.5\text{ mA}$, $R_L=4.7\text{ k}\Omega$ $I_F=12\text{ mA}$, $R_L=270\text{ }\Omega$	2,4
Propagation Delay Time To Logic High at Output	t_{PLH}	SFH6318T	—	2.0	35		$I_F=1.6\text{ mA}$, $R_L=2.2\text{ k}\Omega$	—
		SFH6319T	—	4.0 1.5	60 7.0		$I_F=0.5\text{ mA}$, $R_L=4.7\text{ k}\Omega$ $I_F=12\text{ mA}$, $R_L=270\text{ }\Omega$	2,4
Common Mode Transient Immunity at Logic High Level Output	$ CM_H $	—	—	1 K	—	V/ μs	$I_F=0\text{ mA}$, $R_L=2.2\text{ k}\Omega$ $V_{CM}=10\text{ V}_{P-P}$	5,6
Common Mode Transient Immunity at Logic Low Level Output	$ CM_L $	—	—		—		$I_F=1.6\text{ mA}$, $R_L=2.2\text{ k}\Omega$ $V_{CM}=10\text{ V}_{P-P}$	

Notes

- DC current transfer ratio is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F times 100%.
- Pin 7 open.
- Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.
- Using a resistor between pin 5 and 7 will decrease gain and delay time.
- Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{CM} , to assure that the output will remain in a logic high state (i.e. $V_O>2.0\text{ V}$) common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e. $V_O<0.8\text{ V}$).
- In applications where dv/dt may exceed 50,000 V/ μs (such as state discharge) a series resistor, R_{CC} should be included to protect I_C from destructively high surge currents. The recommended value is

$$R_{CC} \cong \frac{IV}{0.15 I_F (\text{mA})} \text{ k}\Omega$$
Refer to Figure 2.

Figure 1. Switching test circuit

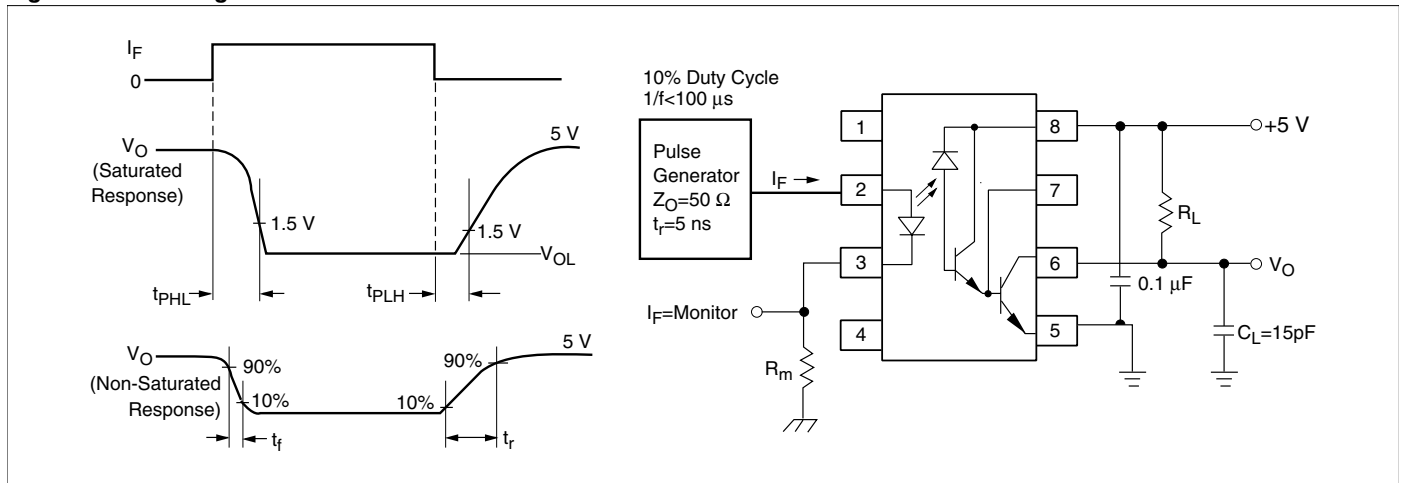


Figure 2. Test circuit for transient immunity and typical waveforms

