Network-Oriented SuperH™ RISC engine SH2-DSP with On-Chip 10/100 Mbps Ethernet™ Controller SH7615

Main Uses: Ethernet™ LAN connection system network controllers (network monitor cameras, FA/LBP/MFP LAN controllers, Internet phones, etc.)

- On-chip IEEE802.3 compliant Ethernet™ controller (MAC layer part)
- Complies with IEEE1149.1/JTAG
- 78 MIPS data processing capability when operating at maximum frequency of 60 MHz

High-speed Ethernet™ products can easily be supported by connection of a 10/100 Mbps compatible physical layer LSI. Enables boundary scan tests (JTAG tests), and improves the ease and reliability of board testing.

Data exchange via networks has come into general use for personal computers and their peripherals, and OA/FA equipment. Also, as Internet access has become easier, there has been a dramatic increase in the amount of multimedia information handled, including graphics, images, video, and speech, leading to a demand for networks capable of faster transfer. The Ethernet™*1 currently answers this need, and has become established as a standard interface for connection between network devices. Meanwhile, devices connected to the Internet require compression/decompression techniques for efficient transmission and reception of image and voice data, and there is a need for high-performance CPU/DSP functions for this purpose.

To meet this need, Hitachi developed the SH7615 RISC processor, with an SH2-DSP core and an on-chip Ethernet™ controller supporting 10/100 Mbps transfer speeds in LAN connection, as a network-oriented model in the SuperH™*2 RISC engine family. An overview of this processor is given here.

Features

The SH7615 achieves high performance of 78 MIPS/120 MOPS at a 3.3 V operating voltage and 60 MHz operating frequency.

■ Fast CPU/SH2-DSP

The SH7615 has an SH2-DSP with a 32-bit architecture as its CPU core, and has a 78 MIPS data processing capability at the maximum operating frequency of 60 MHz. DSP functions have also been enhanced, and the extended Harvard architecture DSP achieves a maximum processing performance of 120 MOPS.

■ Ethernet™ controller

The SH7615 has an on-chip media access controller (MAC) compliant with the IEEE802.3 standard, allowing direct connection to a physical layer LSI via the standard media independent interface (MII). Also provided on-chip is a direct memory access controller (E-DMAC) connected directly to the Ethernet™ controller.

A large part of buffer management is controlled by the E-DMAC itself using descriptors, enabling the load on the CPU to be reduced and efficient data

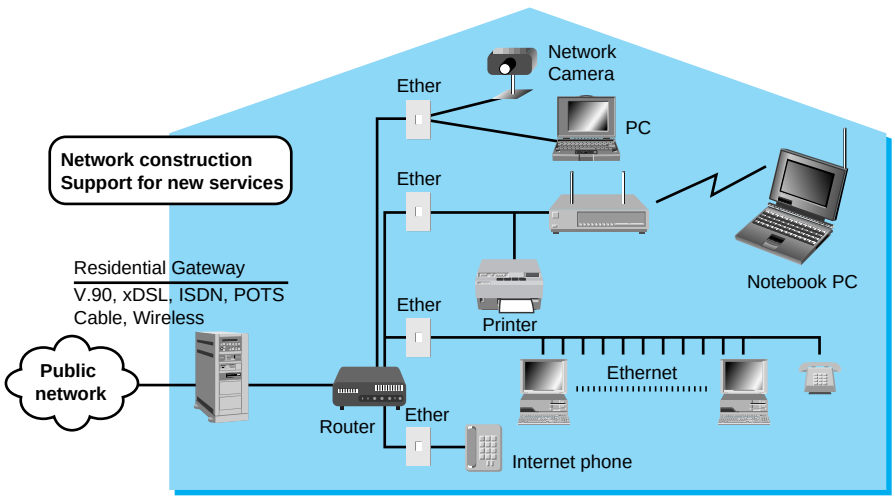

Fig. 1 SH7615 Target Applications

transfer control to be performed. In addition, high-speed LAN connection can be achieved easily by connecting a physical layer LSI supporting 10/100 Mbps. Other on-chip features include detection of Magic Packets™*3 supporting activation from the network (Wake on LAN), and various standby functions that help reduce power consumption when OA/FA equipment is in standby mode.

■ **IEEE1149.1/JTAG compliance**

Boundary scan tests (JTAG tests) can be carried out, simplifying board testing.

■ **On-chip memory**

• Cache: Maximum 4 kbytes

—Mixed instruction/data type cache, with instruction cache or data cache mode specifiable

—Can be used as 2-kbyte cache and 2-kbyte RAM.

• On-chip RAM

—X-RAM: 4 kbytes

—Y-RAM: 4 kbytes

■ **Peripheral modules**

• Interrupt controller

—16-level priority settings can be made.

—On-chip peripheral module interrupt vector address can be set.

• Four user break controller channels (A, B, C, D) on-chip

—Single-condition or sequential-condition interrupt generation for channels A, B, C, and D

—PC trace function

• Direct memory access controller (DMAC)

—4-Gbyte address space, maximum 16M transfers

—Transfer data length: Choice of 8 bits, 16 bits, 32 bits, or 16 bytes

• Comprehensive serial functions

—Two-channel serial communication interface with FIFO, supporting asynchronous and synchronous modes

—Three serial I/O channels, double-buffering transmit/receive ports in full-duplex operation

• Multifunction timers

—Three-channel timer pulse unit with a maximum 8 pulse input/output capability

—Single-channel 16-bit free-running timer (FRT)

—Single-channel watchdog timer

• System controller

—Selection of seven operating modes and three power-down modes

■ **Applications**

• Information/OA product field

Terminal devices with built-in network functions: network printers, network cameras, FA products, Internet phones

*1: Ethernet is a trademark of Xerox Corp.
*2: SuperH is a trademark of Hitachi, Ltd.
*3: Magic Packet is a trademark of Advanced Micro Devices, Inc.

Table 1 SH76xx Series Specifications

Model	SH7612	SH7615
CPU	SH2-DSP core	SH2-DSP core
Operating frequency	60 MHz	60 MHz
Power supply voltage	3.3 V	3.3 V
Cache size	4 kbytes	4 kbytes
RAM size	16 kbytes	8 kbytes
User break controller	2 channels	4 channels
Divider	√	—
Interrupt controller	√	√
DMAC	2 channels	2 channels
Ether controller DMAC	—	2 channels
Ether controller	—	√
Hitachi user debug interface	√	√
Serial communication interface with FIFO	2 channels	2 channels
Serial communication interface	√	√
Serial I/O	3 channels	3 channels
Timer pulse unit	3 channels	3 channels
Watchdog timer	1 channel	1 channel
Free-running timer	1 channel	1 channel
I/O ports	14 pins	30 pins
5 V interface	—	√
Package	176LQFP	208LQFP

√ : Available

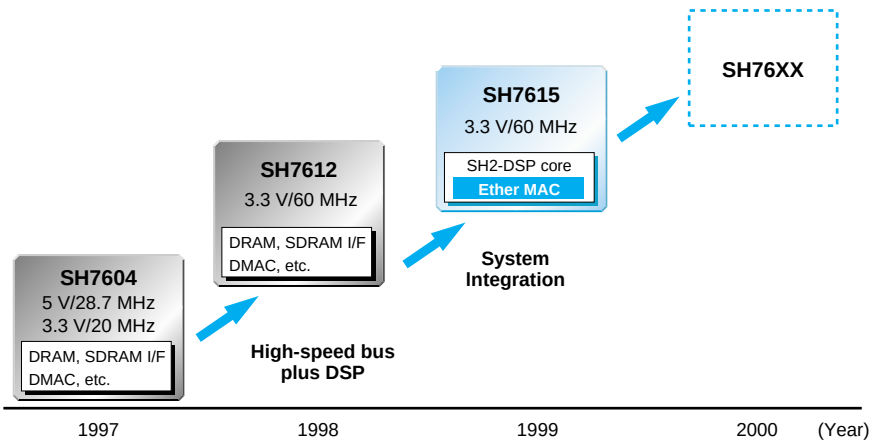

Fig. 2 SH76xx Series Product Evolution