TEXAS INSTRUMENTS

STORAGE
Products Group

SD5210
Integrated Processor/DSP
HDD Platform Device

Prototype

January 1999

FEATURES

- **ULTRA-2 DMA ATA interface**
  - **Compliant to ATA-1, ATA-2, ATA-3, and ATA/ATAPI-4 Standards[†]**
  - **Direct PC bus connection with on-board ATA drivers**
  - **Supports ultra DMA ATA (66 Mbyte/s)[†]**
  - **Supports PIO, single DMA, multiword DMA, and ultra DMA transfers[†]**
  - **Operates in master-only mode, slave-only mode, or both**
  - **IORDY flow control**
  - **Supports auto-read and auto-write**
  - **Supports queued commands[†]**

- **T320C2700B0 and external interface**
  - **Digital Signal Processor (DSP) interface**
  - **2 k words of internal SRAM**
  - **16 k words of internal ROM**
  - **150 MIPS**
  - **100 MHz emulation/trace speed**
  - **JTAG boundary scan compliant**

- **Buffer manager**
  - **Supports up to 16 Mbit EDO DRAM or 16 Mbit SDRAM**
  - **High performance worldwide up to 160 Mbit/s burst transfer rate**
  - **Flexible buffer segmentation**
  - **Separate host, disk, and processor address pointers**
  - **Supports code execution from buffer**

- **Disk formatter/sequencer**
  - **Writeable control store (WCS)-based sequencer included**
  - **Supports headerless operation**
  - **8-bit Non-Return-to-Zero (NRZ) interface supporting data rates up to 450 Mbit/s**
  - **Erasure flag for thermal asperity**
  - **1-byte or 2-byte fault-tolerant Synchronization**
  - **Rotational tolerance compensation**
  - **Supports read and write cache**
  - **Supports code execution from buffer**

- **Serial ports**
  - **Programmable for concurrent transfer**
  - **Interfaces with 3 serial devices**

- **Error-Correction Code (ECC) logic**
  - **30 bytes of ECC and 4 bytes of EDC**
  - **Five bytes of correction per interleave (t = 5)**
  - **Three way interleaved (I = 3)**
  - **Ten erasures corrected per interleave**
  - **Programmable seeding (LBA or physical block number)**
  - **On-the-fly correction; corrects unlimited consecutive sectors**
  - **Efficient defect scanning logic included**

- **Servo logic**
  - **Servo sync mark sequencer for flexible sync mark detection**
  - **WCS sequencer for timing signals**
  - **Servo field protection write lock logic**
  - **Sequencer control of gray code**
  - **Programmable:**
    - **Servo (sub) field lengths**
    - **Track ID field**
    - **Servo burst field length and numbers**
    - **0-crossing divider**
    - **Time domain filter**
    - **Commutation pulse time and length**
  - **Supports firmware and/or automatic commutation generation**
  - **Dedicated free-running timer with capture registers and interrupt**

- **Clock control**
  - **Clocks derived from external crystal-based oscillator or external oscillator**
  - **Two high performance PLL 6ZL zero pin clock generators**
  - **Internal power-down modes**

- **General-purpose timers**

- **Multiplexer (MUX) control for multiple modes**

- **Single reference firmware set**

- **176-pin Plastic Quad Flat Pack (PQFP)**

- **1850C07 technology (0.18 μ CMOS)**

- **Fully SCANed design for high coverage manufacturability**

- **RAM BIST for high megacell coverage**

[†] With appropriate firmware, software

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FUNCTIONAL BLOCK DIAGRAM