Dual Enhancement-Mode MOSFETS (N- and P-Channel)

CHARACTERISTICS

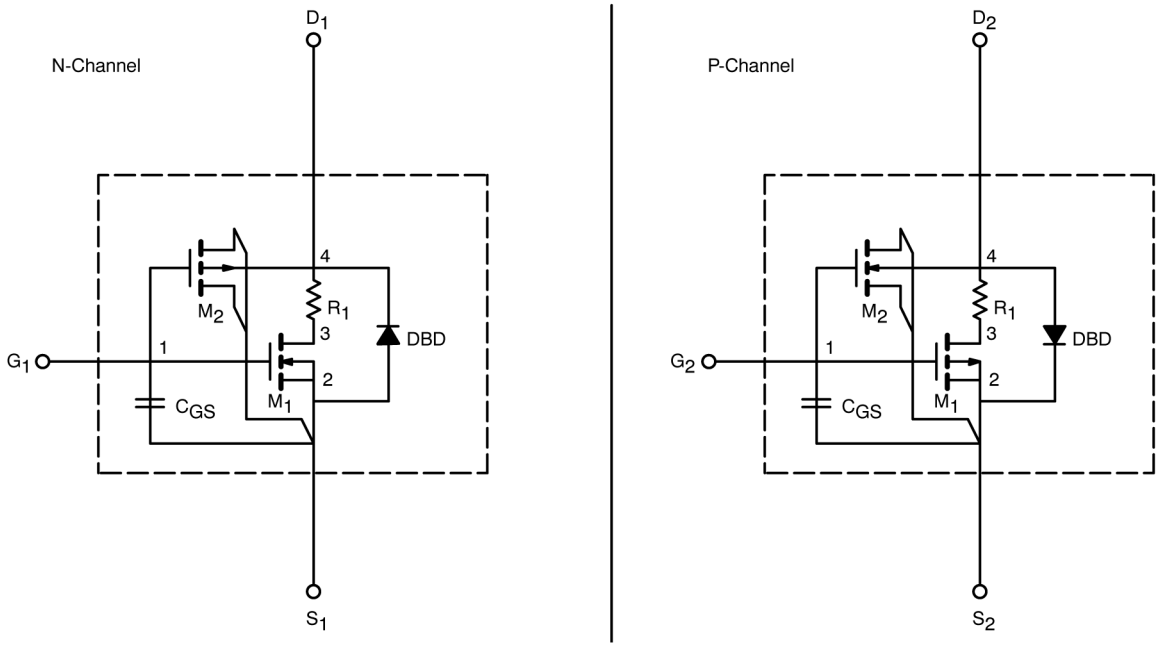
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Applicable over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The model subcircuit schematic is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



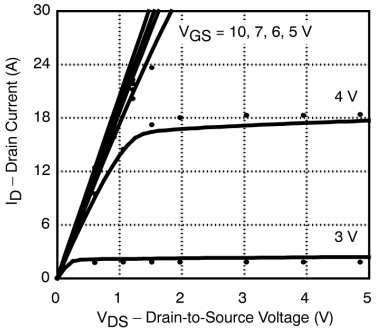
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

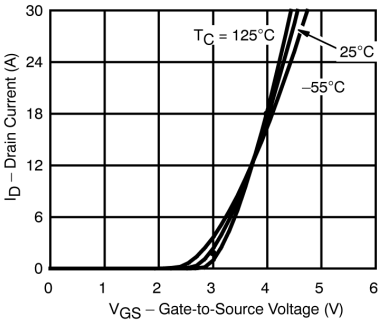
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Conditions**		**Typical**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V, V_{GS}, I_D = 250 µA	N-Ch	1.75	V
		V_{DS} = V, V_{GS}, I_D = –250 µA	P-Ch	2	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq 5$ V, V_{GS} = 10 V	N-Ch	100	A
		$V_{DS} \leq -5$ V, V_{GS} = –10 V	P-Ch	39	
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4.5 A	N-Ch	0.148	Ω
		V_{GS} = –10 V, I_D = –3.1 A	P-Ch	0.12	
		V_{GS} = 4.5 V, I_D = 3.9 A	N-Ch	0.058	
		V_{GS} = –4.5 V, I_D = –2.8 A	P-Ch	0.13	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 4.5 A	N-Ch	13	S
		V_{DS} = –15 V, I_D = –3.1 A	P-Ch	7.4	
Diode Forward Voltage[a]	V_{SD}	I_S = 2 A, V_{GS} = 0 V	N-Ch	0.81	V
		I_S = –2 V, V_{GS} = 0 V	P-Ch	–0.80	
Dynamic[b]					
Total Gate Charge[b]	Q_g	N-Channel V_{DS} = 30 V, V_{GS} = 10 V, I_D = 4.5 A P-Channel V_{DS} = –10 V, V_{GS} = –30 V, I_D = –3.1 A	N-Ch	16	nC
			P-Ch	16	
Gate-Source Charge[b]	Q_{gs}		N-Ch	4	
			P-Ch	4	
Gate-Drain Charge[b]	Q_{gd}		N-Ch	3	
			P-Ch	1.6	
Turn-On Delay Time[b]	$t_{d(on)}$	N-Channel V_{DD} =30 V, R_L = 30 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = –30 V, R_L = 30 Ω $I_D \cong$ –1 A, V_{GEN} = –10 V, R_G = 6 Ω	N-Ch	29	ns
			P-Ch	18	
Rise Time[b]	t_r		N-Ch	9	
			P-Ch	10	
Turn-Off Delay Time[b]	$t_{d(off)}$		N-Ch	35	
			P-Ch	10	
Fall Time[b]	t_f		N-Ch	7	
			P-Ch	27	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2 A, di/dt = 100 A/µs	N-Ch	35	
			P-Ch	52	

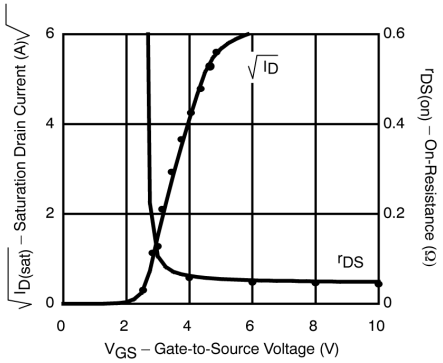
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

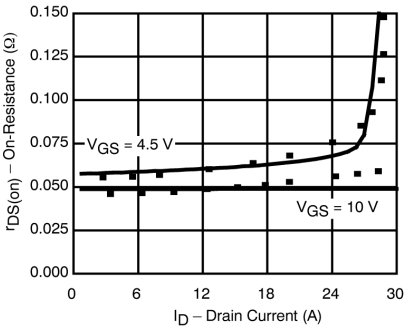
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

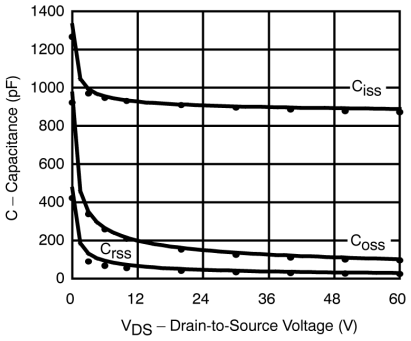
N-Channel MOSFET

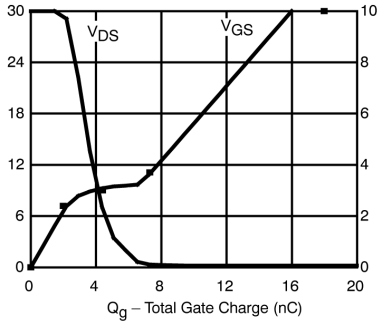






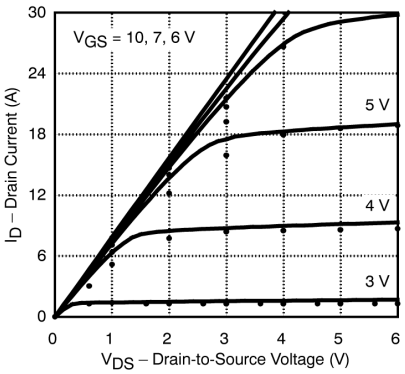


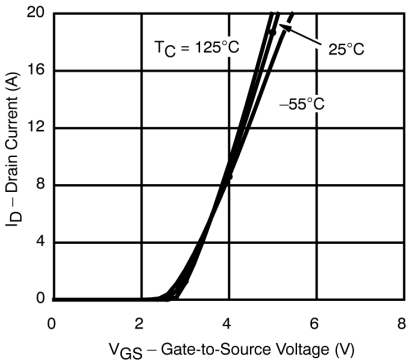


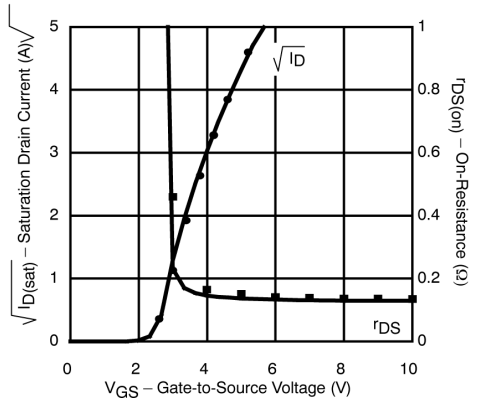


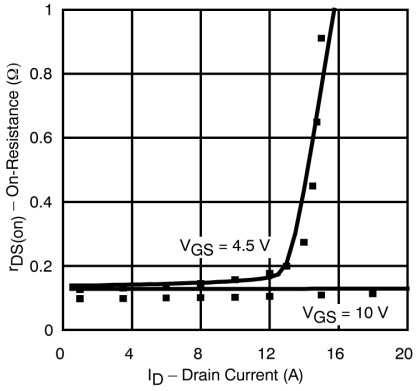
Note: Dots and squares represent measured data.

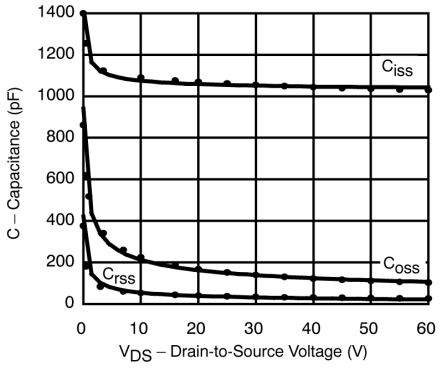
P-Channel MOSFET

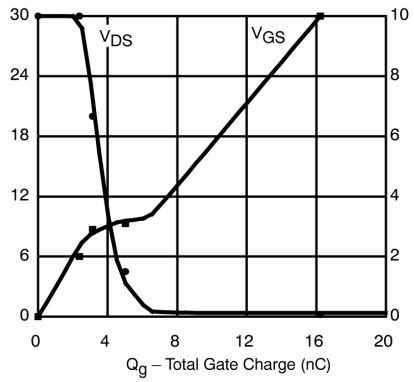












Note: Dots and squares represent measured data.