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DESCRIPTION

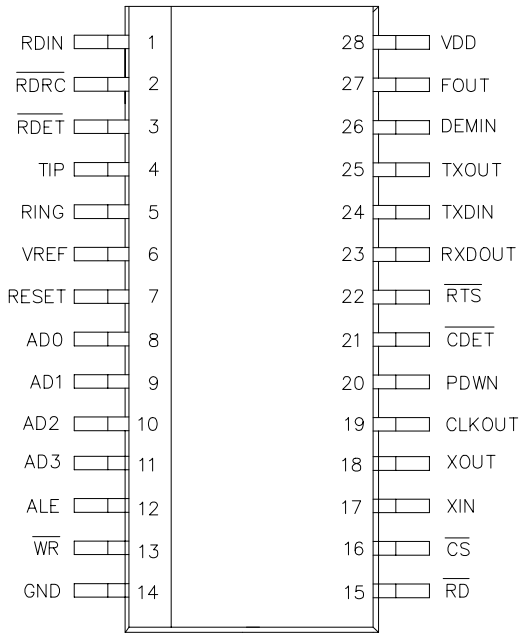
The SB7310 is a single-chip Modem IC which provides the functions necessary to implement either a V.23 compliant modem or a Bell 202 modem. The SB7310 also provides important functions for remote industrial applications such as, Caller ID, DTMF Tone Generation and Call Progress Tone Detection. The SB7310 operates up to 1200 BPS in half-duplex mode over 2 wires or full-duplex mode over 4 wires.

The SB7310 is fabricated in a low voltage CMOS process and is assembled in a 28 pin SOP plastic package. The SB7310 operates from a single 3.3 Volt supply with very low power consumption.

FEATURES

- Continuous phase FSK modulation and demodulation.
- CCITT V.23 or Bell 202 2 wire half duplex or 4 wire full duplex operation
- Host 8051 CPU DTE interface
- Parallel microprocessor bus for control and serial port for data transfer
- DTMF and Call Progress Tones generator and Call Progress Tones Detection
- Test modes available: ALB, Mark, Space, Alternating bit patterns
- High input sensitivity (-48dBm Typical)
- Calling Number Delivery (CND)
- Calling Name Delivery (CNAM)
- Power down mode
- Single DC power supply operation
- 3.3 Volt - 6 Volt operation
- Low operation current

PIN CONFIGURATION



APPLICATIONS

- Gas, Electric, Water meter reading
- Vending machine data reading
- Copier data collection and monitoring
- Security monitoring and control
- Smart Card data transaction
- Office/Home appliance control & Monitoring

ORDERING INFORMATION

DEVICE(1)	PACKAGE	TEMP. (T_J)
SB7310S	SOP-28	-40 to +85°C

Note:
(1) Add suffix 'TR' for tape and reel.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
Supply Voltage		-0.3 to 7.0	V
Input Voltage (All pins)	V_{IN}	-0.3 to V_{DD}+0.3	V
Storage Temperature Range	T_{STG}	-40 to +125	°C
Operating Junction Temperature Range	T_J	-40 to +85	°C

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PIN DESCRIPTION

Pin No.	Symbol	Pin Type[1]	Power Down Status	Description
1	RDIN	SI	ACTIVE	**Ring Detect Input:** The attenuated ring signal is connected to this pin.
2	RDRC	SI / OD	ACTIVE	**Ring Detect RC Input / Output:** The RC network will be connected to this pin to set time delay for ring signal.
3	RDET	O	ACTIVE	**Ring Detect Output:** This pin is the output for the ring signal. The low level indicates that the ring signal is detected..
4	TIP (RXA+)	AI	OFF	**Tip input:** This pin is connected to the Tip side of the twisted pair telephone lines. This pin must be DC isolated from the phone lines. Under the power down mode, this pin is functionally disconnected from the internal circuitry.
5	RING (RXA-)	AI	OFF	**Ring input:** This pin is connected to the Ring side of the twisted pair telephone lines. This pin must be DC isolated from the phone lines. Under the power down mode, this pin is functionally disconnected from the internal circuitry.
6	VREF	AO	HIGH-Z	**Voltage Reference Output:** Internally generated reference voltage output. A 0.1µF bypass capacitor is connected between this pin and GND. Under the power down mode, this pin becomes high impedance.
7	RESET	SI	ACTIVE	**Reset Input:** High level is active. An external resistor to GND and a capacitor to VDD connected to this pin allows power on reset function. All control registers contents will be cleared to “0” when this pin is set to high level.
8-11	AD0-AD3	I / O	HIGH-Z OFF	**Data/Address Bus for Host CPU Interface:** This bi-directional tri-state multiplexed lines carry information to and from the internal registers. Under the power down mode, these pins become high impedance and are disconnected from the internal circuitry.
12	ALE	I	OFF	**Address Latch Enable Input:** The falling edge of ALE latches the address on AD0-AD3. Under the power down mode, this pin is disconnected from the internal circuitry.
13	WR	I	OFF	**Write Signal Input:** Low level is active. Data on the AD0-3 bus is latched on the rising edge of WR while CS is low level. Under the power down mode, this pin is disconnected from the internal circuitry to prevent registers from being updated.
14	GND	-	-	**Device Ground:** Connect to the system ground level.
15	RD	I	OFF	**Read Signal Input:** Low level is active. Data is outputted on the AD0-3 bus with low level of RD while CS is low. Under the power down mode, this pin is disconnected from the internal circuitry.
16	CS	I	OFF	**Chip Select Input:** Low level is active. Keep low for read/write operation. Under the power down mode, this pin is disconnected from the internal circuitry.
17	XIN	I	OFF	**Crystal Oscillator Input:** Crystal is connected to this pin. XIN can be driven from an external clock. Under the power down mode, this pin is disconnected from the internal circuitry.

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PIN DESCRIPTION (Cont.)

Pin No.	Symbol	Pin Type[(1)]	Power Down Status	Description
18	XOUT	O	HIGH	**Crystal Oscillator Output:** Crystal is connected to this pin. Under the power down mode, this pin is set to high level.
19	CLKOUT	O	HIGH-Z	**Clock Output:** Crystal frequency clock signal is available from this pin. Under the power down mode, this pin becomes high impedance.
20	PDWN	SI	ACTIVE	**Power Down Input:** This pin must be kept at low level for the normal operation. When it is high, the device will be in the power down mode.
21	CDET	O	HIGH-Z	**Carrier Detect Output:** Low level is active. Under power down mode, this pin becomes high impedance.
22	RTS	I	OFF	**Request to Send Input:** Low level is active. When it is low the modem starts to transmit an FSK signal. Keep this pin at high level when using RTS bit in the register. Under the power down mode, this pins is disconnected from the internal circuitry.
23	RXDOUT	O	HIGH-Z	**Receive Data Output:** Serial receive data output to the Host CPU. Under the power down mode, this pin becomes high impedance. Mark = “1” and Space = “0” at this pin.
24	TXDIN	I	OFF	**Transmit Data Input:** Serial transmit data from the Host CPU. Keep this pin at high level when using TXD bit in the register for the transmission. Under the power down mode, this pins is disconnected from the internal circuitry. Mark = “1” and Space = “0” at this pin.
25	TXOUT (TXA)	AO	HIGH-Z	**Transmit Signal Output:** Analog FSK signal, tone signal or DTMF tone signal will be transmitted from this pin. Under the power down mode, this pin becomes high impedance.
26	DEMIN	AI	VREF	**Demodulator Input:** This pin must be connected to FOUT pin through a 0.01µF capacitor.
27	FOUT	AO	HIGH-Z	**Receive Filter Output:** This pin must be connected to DEMIN pin through a 0.01µF capacitor. Under the power down mode, this pin becomes high impedance.
28	VDD	-	-	**Power supply Input:** DC supply voltage is connected between this pin and GND pin.

Note:
(1) The legend for pin types. SI: Schmitt Input, I: CMOS Input, AI: Analog Input, O: CMOS Output, OD: NMOS Open Drain Output, AO: Analog Output

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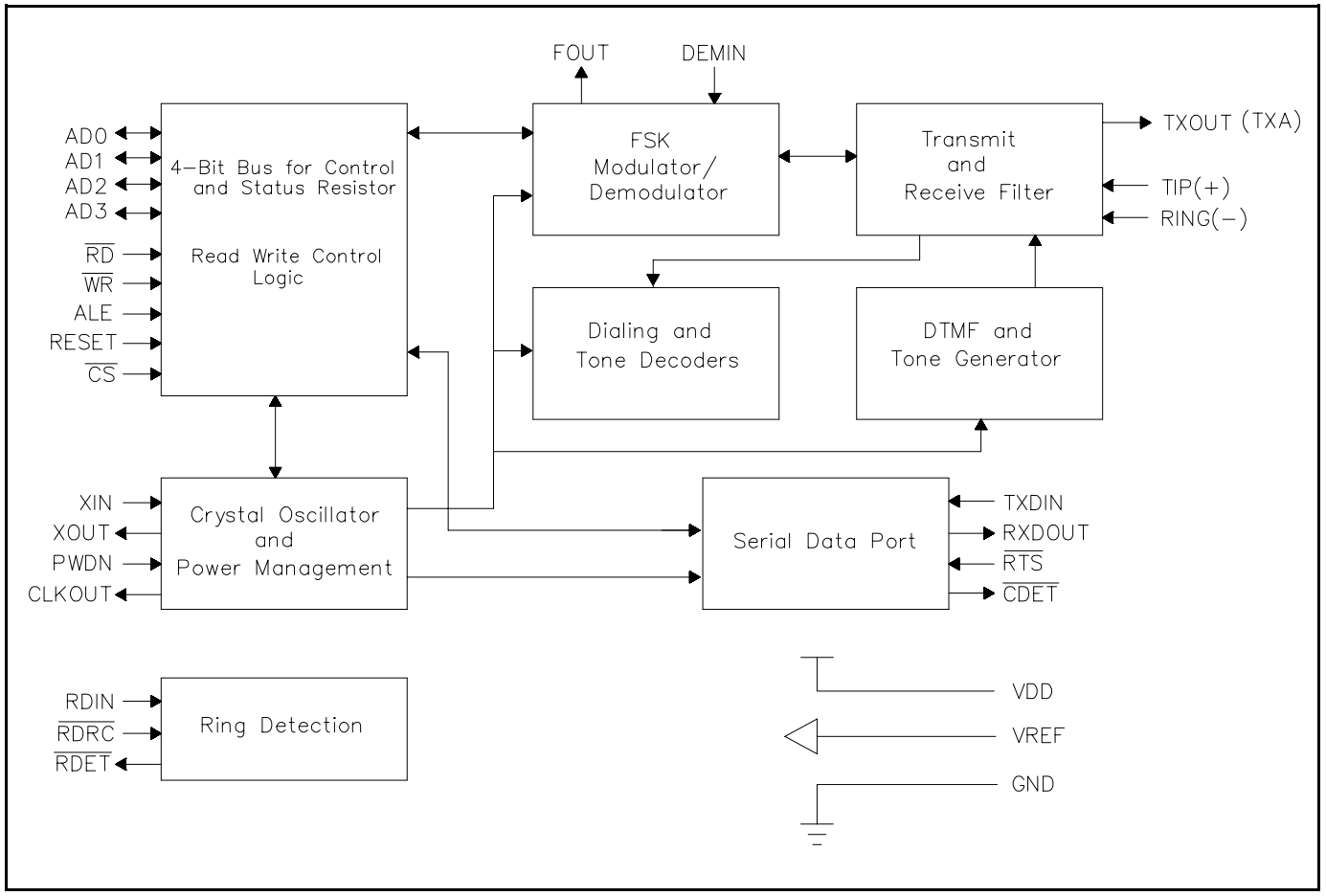
SYSTEM DESCRIPTION

The SB7310 is a CMOS device designed to support the CCITT V.23 or Bell 202 Modem applications. It includes the FSK modulator/demodulator functions, Call-Progress Tones detection, Handshake Tones generation and is capable of producing DTMF tones. The SB7310 has three pins which are allocated to Ring Signal Detection for Caller ID applications.

BLOCK DIAGRAM



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OPERATION

FSK Modulator and Demodulator

The FSK Modulator produces a frequency shift keying modulated analog signal which uses two discrete frequencies to represent the transmit data. CCITT V.23 uses 1300 Hz for Mark and 2100 Hz for Space transmission. Bell 202 uses 1200 Hz for Mark and 2200 Hz for Space transmission. The DAC output signal is filtered by the switched capacitor filtering (SCF) transmit filter and smoothing filter to remove high frequency components. The signal is then amplified by a programmable gain stage. The FSK demodulator consists of a input gain stage, receive filter, proprietary FSK demodulator and Carrier Detect circuit.

Parallel Bus interface

Eight 4-bit registers are provided to the user for control, status, monitoring and mode selection of the modem. The first four consecutive registers are read/write registers and are allocated to control and set the modem to any mode. The fifth register is a read only status register to monitor different modem signal status outputs. The sixth register is a read/write register and contains the four-digit DTMF digit information to be transmitted. The seventh register is a test register reserved by the manufacturer for internal use and future application. The eighth register is a read only register for device ID identification. All these registers are accessible via a 4-bit parallel bus interface to a host CPU.

Serial Data Transfer

The typical RS232 Modem signals TXD, RXD, and RTS can be controlled externally, not only through the registers bits but also from the dedicated I/O pins.

DTMF Generator

The DTMF generator will generate two different DTMF Tones which correspond one of the 16 standard 4-bit digits. Dialing will be initiated by selecting DTMF mode and using Tone register and Transmit Enable or RTS input.

Call Progress Tones

When the receive condition is set by RTS bit, the normal receive filter characteristics can be converted to detect Call Progress Tone frequencies by setting Call Progress Mode bit.

Line Reversal and Ring Signal Detection

The application circuit in Figure 3 shows the implementation of Line Reversal and Ring Signal detection for Caller ID applications. The Line Reversal or Ring Signal will increase the RDIN voltage above the Schmitt trigger circuit high going threshold VT+. A resistor to VDD and capacitor to VSS should be connected externally to set the time interval from RDIN returning low to RDET going high. Normally, RDIN is at GND and RDET is high. When the Ring Signal occurs or Line Reversal occurs, RDIN rises above VT+ level. The capacitor at RDRC discharges. This event causes the second Schmitt trigger output RDET change from high to low. The RDET pin follows the Ring Signal cadence or gives one negative going pulse for the Line Reversal event with an adjustable delay. The details of the implementation and selection of external components are given in the Application Section.

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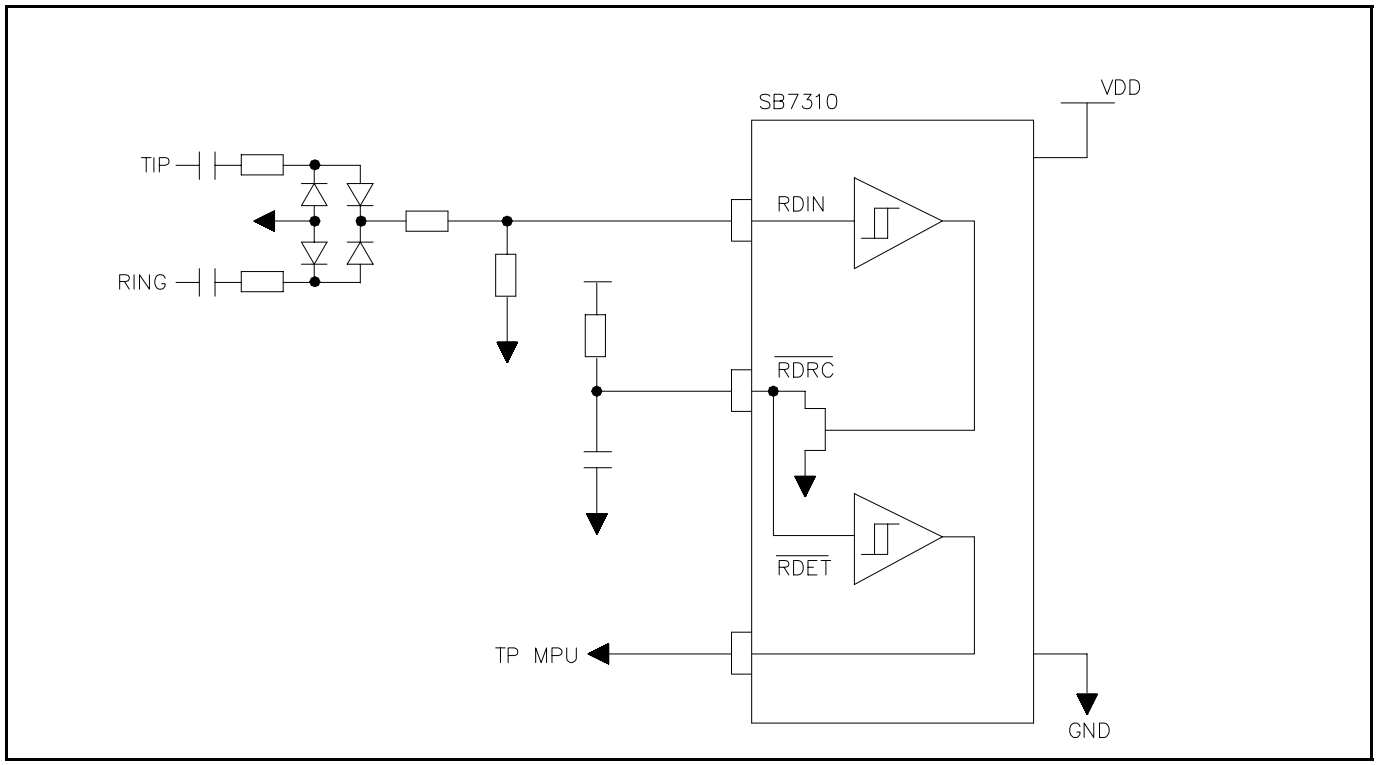

Figure 1. Application Example: Line Reversal or Ring Signal Detection

FSK Demodulation

The FSK signal is band-pass filtered and then demodulated according to a proprietary DPLL technique. A carrier detector provides the indication of a received signal level that is above -43dBm and below - 48dBm. The following table gives the FSK signal characteristics for two different specs.

FSK Signal Characteristics

ITEM	CCITT V.23	USA Bell 202
Mark frequency	1300Hz ± 1.5%	1200Hz ± 1%
Space frequency	2100Hz ± 1.5%	2200Hz ± 1%
Received signal: mark/Space	-9dBm to -48dBm	0dBm to -45dBm(1)
Transmission Rate	1200Baud ± 1%	1200Baud ± 1%

Note:
(1) The signal power is expected in dBm referenced to a 600 Ω termination at the CPE tip and ring interface.

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Carrier Detection

The carrier detection is the indication of energy in the FSK signal spectrum. It detects the presence of any FSK signal tones that will be in the band. When the CDET output is high which corresponds the non-existence of receive signal, the RXD output will stay high level. Because speech or any other tones also lie in the FSK frequency band, the CDET detector can respond to these signals.

Power Down

The SB7310 may be put into a low-power mode by setting the PDWN pin high. This feature does not affect the RDIN, RDRC and RDET operations.

HOST INTERFACE REGISTER BIT DESCRIPTIONS

Eight 4-bit internal registers are accessible for control and status monitoring. The AD0-AD3 lines are latched by ALE as addressing eight memory locations, starting from “0000” to “0111” values.

Register Name	ADDRESS (AD3-AD0)	Mode	D3	D2	D1	D0
CR0	X000	Read/ Write	FD	RTS	M1	M0
CR1	X001	Read/ Write	T2113	V23	T1	T0
CR2	X010	Read/ Write	TP1	TP0	DL	AL
CR3	X011	Read/ Write	N/A	N/A	RESET	TXDIN
SR4	X100	Read	N/A	RI	CD	RXDOUT
DTMFR5	X101	Read/ Write	DTMF3	DTMF2	DTMF1	DTMF0
TESTR6	X110	Read/ Write	N/A	TEST2	TEST1	TEST0
IDR7	X111	Read	0	0	N/A	N/A

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Control Register 0: CR0

Bit No.	Name	Mode	Description
D3	**FD** FSK Full Duplex Mode	Read/ Write	This bit controls full or half duplex mode: FD bit — mode 0 — half duplex mode 1 — full duplex mode When the full duplex mode is selected, the receiver function is always enabled. When the half duplex mode is selected, receiver function is enabled only if RTS bit is set to "0" and RTS pin is high level. CD is always active even if FD=0 and RTS=1.
D2	**RTS** Transmit Enable	Read/ Write	This bit controls transmit mode. When this bit is used to control transmit status, the RTS pin must be connected to high level. This bit must be set to logic "0" when RTS pin is used instead. The next table shows the relationship between this bit and RTS pin under the various modes: RTS bit / RTS pin / mode 0 / 1 / receive mode X / 0 / transmit mode for half duplex transmit and receive modes for full duplex 1 / X / the same as above
D1/D0	**M1/M0** Mode1/ Mode0	Read/ Write	D1/D0 pattern selects four different modem configurations as follows: M1 bit / M0 bit / mode 0 / 0 / FSK mode 0 / 1 / Tone mode 1 / 0 / DTMF mode 1 / 1 / Call progress mode

*In FSK mode, data determined the 1300Hz/2100Hz selection. In Tone mode, CR1 bit D3 does the selection.

Control Register 1: CR1

Bit No.	Name	Mode	Description
D3	**T2113** Tone 2100Hz/ 1300Hz	Read/ Write	Logic "0" selects 2100 Hz Answer Tone transmission or reception depending on RTS condition when the Tone mode is selected. Logic "1" selects 1300Hz for the above conditions. T2113 bit — Tone 0 — 2100 Hz 1 — 1300Hz
D2	**V23** V23 or Bell 202 Carriers	Read/ Write	D2 bit select two deferent mode as follows: V23 bit — mode 0 — Bell202 mode 1 — V.23 mode

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Control Register 1: CR1 (Cont.)

Bit No.	Name	Mode	Description
D1/D0	**T1/T0** Transmit Level Attenuation	Read/ Write	These bits select the transmit signal level attenuation as follows: T1 bit / T0 bit / Transmit Level Attenuation 0 / 0 / 0.0 dB 0 / 1 / -1.5 dB 1 / 0 / -3.0 dB 1 / 1 / -4.5 dB

Control Register: CR2

Bit No.	Name	Mode	Description
D3/D2	**TP1/TP0** Transmit Pattern	Read/ Write	These bits select the transmit data patterns as follows: TP1 bit / TP0 bit / transmit data pattern 0 / 0 / Normal Data 0 / 1 / Space (“0”) 1 / 0 / Alternating mark/space pattern 1 / 1 / Mark (“1”)
D1	**DL** Digital Loop-Back	Read/ Write	Logic “1” level connects TXDIN signal input to the RXDOUT pin for Local Digital loop-back test. DL bit / mode 0 / local digital loop back disabled 1 / local digital loop back enabled
D0	**AL** Analog Loop-Back	Read/ Write	Logic “1” level connects TXOUT signal output to the receive input for Local Analog loop-back test. RTS and FD bit must be set to “1” for analog loop back test AL bit / mode 0 / local analog loop back disabled 1 / local analog loop back enabled

Control Register: CR3

Bit No.	Name	Mode	Description
D3	-	-	Not Used
D2	-	-	Not Used
D1	**RESET** Register Reset	Read/ Write	Logic “1” level resets all the register bits to logic “0” level except this bit. This bit must be cleared first by writing logic “0” to this bit position prior to writing to another bit position. This bit is cleared when RESET pin is set to high.

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Control Register: CR3 (Cont.)

Bit No.	Name	Mode	Description
D0	**TXDIN** Transmit Data	Read/ Write	The data written to this bit position will be inverted, then transmitted from the TXOUT pin. When this bit is used, the data transmission TXDIN pin must be connected to high level. When the TXDIN pin is used for transmission, this bit must be kept at logical "0". The next table shows the relationship between this bit and TXDIN pin under the various modes: TXDIN bit / TXDIN pin / mode 0 / 1 / Mark signal will be transmitted 1 / 1 / Space signal will be transmitted 0 / 0 / the same as above 1 / 0 / not allowed

Status Register: SR4

Bit No.	Name	Mode	Description
D3	-	-	Not Used
D2	**RI** Ring Indicator	Read	The Ring Indicator Output Logic "1" level shows the existence of a receive Ring signal The output follows the cadence of the Ring Signal. RI bit / condition 0 / no ring detected 1 / ring detected
D1	**CD** Carrier Detect	Read	Shows the existence of the energy in the corresponding frequency band at receiver input. The following table shows the relationship between inputs and CD output indication. CD bit conditions 0 / no energy detected at receiver input 1 / energy detected at receiver input
D0	**RSDOUT** Receive Data	Read	The inverse polarity of the receive data which is also available at pin 23 is read from this bit position.

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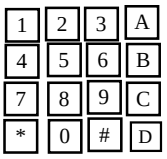
Control Register: DTMFR5

Bit No.	Name	Mode	Description
D3-D0	**DTMF3-0** DTMF Digits	Read/ Write	Four bit pattern will give 16 different High and Low tone combination for the DTMF Tone Generation. The following table gives transmitted digits versus D3-D0 pattern which has to written to this DTMFR5 Register and transmitted frequencies for each digit.

Digit	DTMF3-0	Frequency
1	0000	697Hz+1209Hz
2	0001	697Hz+1336Hz
3	0010	697Hz+1477Hz
A	0011	697Hz+1633Hz
4	0100	770Hz+1209Hz
5	0101	770Hz+1336Hz
6	0110	770Hz+1477Hz
B	0111	770Hz+1633Hz
7	1000	852Hz+1209Hz
8	1001	852Hz+1336Hz
9	1010	852Hz+1477Hz
C	1011	852Hz+1633Hz
*	1100	941Hz+1209Hz
0	1101	941Hz+1336Hz
#	1110	941Hz+1477Hz
D	1111	941Hz+1633Hz



Test Register: TESTR6

Bit No.	Name	Mode	Description
D2-D1	**TEST2/ TEST1**	Read/ Write	**Both bits must be set to logic "0" for the normal operation**

Device ID Register: IDR7
(NOTE: These ID bits are for internal purpose only and should not be disclosed to any customers.)

Bit No.	Name	Mode	Description
D3-D2	Device ID	Read	These 2 bits indicate device ID. For SB7310, these bits are always read as **0 0**.

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ELECTRICAL CHARACTERISTICS

All MAX and MIN limits in electrical characteristics are the design target values. These values may be changed during design and/or device characterization.

DC ELECTRICAL CHARACTERISTICS

Unless specified, V_{DD} = 5V±10%, T_A = -40°C to 85°C. Typical values are at V_{DD} = 5V, T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Voltage Range	V_{DD}		3.3	5	6	V
Supply Current	I_{DD}	All outputs open, V_{DD}=5V, PDWN = 0V		5	7	mA
Power Down Supply Current	I_{PD}	All outputs open, V_{DD} = 5V, PDWN = V_{DD}			1	µA
Input Low Voltage	V_{IL}	$\overline{AD0\text{-}3}$, $\overline{WR}$, RD, $\overline{ALE}$, CS, TXD, RTS, XIN pins			0.3xV_{DD}	V
Input High Voltage	V_{IH}	$\overline{AD0\text{-}3}$, $\overline{WR}$, RD, $\overline{ALE}$, CS, TXD, RTS, XIN pins	0.7xV_{DD}			V
Input Low Threshold Voltage	V_{T-}	RESET, $\overline{RDRC}$, RDIN, PDWN pins. V_{DD} = 5V		2		V
Input High Thresh-old Voltage	V_{T+}	RESET, $\overline{RDRC}$, RDIN, PDWN pins. V_{DD} = 5V		3		V
Output Low Voltage	V_{OL}	AD0-3, CLKOUT, $\overline{RDET}$, $\overline{RDRC}$, RXDOUT, $\overline{CDET}$ pins. V_{DD} = 4.5V, I_{OL} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	AD0-3, CLKOUT, $\overline{RDET}$, $\overline{RDRC}$, RXDOUT, $\overline{CDET}$ pins. V_{DD} = 4.5V, I_{OH} = -1.6mA	3.7			V
Input Leakage Current	I_{IN}	AD0-3, $\overline{WR}$, $\overline{RD}$, ALE, $\overline{CS}$, RESET, RDIN, $\overline{TXDIN}$, RTS pins V_{DD} = 5.5V, V_{IN} = 0V/5.5V	-1		+1	µA
Output Leakage Current	I_{OFF}	$\overline{AD0\text{-}3}$, $\overline{RDRC}$, CLKOUT, RXDOUT, $\overline{CDET}$ pins. V_{DD}=5.5V, V_{OUT} = 0V/5.5V, outputs off	-1		+1	µA
Input Impedance	R_{IN1}	TIP, RING pin	175	250	325	kΩ
Input Impedance	R_{IN2}	DEMIN pin	140	200	260	kΩ
Output Load	R_L	FOUT, TXOUT pin, V_{DD} = 5V	20			kΩ

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AC CHARACTERISTICS

Unless specified, V_{DD} = 5V±10%, X_{IN} = 11.0592MHz, T_A = -40°C to 85°.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal					
Frequency		-0.1%	11.0592	+0.1%	MHz
FSK Modulator and Tone Generator					
Output Frequency Error	fxin = 11.0592 MHz	-10		+10	Hz
Harmonic Distortion			-40		dB
Transmit Level	T0=T1=0, R_L=∞, VDD=5V	-12.5	-11	-9.5	dBm
DTMF Generator					
Output Frequency Error	fxin = 11.0592 MHz	-10		+10	Hz
Transmit Level, Low Tones	T0=T1=0, R_L=∞, VDD=5V		-11.5		dBm
Transmit Level, High Tones	T0=T1=0, R_L=∞, VDD=5V		-10		dBm
Twist	T0=T1=0, R_L=∞		1.5		dBm
Carrier Detect					
Carrier Detect ON Sensitivity at DEMIN pin	fIN=1700 Hz, VDD=5V, M1=M0=0	-16	-14	-12	dBm
	fIN=425 Hz, VDD=5V, M1=M0=1	-16	-14	-12	
Carrier Detect OFF Sensitivity at DEMIN pin	fIN=1700 Hz, VDD=5V, M1=M0=0	-19	-17	-15	dBm
	fIN=425 Hz, VDD=5V, M1=M0=1	-19	-17	-15	
Carrier Detect Sensitivity Hysteresis	VDD=5V	2	3	4	dB

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AC CHARACTERISTICS (Cont.)

Unless specified, V_{DD} = 5V±10%, X_{IN} = 11.0592MHz, T_A = -40°C to 85°.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Filter Gain					
Receive Band Pass Filter	fIN=600 Hz, -34dBm		10.5		dB
	fIN=1200 Hz, -34dBm		34		
	fIN=2200 Hz, -34dBm		36		
	fIN=3000 Hz, -34dBm		14		
Call Progress Mode Filter	fIN=150 Hz, -34dBm		10.5		dB
	fIN=300 Hz, -34dBm		34.5		
	fIN=550 Hz, -34dBm		36.5		
	fIN=600 Hz, -34dBm		14.5		
Tone Filter	T2113=0 fIN=1300 Hz, -34dBm		15		dB
	T2113=0 fIN=2100 Hz, -34dBm		36		
	T2113=1 fIN=1300 Hz, -34dBm		35		
	T2113=1 fIN=2100 Hz, -34dBm		16		

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SWITCHING CHARACTERISTICS

Unless specified, VDD = 5V±10%, XIN = 11.0592MHz, T_A = -40°C to 85°C.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Oscillator Startup	t_{DOSC}		2		ms
Power Down to FSK signal receive	t_{SUPD}		8		ms
Carrier detect response time	t_{DAQ}		7		ms
End of FSK signal to Carrier Detect OFF	t_{DCH}		9		ms

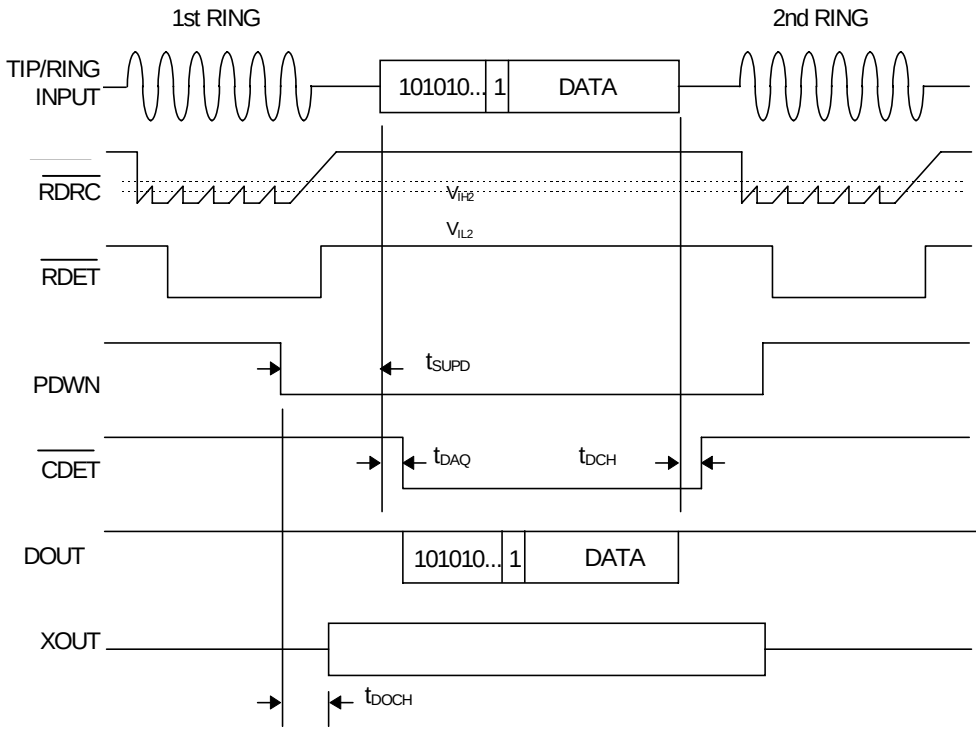

Figure 2. Caller ID Data Timing Diagram

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SWITCHING CHARACTERISTICS for the Host Interface

Unless specified, V_{DD} = 5V±10%, X_{IN} = 11.0592MHz, C_L= 50pF, T_A = -40°C to 85°C.

ALE Width	t_{WALE}	100			ns
ALE low to RD or WR low	t_{ALRW}	150			ns
Data to ALE Setup time	t_{SDA}	30			ns
Data to ALE Hold time	t_{HDA}	40			ns
RD Pulse Width	t_{WRD}	200			ns
Data Output Delay time	t_{DRD}			200	ns
Data Output Hold time	t_{HRD}	10			ns
CS to RD Setup time	t_{SCR}	20			ns
CS to RD Hold time	t_{HCR}	20			ns
Data to WR Setup time	t_{SDW}	100			ns
Data to WR Hold time	t_{HDW}	20			ns
WR Pulse Width	t_{WWR}	200			ns
CS to WR Setup Time	t_{SCW}	20			ns
CS to WR Hold time	t_{HCW}	20			ns

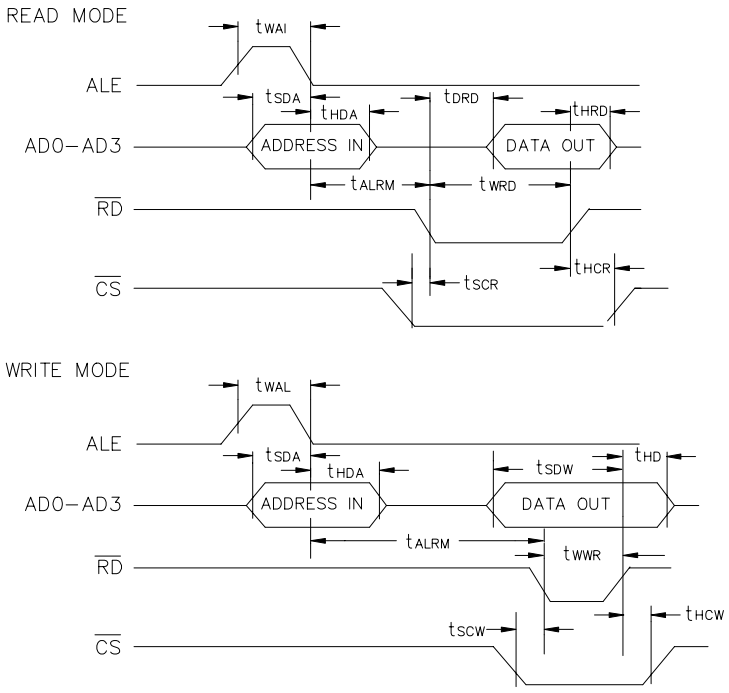

Figure 3. Parallel Data Bus Timing Diagram

HOST CPU INTERFACE TIMING WAVEFORMS

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APPLICATION CIRCUIT EXAMPLES

A typical modem IC uses the TXA and RXA as I/O pins to form telephone interface circuitry called a DAA. The SB7310 TXA function is represented by TXOUT. RXA is replaced by a differential input called TIP and RING. These two pins can be tied to the telephone line TIP and RING through a capacitor for ON-HOOK Caller ID applications. Differential inputs provide better common mode noise rejection and therefore better performance. For modem applications, a single-ended RXA is needed. You can use TIP as RXA+ and leave RING (RXA-) open (no connection).

Two application circuit examples will be provided, one for Caller ID application, and one for modem application. (TBD).

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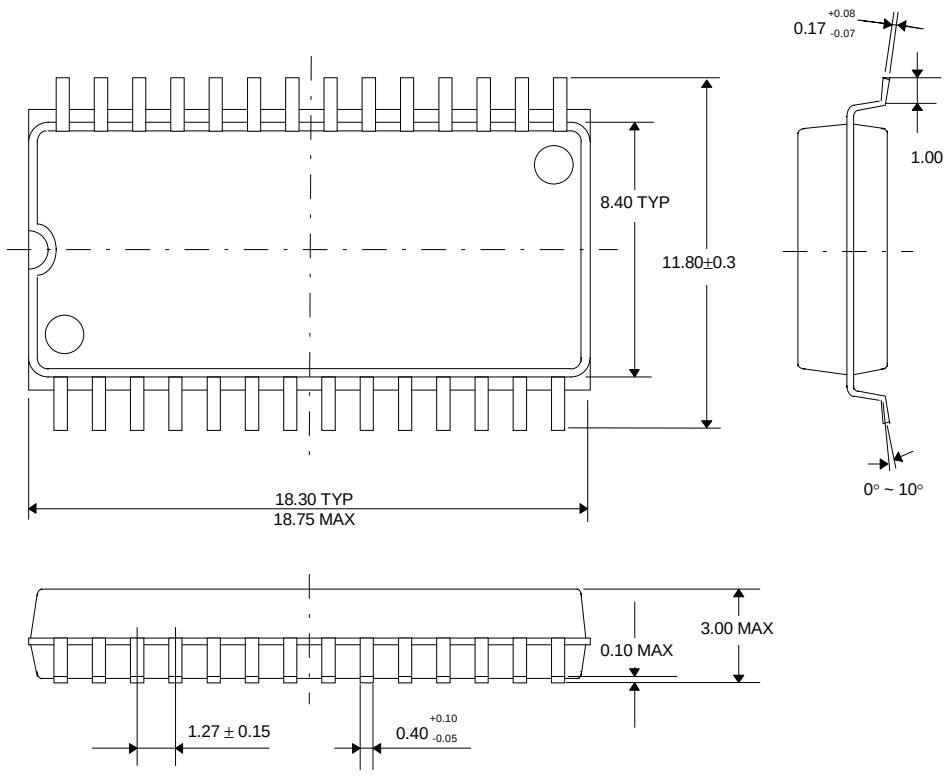
OUTLINE DRAWING - SOP-28



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