SHARP

Microcomputer Data Sheet

SM5K3/SM5K4/SM5K5
4-Bit Single-Chip Microcomputer

FEATURES

- 2,048 × 8-bits ROM Capacity
- 128 × 4-bits RAM Capacity
- 50 Instruction Sets
- 4 Levels of Subroutine Nesting
- Input/Output Ports
  - 8 Input Ports
  - 4 Output Ports
  - Input/Output Ports
    - 12 Ports for the 36-Pin QFP and 32-Pin SOP
    - 11 Ports for the 30-Pin SDIP
    - 8-Pins for the 28-Pin SOP
- Interrupts
  - Internal Interrupt × 1 (Timer)
  - External Interrupt × 2 (2 External Interrupt Inputs)
- A/D Converter
  - 10-bits Resolution
  - 4 Channels
- Timer/Counter 8-bit × 1
- Built-in Main Clock Oscillator Circuit for System Clock
  - Ceramic/Crystal Oscillator (SM5K3/SM5K5)
  - CR Oscillator (SM5K4)
- Signal Generation for Real Time Clock* (SM5K3/SM5K5)
- Built-in 15 Stages Divider for Real Time Clock* (SM5K3/SM5K4)
- Instruction Cycle Time
  - 1 µs (MIN.), 2 MHz, at 5 V ±10% (SM5K3/SM5K5)
  - 2 µs (MIN.), 1 MHz at 2.2 V to 5.5 V (SM5K3/SM5K5)
  - 1 µs (MIN.), 1.67 MHz ±20%, at 5 V ±10% (SM5K4)
- Large Current Output Pins (LED Direct Drive)
  - 15 mA (TYP.) × 4 (Sink Current)
- Supply Voltages
  - 2.2 V to 5.5 V (SM5K3/SM5K5)
  - 2.7 V to 5.5 V (SM5K4)
- Packages
  - 30-pin SDIP (SDIP030-P-0400)
  - 32-pin SOP (SOP032-P-0525)
  - 36-pin QFP (QFP036-P-1010)
  - 28-pin SOP (SOP028-P-0450) (SM5K3/SM5K5)
  - 24-pin SSOP (SSOP024-P-0275) (SM5K4)

**NOTE: ***In case of using crystal oscillator.

DESCRIPTION

The SM5K3/5K4/5K5 are CMOS 4-bit single-chip microcomputers incorporating 4-bit parallel processing function, ROM, RAM, 10-bit A/D converter and timer/counters.

It provides three kinds of interrupts and 4 levels of subroutine stack. Being fabricated through CMOS process, the chip requires less power and available in a small package, best suited for LOW power controlling, compact equipment like a precision charger.

PIN CONNECTIONS

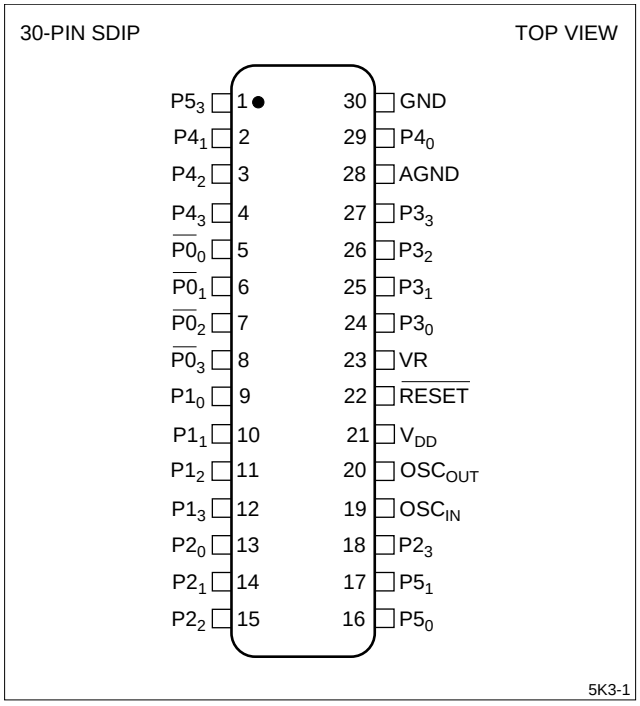


Figure 1. 30-Pin SDIP

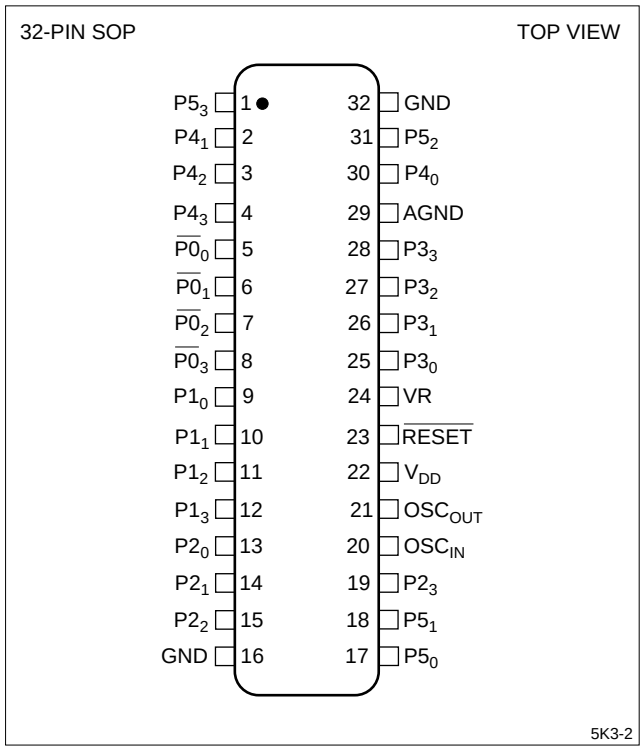


Figure 2. 32-Pin SOP

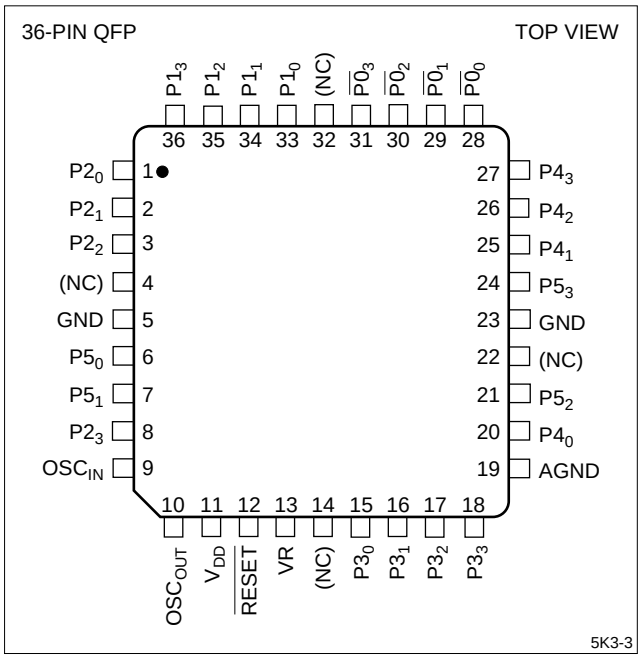


Figure 3. 36-Pin QFP

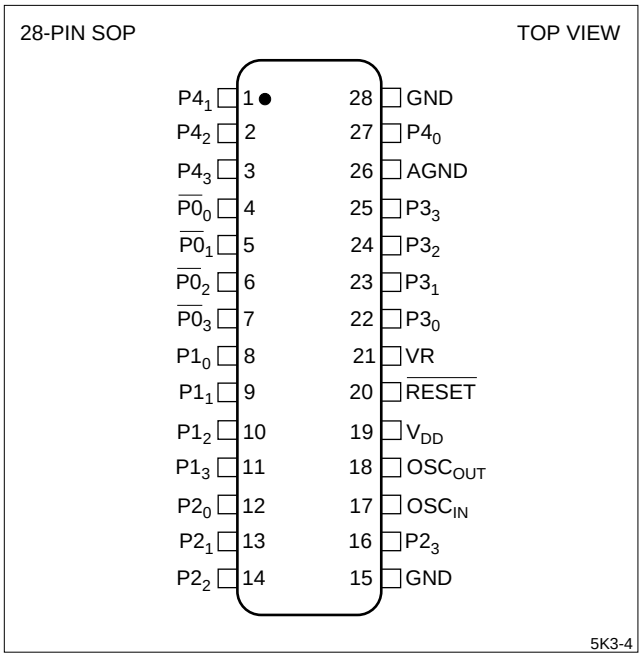


Figure 4. 28-Pin SOP

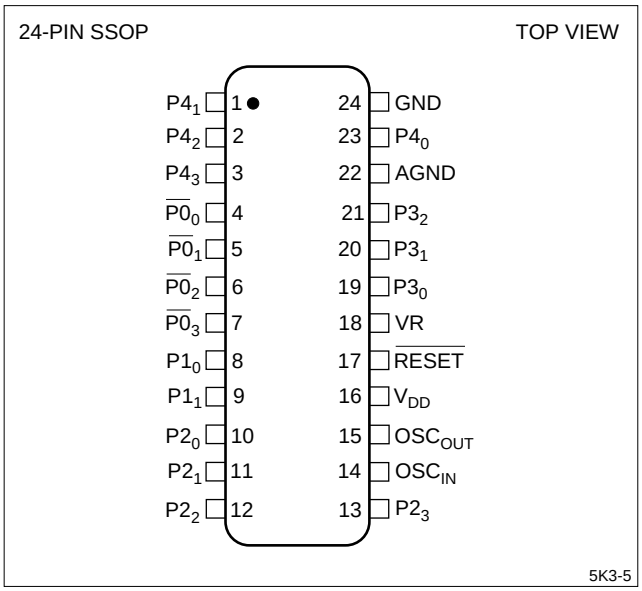
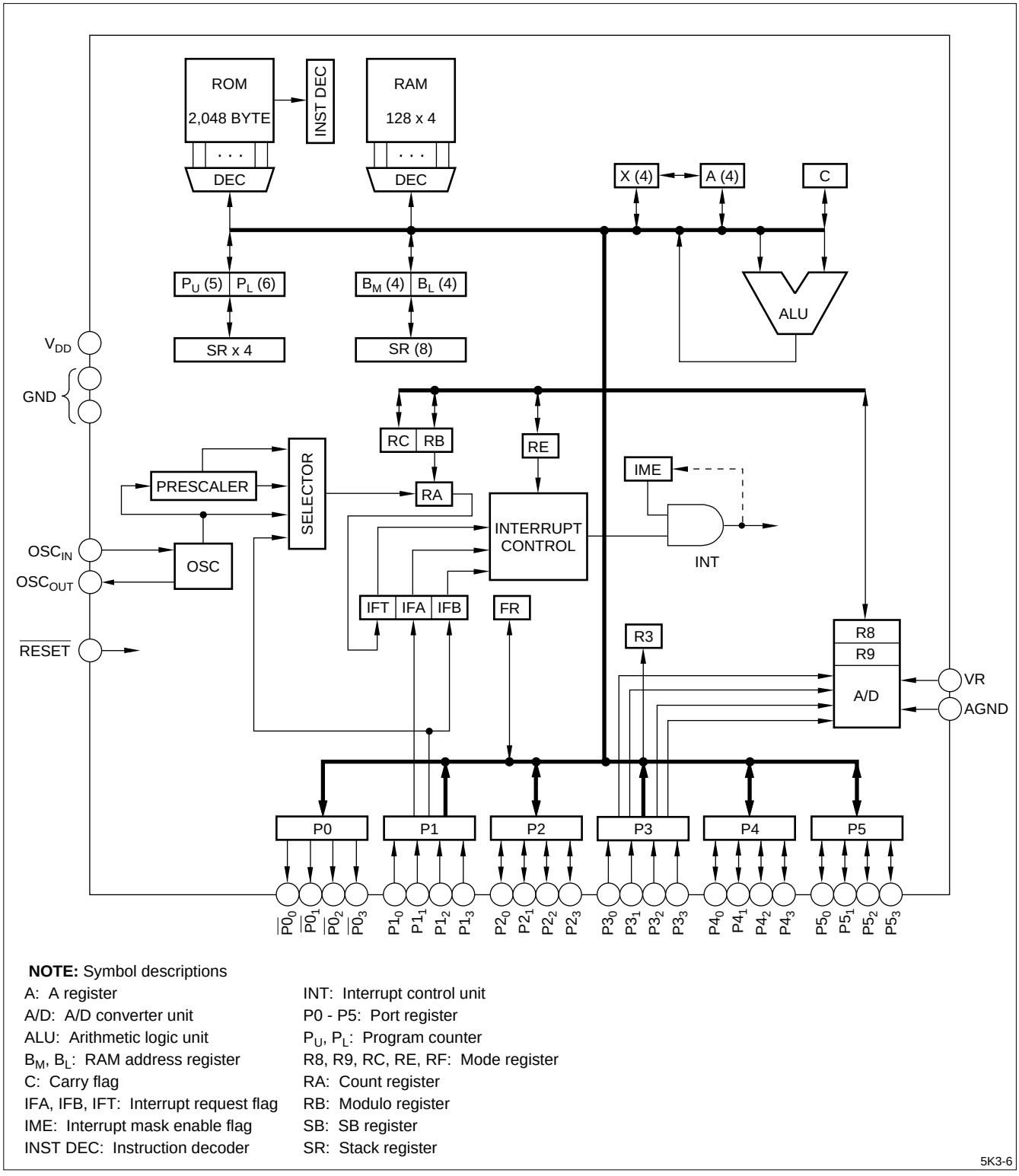


Figure 5. 24-Pin SSOP



NOTE: Symbol descriptions

A: A register
A/D: A/D converter unit
ALU: Arithmetic logic unit
B_M, B_L: RAM address register
C: Carry flag
IFA, IFB, IFT: Interrupt request flag
IME: Interrupt mask enable flag
INST DEC: Instruction decoder
INT: Interrupt control unit
P0 - P5: Port register
P_U, P_L: Program counter
R8, R9, RC, RE, RF: Mode register
RA: Count register
RB: Modulo register
SB: SB register
SR: Stack register

5K3-6

Figure 6. Block Diagram

PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
$\overline{P0_0}$ - $\overline{P0_3}$,	O	High current output (sink current 15 mA)
$P1_0$ - $P1_1$	I	Input (standby release) (counter input $P1_1$) with pull-up resistor
$P1_2$ - $P1_3$	I	Input (standby release) with pull-up resistor
$P2_0$ - $P2_3$	I/O	Input (with pull-up resistor) or output (independent)
$P3_0$ - $P3_3$	I	Input (also used as analog input) with pull-up resistor
$P4_0$ - $P4_3$, $P5_0$ - $P5_3$	I/O	Input (with pull-up resistor) and output
OSC_{IN}, OSC_{OUT}	I/O	Ceramic/crystal oscillation pin (SM5K3/5K5)/CR Oscillation pin (SM5K4)
$\overline{RESET}$	I	Reset signal input with pull-up resistor
VR, AGND	I	A/D converter reference supply input port
V_{DD}, GND	I	Power supply, ground

NOTE: Symbols apply to 32-pin SOP and 36-pin QFP. (In case of 30-pin SDIP, $P5_2$ does not exist.
In case of 28-pin SOP, $P5_0$ - $P5_3$ do not exist. In case of 24-pin SSOP, $P1_2$, $P1_3$, $P3_3$, $P5_0$ - $P5_3$ pins do not exist).

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		-0.3 to +7.0	V
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V
Maximum output current	I_{OH}	HIGH level output current (all outputs)	4	mA
	I_{OL0}	LOW level output current ($\overline{P0_0}$ - $\overline{P0_3}$)	30	mA
	I_{OL1}	LOW level output current (all but $\overline{P0_0}$ - $\overline{P0_3}$)	4	mA
Total output current	ΣI_{OH}	HIGH level output current (all outputs)	20	mA
	ΣI_{OL}	LOW level output current (all outputs)	80	mA
Operating temperature	T_{OPR}		-20 to +70 (SM5K3/5K5) -20 to +85 (SM5K4)	°C
Storage temperature	T_{STG}		-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SM5K3/SM5K5

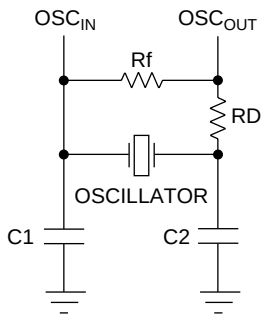
PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply voltage	V_{DD}		2.2 to 5.5	V
Instruction time	T_{SYS}	V_{DD} = 2.2 V to 5.5 V	2 to 5	µs
		V_{DD} = 5.0 V ±10%	1 to 61	µs
Main clock frequency	f_{OSC}	V_{DD} = 2.2 V to 5.5 V	1 M to 32.768 k	Hz
		V_{DD} = 5.0 V to ±10%	2 M to 32.768 k	Hz

SM5K4

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply voltage	V_{DD}		2.7 to 5.5	V
Instruction time	T_{SYS}	V_{DD} = 2.7 V to 5.5 V	2 to 61	µs
		V_{DD} = 5.0 V ±10%	1 to 5	µs
Main clock frequency*	f_{OSC}	V_{DD} = 2.7 V to 5.5 V	1 M to 400 k	Hz
		V_{DD} = 5.0 V to ±10%	2 M to 400 k	Hz

**NOTE: ***Degree of fluctuation frequency ± 20%.

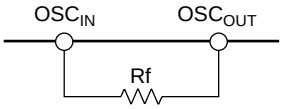
OSCILLATION CIRCUIT



NOTE: Reference only, circuit configuration varies according to oscillator used.

5K3-7

Figure 7. SM5K3/SM5K Circuit Configuration



NOTE: Rf = 33 kΩ (f_{OSC} = 1.67 MHz, TYP.)

5K3-8

Figure 8. SM5K4 Circuit Configuration

NOTES:

1. The typical oscillation frequency shall be determined in consideration of operating condition and fluctuation frequency.
2. Mount Rf, RD, C_1, C_2, Oscillator (SM5K3/SM5K5)/Rf (SM5K4) as close as possible to the oscillator pins of the LSI, in order to reduce an influence from floating capacitance.
3. Since the value of resistor Rf, RD, C_1, C_2, Oscillator (SM5K3/SM5K5)/Rf (SM5K4) varies depending on circuit pattern and others, the final Rf, RD, C_1, C_2, Oscillator (SM5K3/SM5K5)/Rf (SM5K4) value shall be determined on the actual unit.
4. Don't connect any line to OSC$_{IN}$ and OSC$_{OUT}$ except oscillator circuit.
5. Don't put any signal line across the oscillator circuit line.
6. On the multi-layer circuit, do not let the oscillator circuit wiring cross other circuit.
7. Minimize the wiring capacitance of GND and V_{DD}.

DC CHARACTERISTICS

SM5K3

V_{DD} = 5.0 V or 3.0 V, T_{OPR} = -20°C to +70°C (TYP.) unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTES
Input voltage	V_{IH1}		0.8 × V_{DD}		V_{DD}	V	1
	V_{IL1}		0		0.2 × V_{DD}	V	1
	V_{IH2}		0.9 V_{DD}		V_{DD}	V	2
	V_{IL2}		0		0.1 × V_{DD}	V	2
Input current	I_{IL1}	V_{IN} = 0 V, V_{DD} = 2.2 V to 3.3 V	2	25	90	µA	3
		V_{IN} = 0 V, V_{DD} = 4.5 V to 5.5 V	25	70	250	µA	3
	I_{IH1}	V_{IN} = V_{DD}			2	µA	3
	I_{IL2}	V_{IN} = 0 V		1.0	10	µA	4
	I_{IH2}	V_{IN} = V_{DD}		1.0	10	µA	4
Output current	I_{OL1}	V_O = 1.0 V, V_{DD} = 2.2 V to 3.3 V	5	15		mA	5
		V_O = 1.0 V, V_{DD} = 4.5 V to 5.5 V	15	25		mA	5
	I_{OH1}	V_O = V_{DD} – 0.5 V, V_{DD} = 2.2 V to 3.3 V	0.3	1.5		mA	5
		V_O = V_{DD} – 0.5 V, V_{DD} = 4.5 V to 5.5 V	1.0	2.2		mA	5
	I_{OL2}	V_O = 1.5 V, V_{DD} = 2.2 V to 3.3 V	1.2	5.0		mA	6
		V_O = 1.5 V, V_{DD} = 4.5 V to 5.5 V	5	9.0		mA	6
	I_{OH2}	V_O = V_{DD} – 0.5 V, V_{DD} = 2.2 V to 3.3 V	0.3	2.0		mA	6
		V_O = V_{DD} – 0.5 V, V_{DD} = 4.5 V to 5.5 V	1.0	2.4		mA	6
	I_{OH3}	V_{OH} = V_{DD} – 1.0 V, V_{DD} = 2.2 V to 3.3 V	0.15			mA	7
		V_{OH} = V_{DD} – 1.0 V, V_{DD} = 4.5 V to 5.5 V	0.5			mA	7

NOTES:

1. Applicable pins; $P1_2$, $P1_3$, $P2_0$ - $P2_3$, $P3_0$ - $P3_3$ (digital input mode), $P4_0$ - $P4_3$, $P5_0$ - $P5_3$.
2. Applicable pins: $\overline{OSC_{IN}}$, $\overline{RESET}$, $P1_0$, $P1_1$.
3. Applicable pins: $\overline{RESET}$, $P1_0$ - $P1_3$, $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (digital input mode).
4. Applicable pins: $P3_0$ - $P3_3$ (analog input mode).
5. Applicable pins: $P0_0$ - $P0_3$ (high current mode).
6. Applicable pins: $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (output mode). (See note 11.)
7. Applicable pins: $P3_0$ - $P3_3$. (See note 12.)
8. No load (A/D conversion is stop).
9. A/D conversion in operation (operation enable).
10. A/D conversion in stop (operation disable).
11. In case of 32-pin SOP and 36-pin QFP. In case of 30-pin SDIP, $P5_2$ does not exist. In case of 28-pin SOP, $P5_0$ - $P5_3$ do not exist.
12. P3 ports are normally used for input ports with pull-up resistor. These ports can be also used.

SM5K3 (Cont'd)

V_{DD} = 5.0 V or 3.0 V, T_{OPR} = -20°C to + 70°C (TYP.) unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTES
Supply current	I_{DD}	f_{OSC} = 2 MHz, V_{DD} = 4.5 V to 5.5 V		1,200	2,500	µA	8
		f_{OSC} = 1 MHz, V_{DD} = 2.2 V to 3.3 V		300	800	µA	8
		f_{OSC} = 1 MHz, V_{DD} = 4.5 V to 5.5 V		600	1,200	µA	8
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 2.2 V to 3.3 V		20	120	µA	8
	I_{HLT}	f_{OSC} = 2 MHz, V_{DD} = 4.5 V to 5.5 V		760	1,500	µA	8
		f_{OSC} = 1 MHz, V_{DD} = 2.2 V to 3.3 V		200	600	µA	8
		f_{OSC} = 1 MHz, V_{DD} = 4.5 V to 5.5 V		400	900	µA	8
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 2.2 V to 3.3 V		20	75	µA	8
	I_{STOP}	Ceramic OSC mode, V_{DD} = 2.2 V to 3.3 V			2	µA	8
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 2.2 V to 3.3 V		15	40	µA	8
	I_{VR}	A/D in operation, V_{DD} = 4.5 V to 5.5 V		220	450	µA	9
		A/D in stop, V_{DD} = 4.5 V to 5.5 V			2	µA	10
A/D conversion	Resolution			10		bit	
	Differential linearity error	f_{OSC} = 1 MHz, T_{OPR} = 25°C, V_{DD} = VR = 5.0 V		±2.5	±4.0	LSB	
	Sequential linearity error			±3.2	±5.0	LSB	
	Total error			±4.0	±6.0	LSB	

NOTES:

1. Applicable pins; $P1_2$, $P1_3$, $P2_0$ - $P2_3$, $P3_0$ - $P3_3$ (digital input mode), $P4_0$ - $P4_3$, $P5_0$ - $P5_3$.
2. Applicable pins: $\overline{OSC_{IN}}$, $\overline{RESET}$, $P1_0$, $P1_1$.
3. Applicable pins: $\overline{RESET}$, $P1_0$ - $P1_3$, $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (digital input mode).
4. Applicable pins: $P3_0$ - $P3_3$ (analog input mode).
5. Applicable pins: $P0_0$ - $P0_3$ (high current mode).
6. Applicable pins: $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (output mode). (See note 11.)
7. Applicable pins: $P3_0$ - $P3_3$. (See note 12.)
8. No load (A/D conversion is stop).
9. A/D conversion in operation (operation enable).
10. A/D conversion in stop (operation disable).
11. In case of 32-pin SOP and 36-pin QFP. In case of 30-pin SDIP, $P5_2$ does not exist. In case of 28-pin SOP, $P5_0$ - $P5_3$ do not exist.
12. P3 ports are normally used for input ports with pull-up resistor. These ports can be also used.

SM5K4

V_{DD} = 5.0 V or 3.0 V, T_{OPR} = -20°C to +85°C (TYP.) unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTES
Input voltage	V_{IH1}		0.8 × V_{DD}		V_{DD}	V	1
	V_{IL1}		0		0.2 × V_{DD}	V	1
	V_{IH2}		0.9 × V_{DD}		V_{DD}	V	2
	V_{IL2}		0		0.1 × V_{DD}	V	2
Input current	I_{IL1}	V_{IN} = 0 V, V_{DD} = 2.7 V to 3.3 V	1.0	25	90	µA	3
		V_{IN} = 0 V, V_{DD} = 4.5 V to 5.5 V	15	70	250	µA	3
	I_{IH1}	V_{IN} = V_{DD}			3.0	µA	3
	I_{IL2}	V_{IN} = 0 V		1.0	10	µA	4
	I_{IH2}	V_{IN} = V_{DD}		1.0	10	µA	4
Output current	I_{OL1}	V_O = 1.0 V, V_{DD} = 2.7 V to 3.3 V	3	15		mA	5
		V_O = 1.0 V, V_{DD} = 4.5 V to 5.5 V	12	25		mA	5
	I_{OH1}	V_O = V_{DD} – 0.5 V, V_{DD} = 2.7 V to 3.3 V	0.2	1.5		mA	5
		V_O = V_{DD} – 0.5 V, V_{DD} = 4.5 V to 5.5 V	0.8	2.2		mA	5
	I_{OL2}	V_O = 1.5 V, V_{DD} = 4.5 V to 5.5 V	4.0	9.0		mA	6
	I_{OH2}	V_O = V_{DD} – 0.5 V, V_{DD} = 2.7 V to 3.3 V	0.2	2.0		mA	6
		V_O = V_{DD} – 0.5 V, V_{DD} = 4.5 V to 5.5 V	0.8	2.4		mA	6
	I_{OH3}	V_{OH} = V_{DD} – 1.0 V, V_{DD} = 4.5 V to 5.5 V	0.5			mA	7
Supply current	I_{DD}	f_{OSC} = 2.0 MHz, V_{DD} = 4.5 V to 5.5 V		1,200	2,800	µA	8
		f_{OSC} = 1.0 MHz, V_{DD} = 2.7 V to 3.3 V		300	900	µA	8
		f_{OSC} = 1.0 MHz, V_{DD} = 4.5 V to 5.5 V		600	1,400	µA	8
	I_{HLT}	f_{OSC} = 2.0 MHz, V_{DD} = 4.5 V to 5.5 V		760	1,700	µA	8
		f_{OSC} = 1.0 MHz, V_{DD} = 4.5 V to 5.5 V		400	1,000	µA	8
	I_{STOP}	V_{DD} = 2.7 V to 5.5 V			5	µA	8
	I_{VR}	A/D conversion in operation, V_{DD} = 2.7 V to 3.3 V		130	350	µA	9
		A/D conversion in operation, V_{DD} = 4.5 V to 5.5 V		220	500	µA	9
		A/D conversion in stop, V_{DD} = 2.7 V to 5.5 V			3	µA	10
A/D conversion	Resolution				10	bit	
	Differential linearity error	f_{OSC} = 1.0 MHz, T_{OPR} = 25°C, V_{DD} = VR = 5.0 V		±2.5	±4.0	LSB	
	Sequential linearity error			±3.2	±5.0	LSB	
	Total error			±4.0	±6.0	LSB	
Reference clock oscillator frequency	f_{OSC}	V_{DD} = 4.5 to 5.5 V, Rf = 33 kΩ	1.34	1.67	2.0	MHz	

NOTES:

1. Applicable pins; $P1_2$, $P1_3$, $P2_0$ - $P2_3$, $P3_0$ - $P3_3$ (digital input mode), $P4_0$ - $P4_3$, $P5_0$ - $P5_3$.
2. Applicable pins: $\overline{OSC_{IN}}$, $\overline{RESET}$, $P1_0$, $P1_1$.
3. Applicable pins: $\overline{RESET}$, $P1_0$ - $P1_3$, $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (digital input mode).
4. Applicable pins: $P3_0$ - $P3_3$ (analog input mode).
5. Applicable pins: $P0_0$ - $P0_3$ (high current mode).
6. Applicable pins: $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (output mode). (See note 11.)
7. Applicable pins: $P3_0$ - $P3_3$. (See note 12.)
8. No load (A/D conversion is stop).
9. A/D conversion in operation (operation enable).
10. A/D conversion in stop (operation disable).
11. In case of 32-pin SOP and 36-pin QFP. In case of 30-pin SDIP, $P5_2$ does not exist. In case of 28-pin SOP, $P5_0$ - $P5_3$ do not exist.
12. P3 ports are normally used for input ports with pull-up resistor. These ports can be also used.

SM5K5

V_{DD} = 5.0 V or 3.0 V, T_{OPR} = -20°C to +70°C (TYP.) unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTES
Input voltage	V_{IH1}		0.8 × V_{DD}		V_{DD}	V	1
	V_{IL1}		0		0.2 × V_{DD}	V	1
	V_{IH2}		0.9 × V_{DD}		V_{DD}	V	2
	V_{IL2}		0		0.1 × V_{DD}	V	2
Input current	I_{IL1}	V_{IN} = 0 V, V_{DD} = 2.2 V to 3.3 V	2	25	90	µA	3
		V_{IN} = 0 V, V_{DD} = 4.5 V to 5.5 V	25	70	250	µA	3
	I_{IH1}	V_{IN} = V_{DD}			2	µA	3
	I_{IL2}	V_{IN} = 0 V		1.0	10	µA	4
	I_{IH2}	V_{IN} = V_{DD}		1.0	10	µA	4
Output current	I_{OL1}	V_O = 1.0 V, V_{DD} = 2.2 V to 3.3 V	5	15		mA	5
		V_O = 1.0 V, V_{DD} = 4.5 V to 5.5 V	15	25		mA	5
	I_{OH1}	V_O = V_{DD} – 0.5 V, V_{DD} = 2.2 V to 3.3 V	0.3	1.5		mA	5
		V_O = V_{DD} – 0.5 V, V_{DD} = 4.5 V to 5.5 V	1.0	2.2		mA	5
	I_{OL2}	V_O = 0.5 V, V_{DD} = 2.2 V to 3.3 V	7	35		µA	6
		V_O = 0.5 V, V_{DD} = 4.5 V to 5.5 V	20	60		µA	6
	I_{OH2}	V_O = V_{DD} – 0.5 V, V_{DD} = 2.2 V to 3.3 V	300	2,000		µA	6
		V_O = V_{DD} – 0.5 V, V_{DD} = 4.5 V to 5.5 V	1,000	2,400		µA	6

NOTES:

1. Applicable pins; $P1_2$, $P1_3$, $P2_0$ - $P2_3$, $P3_0$ - $P3_3$ (digital input mode), $P4_0$ - $P4_3$, $P5_0$ - $P5_3$.
2. Applicable pins: $\overline{OSC_{IN}}$, $\overline{RESET}$, $P1_0$, $P1_1$.
3. Applicable pins: $\overline{RESET}$, $P1_0$ - $P1_3$, $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (digital input mode).
4. Applicable pins: $P3_0$ - $P3_3$ (analog input mode).
5. Applicable pins: $P0_0$ - $P0_3$ (high current mode).
6. Applicable pins: $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (output mode). (See note 11.)
7. Applicable pins: $P3_0$ - $P3_3$. (See note 12.)
8. No load (A/D conversion is stop).
9. A/D conversion in operation (operation enable).
10. A/D conversion in stop (operation disable).
11. In case of 32-pin SOP and 36-pin QFP. In case of 30-pin SDIP, $P5_2$ does not exist. In case of 28-pin SOP, $P5_0$ - $P5_3$ do not exist.
12. P3 ports are normally used for input ports with pull-up resistor. These ports can be also used.

SM5K5 (Cont'd)

V_{DD} = 5.0 V or 3.0 V, T_{OPR} = -20°C to + 70°C (TYP.) unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTES
Supply current	I_{DD}	f_{OSC} = 2 MHz, V_{DD} = 4.5 V to 5.5 V		1,200	2,500	µA	7
		f_{OSC} = 1 MHz, V_{DD} = 2.2 V to 3.3 V		300	800	µA	7
		f_{OSC} = 1 MHz, V_{DD} = 4.5 V to 5.5 V		600	1,200	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 2.2 V to 3.3 V		20	120	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 4.5 V to 5.5 V		40	160	µA	7
	I_{HLT}	f_{OSC} = 2 MHz, V_{DD} = 4.5 V to 5.5 V		760	1,500	µA	7
		f_{OSC} = 1 MHz, V_{DD} = 4.5 V to 5.5 V		400	900	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 2.2 V to 3.3 V		15	60	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 4.5 V to 5.5 V		20	90	µA	7
	I_{STOP}	Ceramic OSC mode, V_{DD} = 2.2 V to 3.3 V			2	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 2.2 V to 3.3 V		2	10	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 4.5 V to 5.5 V		10	25	µA	7
	I_{VR}	A/D in operation, V_{DD} = 2.2 V to 3.3 V		130	300	µA	8
		A/D in operation, V_{DD} = 4.5 V to 5.5 V		220	450	µA	8
		A/D in stop, V_{DD} = 2.2 V to 5.5 V			2	µA	9
A/D conversion	Resolution			10		bit	
	Differential linearity error	f_{OSC} = 1 MHz, T_{OPR} = 25°C, V_{DD} = VR = 5.0 V		±2.5	±4.0	LSB	
	Sequential linearity error			±3.2	±5.0	LSB	
	Total error			±4.0	±6.0	LSB	

NOTES:

1. Applicable pins; $P1_2$, $P1_3$, $P2_0$ - $P2_3$, $P3_0$ - $P3_3$ (digital input mode), $P4_0$ - $P4_3$, $P5_0$ - $P5_3$.
2. Applicable pins: $\overline{OSC_{IN}}$, $\overline{RESET}$, $P1_0$, $P1_1$.
3. Applicable pins: $\overline{RESET}$, $P1_0$ - $P1_3$, $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (digital input mode).
4. Applicable pins: $P3_0$ - $P3_3$ (analog input mode).
5. Applicable pins: $P0_0$ - $P0_3$ (high current mode).
6. Applicable pins: $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (output mode).
7. No load (A/D conversion is stop).
8. A/D conversion in operation (operation enable).
9. A/D conversion in stop (operation disable).
10. In case of 32-pin SOP and 36-pin QFP. In case of 30-pin SDIP, $P5_2$ does not exist. In case of 28-pin SOP, $P5_0$ - $P5_3$ do not exist.

SYSTEM CONFIGURATION

A Register and X Register

The A register (or accumulator A_{CC}) is a 4-bit general purpose register. The register is mainly used in conjunction with the ALU, C flag and RAM to transfer numerical value and data to perform various operations. The A register is also used to transfer data between input and output pins.

The X register (or auxiliary accumulator) is a 4-bit register and can be used as a temporary register. It loads contents of the A register or its content is transferred to the A register. When the table reference instruction PAT is used, the X and A registers load ROM data. A pair of A and X registers can accommodate 8-bit data.

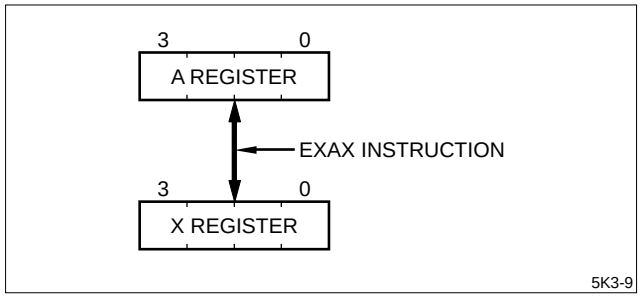


Figure 9. Data Transfer Example Between A Register and X Register

Arithmetic and Logic Unit (ALU) and Carry Signal Cy

The ALU performs 4-bit parallel operation. The ALU operates binary addition in conjunction with RAM, C flag and A register. The carry signal Cy is generated if a carry occurs during ALU operation. Some instructions use Cy. ADC instruction sets/clears the content of the C flag. ADX instruction causes the program to skip the next instruction. Note that Cy is the symbol for carry signal and not for C flag.

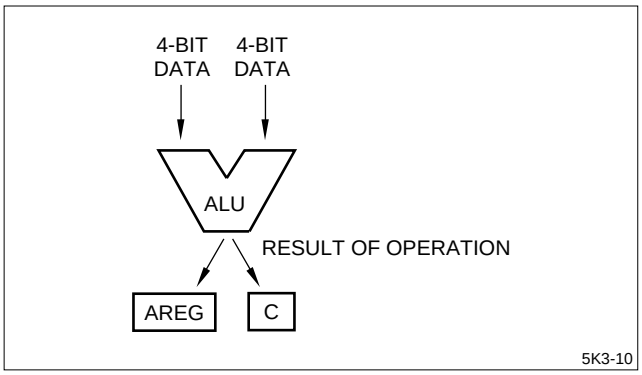


Figure 10. ALU

B Register and SB Register

B Register (B_M, B_L)

The B register is an 8-bit register that is used to specify the RAM address. The upper 4-bit section is called B_M register and lower 4-bit B_L.

SB Register

The SB register is an 8-bit register used as the save register for the B register. The contents of B register and SB register can be exchanged through EX instruction.

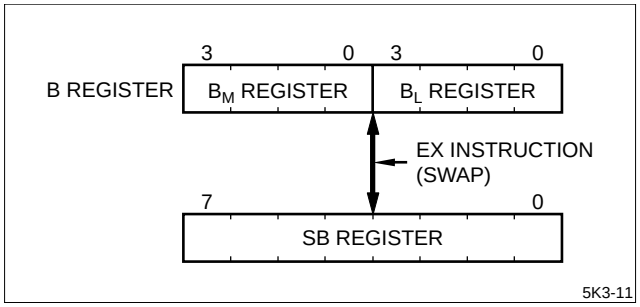


Figure 11. B Register and SB Register

Data Memory (RAM)

The data memory (RAM) is used to store data up to 4 × 16 × 8 = 512 bits.

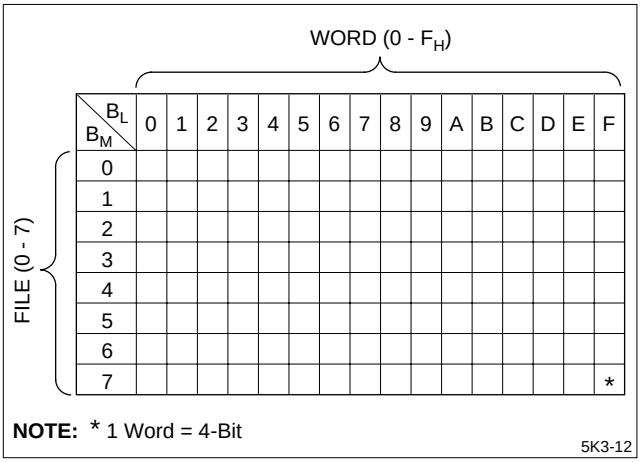


Figure 12. RAM File and Word

Program Counter PC and Stack Register SR

The program counter PC specifies the ROM address. The PC consists of 12-bit as shown in Figure 13. The upper 6-bit (P_U) represents a page while the lower 6-bit (P_L) denotes a step. The P_U section is a register and the P_L section, a binary counter.

Execution of interrupt handing and the table reference instruction PAT also automatically uses one stage of the stack register SR.

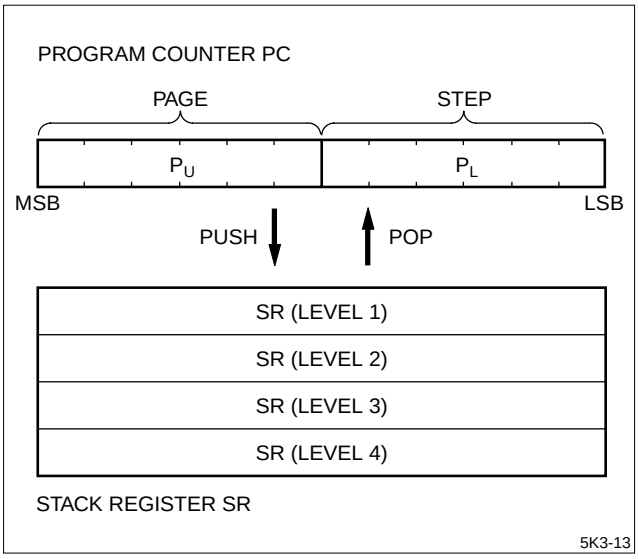


Figure 13. Program Counter PC and Stack Register SR

Program Memory (ROM)

The ROM is used to store the program. The capacity of the ROM is 2,048 step (32 page by 64 step, see Figure 14). The configuration of the ROM and program jumps are illustrated in Figure 15.

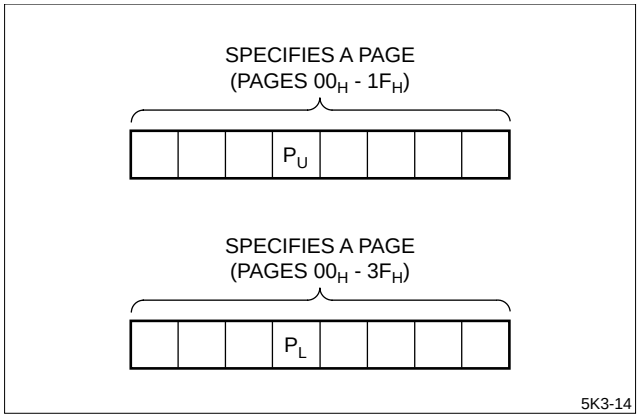
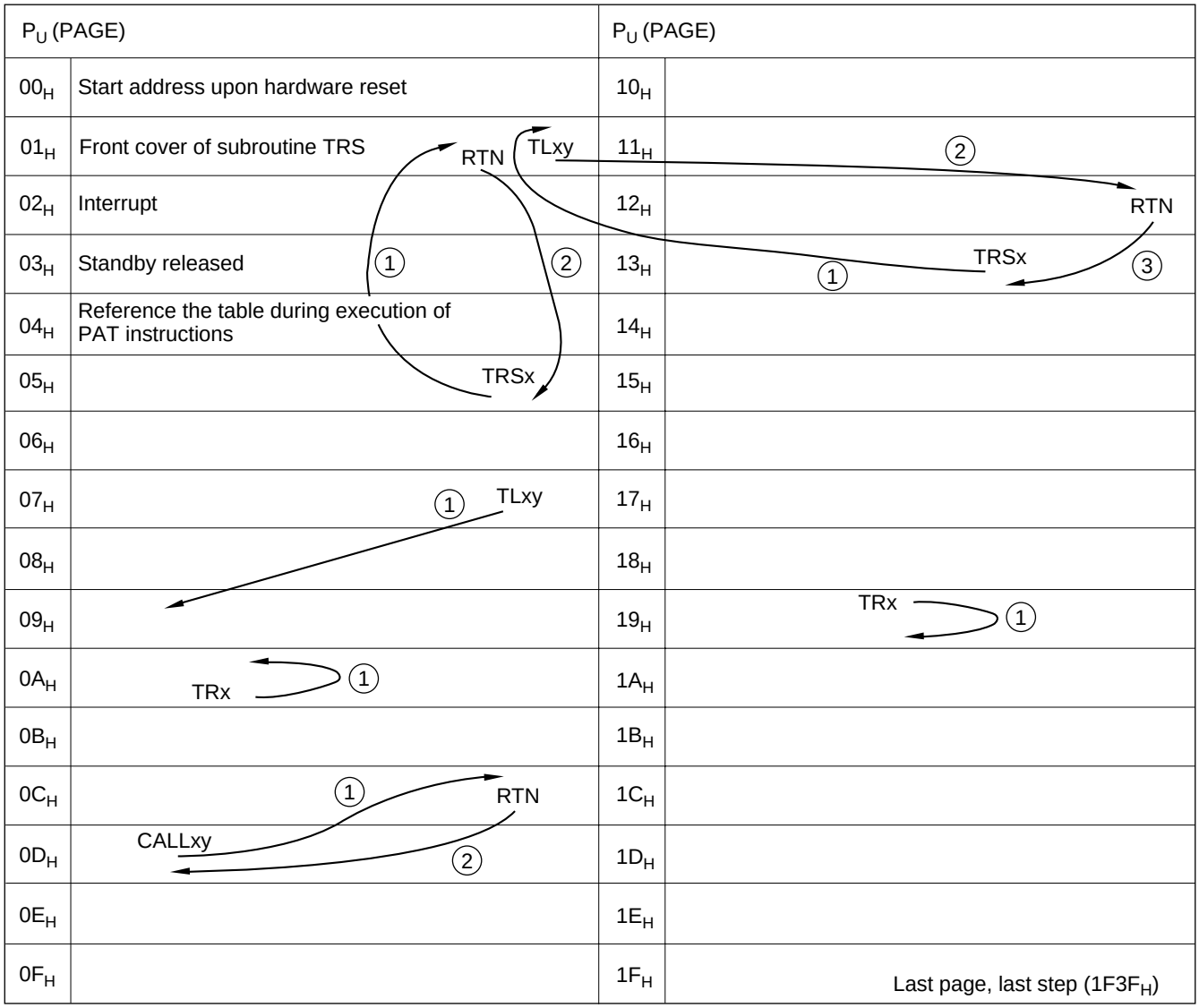


Figure 14. Page and Step for ROM



NOTE: Circled numbers are a step number in the program jump.

Figure 15. ROM Configuration and Program Jump Example

Output Latch Register and Mode Register

The SM5K3/5K4/5K5 contain six output latch registers and eight mode registers which either latch contents of output ports or control some functions of the SM5K3/5K4/5K5.

These registers, their functions and available transfer instructions are shown in Table 1.

An output latch register sets the ouput level of the pin to which it is connected.

Refer to the section of 'Mode Registers' concerning the details of the mode register.

Table 1. Output Latch Registers and Mode Registers

SYMBOL	FUNCTION	OUT	INL	OUT	IN/TPB	ANP/ORP	CONTENT OF B_L
P0	Output register	O	—	O	—	O	0
P1	Input register	—	O	—	O	—	1
P2	I/O register (independent)	—	—	O	O	O	2
P3	Input register (and analog input)	—	—	—	O	—	3
R3	Control register	—	—	O	—	—	3
P4	I/O register	—	—	O	O	O	4
P5	I/O register	—	—	O	O	O	5
R8*	A/D data/control register	—	—	O	O	—	8
R9*	A/D data register	—	—	O	O	—	9
RA*	Timer/counter register	—	—	O	O	—	A
RB*	Timer/modulo register	—	—	O	O	—	B
RC	Timer control register	—	—	O	O	—	C
RE	Interrupt mask register	—	—	O	O	—	E
RF	P2 directional register	—	—	O	O	—	F

NOTES:
1. *8-bit register.
2. Bit 4 (R84) in the R8 register is read only. Read or write operation of this bit does not affect any other operation.

FUNCTION DESCRIPTION

Hardware Reset Function

Reset function initializes the SM5K3/5K4/5K5 systems. When the input on the $\overline{\text{RESET}}$ pin goes LOW, the system enters reset condition after two command cycles. After the $\overline{\text{RESET}}$ pin goes HIGH level, the reset condition is removed as the input pulse from OSC_{IN} pin repeats 2^{15} times, forcing the program counter to start at 0 page and 0 address. Initialized status of the system immediately after resetting is shown below.

Reset causes the following changes:

1. I/O pins are set input.
2. All mode registers are reset.
3. Output latch register P0 is reset, causing $\overline{P0}_0$ to $\overline{P0}_3$ pins go HIGH level.
4. Interrupt request flags (IFA, IFB, and IFT), interrupt master enable flag (IME) are reset, disabling all interrupts.

Table 2. Status of Flags and Registers Immediately After Reset

FLAG REGISTER	STATUS
PC	0
SP	Level 1
RAM	Undefined
Register A	Undefined
Register X	Undefined
P0, P2, P4, P5 output latch register	0
Timers (RA, RB), divider	0
IFA flag	0
IFB flag	0
IFT flag	0
IME flag	0
C flag	Undefined
B_M, B_L, registers, SB register	Undefined
R3, R8*, R9, RC, RE, RF	0

NOTE: * The content of the bit R84 is undefined because it is read only.

Standby Feature

The standby function saves power by stopping the program whenever it is not necessary to run. The mode in which the microcomputer is executing the program is called the run mode and the mode in which it stops the program is called the standby mode. Standby mode is further divided into two modes: stop mode and halt mode, one of which is selected by halt instruction or stop instruction. Upon removal of standby condition, the SM5K3/5K4/5K5 return from the standby mode to the normal run mode. To enter the standby mode, select either stop mode or halt mode whichever is appropriate (see Figure 16).

BLOCKS STOPPED DURING STANDBY MODE

In the Halt Mode

The system clock generating circuit stops during the halt mode, deactivating all the blocks driven by the system clock. The main clock and dividers remain active. This means that timers can be used while in the halt mode. Both internal and external clocks can be used as the count clock.

In the Stop Mode

The main clock and system clock stop upon entering the stop mode. Therefore, only timers using the external clock remain active.

COUNTERS THAT THE SYSTEM RETAINS DURING STANDBY MODE

The contents that will be retained in the halt mode will also be retained in the stop mode. These items are shown in Table 3.

USAGE OF HALT MODE AND STOP MODE

The system returns back to the normal operation mode upon occurring of a standby mode releasing condition. The halt mode should be used when the system must enter and exit normal operation frequently as in the case of key operation.

The halt mode should also be used to keep timers that are operating from the internal clock, while in the standby mode.

The stop mode further saves more power than the halt mode but requires longer time to return to the normal mode. Therefore, the stop mode should be used when the system will not be required to return to the normal mode in a short time.

Table 3. System Contents Secured During Standby Mode

FLAG	REGISTER	OUTPUT LATCH REGISTER/ MODE REGISTER	OTHER
IFA flag IFB flag IFT flag IME flag C flag	A register X register B_M, B_L register SP SR	P0, P2, R3, P5 R8, R9, RA, RB RC, RE, RF	RAM

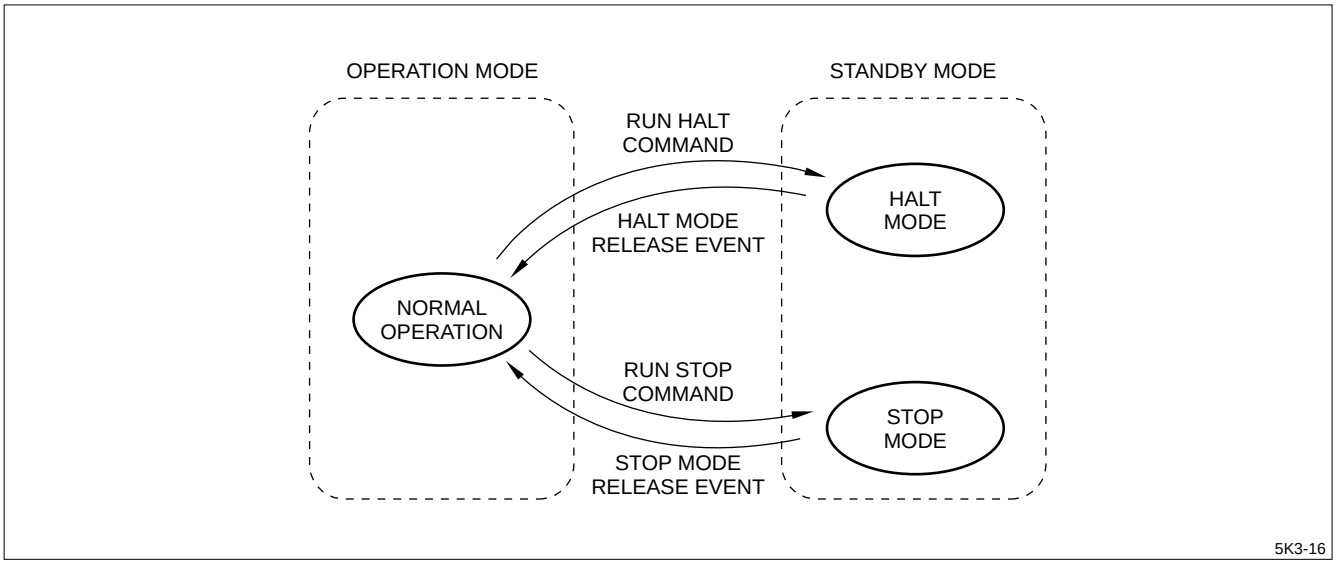


Figure 16. Operation Shift of Program

Table 4. Releasing Events of Standby Mode (6-Type)

RELEASING EVENT	FLAG	INT/EXT	MASKABLE/ NONMASKABLE	PRIORITY
Reset input	—	External	Nonmaskable	—
Low level input on $P1_0$ pin	IFA	External	Maskable	1
Low level input on $P1_1$ pin	IFB	External	Maskable	2
Low level input on $P1_2$ pin	—	External	Nonmaskable	—
Low level input on $P1_3$ pin	—	External	Nonmaskable	—
Timer overflow	IFT	Internal	Maskable	3

Interrupt Feature

The interrupt block consists of mask flags (bit RE0, RE1 and RE2), IME flag and interrupt request handling circuit. Figure 17 shows the configuration of the interrupt block.

Interrupt Used with SM5K3/5K4/5K5

Interrupt event occurs on the falling edge of $P1_0$ or $P1_1$ pin input, or the overflow at the timer. These events set flags IFA, IFB and IFT respectively, that then serve as interrupt request flag.

Table 5 shows interrupt handling priority level and jump address.

IME Flag (Master Enable Flag)

The IME enables or disables all interrupts at the same time. The IE command, when executed, sets the IME flag and enables the interrupt specified by the mask flag setting. The ID command resets the IME flag, disabling process of any interrupt request. Setting the IME flag to reset after releasing hardware reset, all interrupts are inhibited.

Mode Register RE (Interrupt Mask Flag)

The mode register RE (RE0, RE1 and RE2, interrupt mask flag) individually enables or disables three types of interrupts.

Table 5. Interrupt Event Summary

INTERRUPT EVENT (REQUEST FLAG)	JUMP ADDRESS		PRIORITY ORDER	INTERRUPT MASK FLAG
	PAGE	STEP		
Falling edge of input on $P1_0$ (IFA)	2	0	1	RE0
Falling edge of input on $P1_1$ (IFB)	2	2	2	RE1
Timer overflow (IFT)	2	4	3	RE2

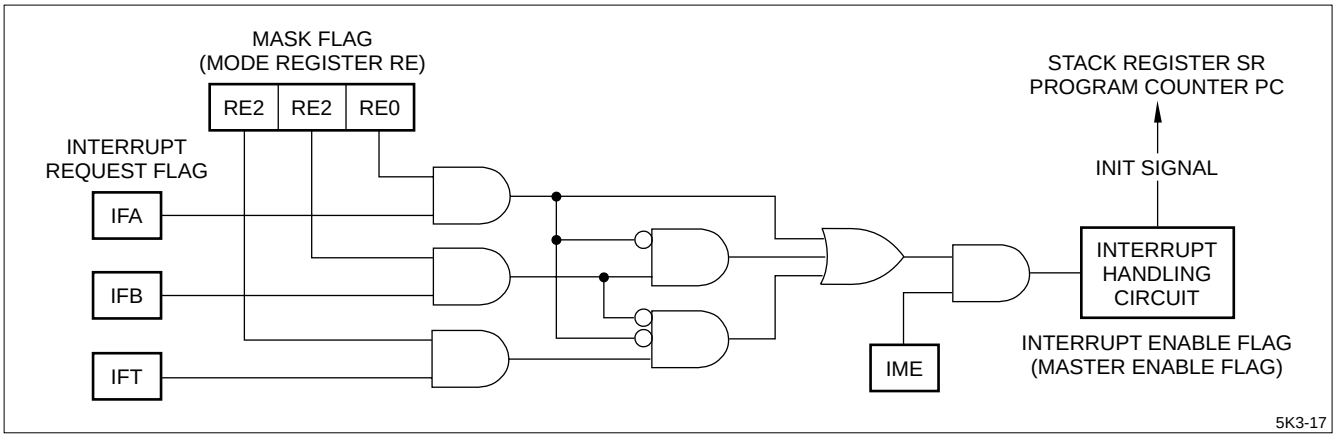


Figure 17. Interrupt Block Diagram

Timer/Counter

The SM5K3/5K4/5K5 have a pair of built-in timer/counter. The timer/counter is used to handle periodic interrupts and to count. The overflowing timer can be used to disable the halt mode. The timer/counter serve as interval timer.

The timer/counter consists of an 8-bit count register RA, modulo register RB (for counter initial value setting), 15-bit divider and 4-bit mode register RC (for count clock selection). The configuration of the timer/counter is shown in Figure 18.

Selecting Count Clock

A count clock is selected by the bit settings in the mode register RC.

Table 6. Count Clock Selection

LOWER 2-BIT OF RC BITS		SELECTED COUNT CLOCK
1	**0**	
0	0	f_{SYS} (system clock)
0	1	$f_{SYS}/2^7$
1	0	$f_{SYS}/2^{15}$
1	1	External event clock ($P1_1$)

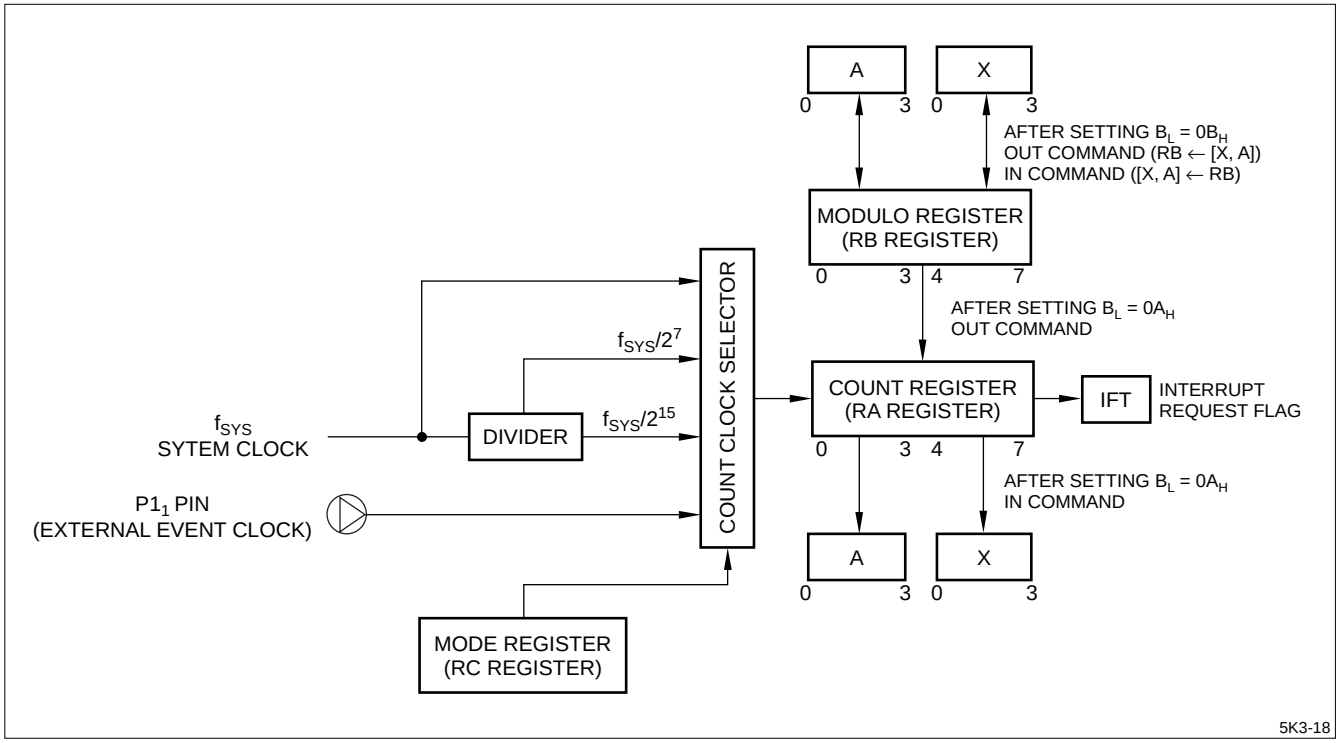


Figure 18. Configuration of Timer/Counter

A/D Conversion

The SM5K3/5K4/5K5 are provided with a built-in 10-bit A/D converter having 4 channel multiplexer analog inputs. The A/D converter operates in A/D conversion mode and comparison mode. In the A/D conversion mode, the converter converts the analog input from the P3 pin to the digital value; and in the comparison mode, it compares the input analog amplitude with that of a reference voltage set inside the SM5K3/5K4/5K5. The $P3_0$ to $P3_3$ pins can be used as analog voltage inputs. One or more of these four inputs can be set to assume A/D pin by the bit operation of the mode register R3. One of these A/D pins is further set as analog input by the bit operation of the mode register R8. The A/D converter is controlled by the bits set in the mode register R8. For details of the mode register R8, refer to 'Mode Registers R8'. Configuration of the A/D converter is illustrated in Figure 19.

CAUTION

Keep the A/D converter reference voltage on the VR pin equal to or below V_{DD}.

Do not apply the voltage to the VR pin before V_{DD} is applied.

Connect AGND to GND.

A/D CONVERSION MODE

In the A/D conversion mode, the converter converts the analog input voltage to the digital value. The analog input voltage is successively compared with the internal voltage charged on the weighted capacitor array until its digital equivalent is determined. The resultant digital data is stored into the mode registers R8 and R9.

The conversion requires 152.5 µs (main clock at 400 kHz/system clock at 5 µs) or 1.86 ms (main clock at 32.768 kHz/system clock at 61 µs).

COMPARISON MODE

In the comparison mode, the analog voltage from one of $P3_0$ to $P3_3$ pins is compared, in amplitude, with internally generated voltage whose value is set by the mode registers R8 and R9. The result data of the comparison is saved into the bit 4 (bit R84) position of the mode register R8. The comparison cycle lasts 62.5 µs (main clock at 400 kHz, system clock at 5 µs) or 763 µs (main clock at 32.768 kHz/system clock at 61 µs).

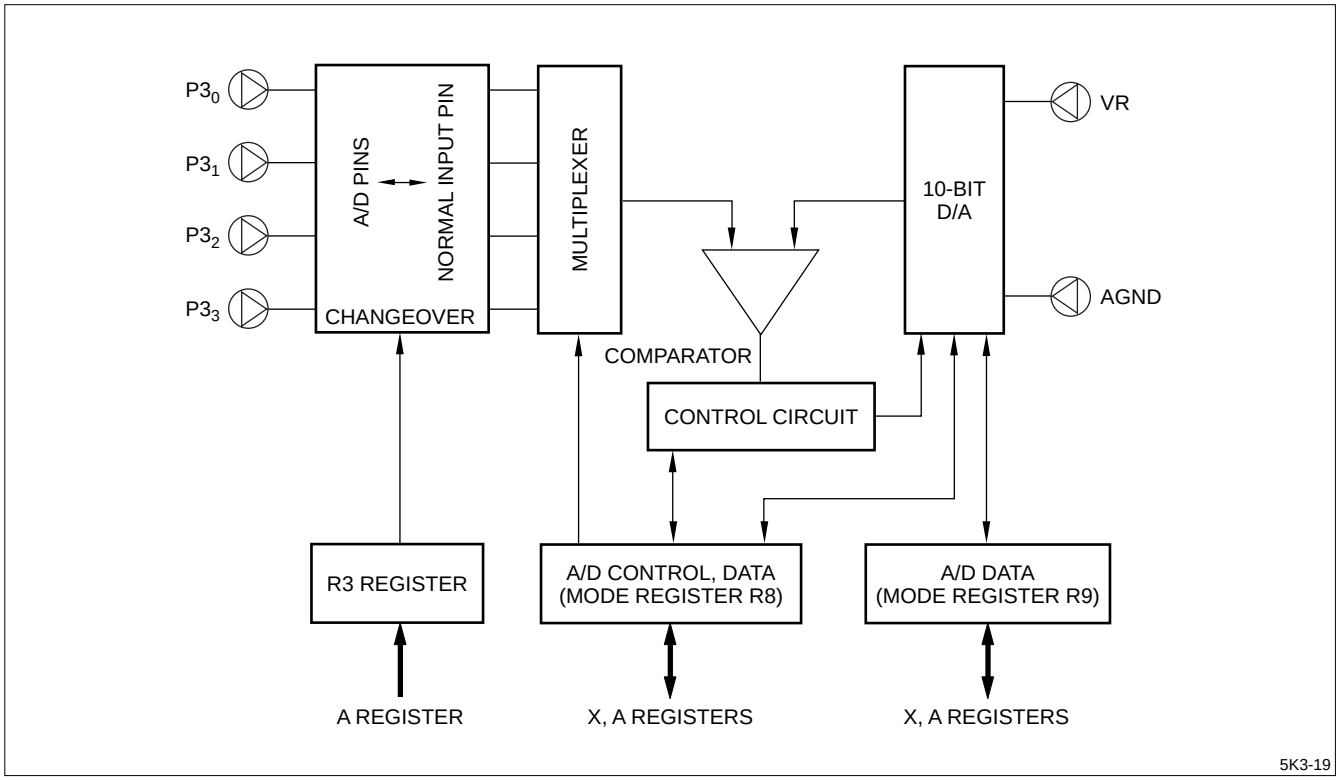


Figure 19. A/D Converter Block Diagram

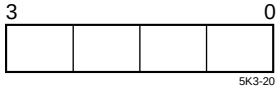
MODE REGISTERS

The registers which control functions of the SM5K3/5K4/5K5 and which serve as counter/timer are commonly referred to as 'mode registers'. In the SM5K3/5K4/5K5, R8 to RB are 8-bit mode registers, and R3, RC, RE and RF are 4-bit mode registers.

To set data into the mode registers, the OUT command is used, and to check the contents of the mode registers IN command is used.

R3 (A/D Pin Selection Register)

Any pin on 4-pin port P3 can be set to accommodate analog voltage (hereafter called A/D pin).



Bit i (i = 3 to 0)

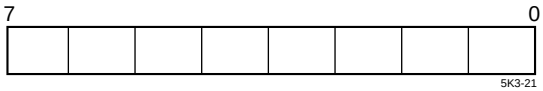
Sets P3i pin to either general purpose input or A/D pin.

BIT	CONTENT
0	(General purpose) input
1	A/D input

NOTE: * Select one pin which is to be selected by mode register R8.

R8 (A/D Conversion Control and A/D Data Register)

An 8-bit register used to control A/D conversion and storing part of A/D conversion result. It also stores the results of comparison.



Bits 7 to 6

Storage of A/D conversion result (A/D conversion mode) and setting of internal voltage (comparison mode).

- Use as part of a 10-bit data register in combination with mode register R9.
- Bit R86 is the LSB.
- Store lower 2-bit of converted data in A/D conversion mode.
- Use as lower 2-bit of internal voltage setting data in comparison mode.

Bit 5: A/D Operation Enable/Disable Flag*

BIT	CONTENT
0	Disable (A/D power source off)
1	Enable (A/D power source on)

NOTE: * When operation is end, these bits are cleared.

Bit 4: Storages of comparison result (read only)

BIT	CONTENT
0	P3i pin voltage < internal setting voltage
1	P3i pin voltage, internal setting voltage

NOTE: (i = 3 to 0)

Bit 3: S/R flag (start/clear)*

BIT	CONTENT
0	End of operation (or stop)
1	Start of operation (or in operation)

NOTE: * When operation is end, these bits are cleared.

Bit 2: Operation mode selection

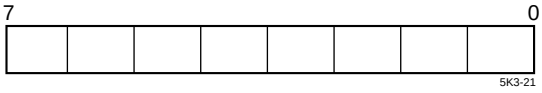
BIT	CONTENT
0	A/D conversion
1	Comparison

Bits 1 to 0: Select one of A/D pins as A/D conversion

BIT	CONTENT
00	$P3_0$
01	$P3_1$
10	$P3_2$
11	$P3_3$

R9 (A/D Data Register)

The register to store the upper 8-bit of 10-bit data resulting from A/D conversion.

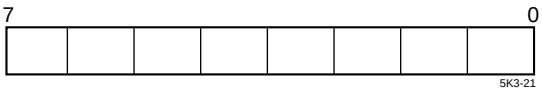


Bit i (i = 7 to 0)

Storages of A/D conversion result (A/D conversion mode) and setting of internal voltage (comparison mode).

- Uses as part of a 10-bit data register in combination with mode register R8.
- Bit R97 is the MSB.
- Stores upper 8-bit of A/D conversion result.
- Uses as upper 8-bit of internal voltage setting data in comparison mode.

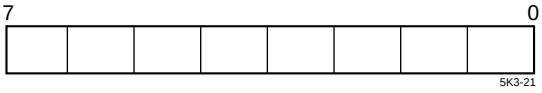
RA (Count Register)



Bit i (i = 7 to 0): Count clock input register

- Uses as counter part of timer/counter (count clock input).
- Loads the content of RB to RA when the RA overflows or when OUT command ($B_L = 0A_H$) is executed.
  RA ← RB
- Loads the content of RA to X and A registers upon execution of IN command ($B_L = 0A_H$).
  (X, A) ← RA
- Bit 7 = MSB, bit 0 = LSB

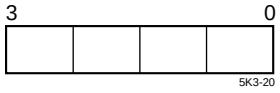
RB (Modulo Register)



Bit i (i = 7 to 0): Count initial value storage register

- Uses as modulo register of timer/counter
- Loads the content of RB to X and A registers upon execution of IN command ($B_L = 0B_H$). X = upper bits, A = lower bits.
  (X, A) ← RB
- Loads the contents of X and A registers to RB upon execution of OUT command ($B_L = 0B_H$). X = upper bits, A = lower bits.
  RB ← (X, A)
- Bit 7 = MSB, Bit 0 = LSB

RC (Timer Control)



Bit 3: Starts up count of the timer

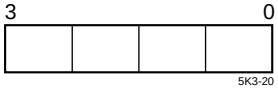
BIT	CONTENT
0	Stop
1	Start

Bit 2: Unused

Bits 1 to 0: Select the source clock to the timer

BIT	CONTENT
00	f_{SYS} (system clock)
01	$f_{SYS}/2^7$
10	$f_{SYS}/2^{15}$
11	Falling edge input on $P1_1$ pin

RE (Interrupt Mask Flag)



Bit 3: Unused

Bit 2: Removes overflow interrupt from timer or standby condition

BIT	CONTENT
0	Disable
1	Enable

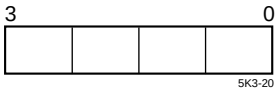
Bit 1: Interrupts on the falling edge of input from $P1_1$ pin, or releases of standby mode by the LOW input from $P1_1$ pin

BIT	CONTENT
0	Disable
1	Enable

Bit 0: Interrupts on the falling edge of input on $P1_0$ pin, or releases of standby mode by the LOW input from $P1_0$ pin

BIT	CONTENT
0	Disable
1	Enable

RF (P2 Port Direction Register)



Bit i (i = 3 to 0): Selection of input pin/output pin

BIT	CONTENT
0	Set P2i pin to input
1	Set P2i pin to output

I/O Ports

The SM5K3/5K4/5K5 have 24 ports; eight input, four output and 12 I/O ports. To verify the input, use suitable instruction to transfer the input on the pin directly to the A register. To select the output latch register to which the content of the A register is to be transferred, and to select the input port from which the signal or data is to be transferred to the A register, use the B_L register. For details of B_L settings and associated ports, refer to Table 1.

Port $P0_0$ to $P0_3$ (CMOS Inverting Output Port)

The data transfers in 4-bit string (use OUT or OUTL instruction) or in unit of 1-bit (use ANP or ORP instruction).

Port $P1_0$ to $P1_3$ (Input Port with Pull-up Resistor)

The data transfers in unit of 4-bit. This port can be used as standby/external interrupt input or count pulse input. The P1 port can also be used as a standby release port without requiring specific setting on $P1_2$ and $P1_3$ pins. Pins $P1_0$ and $P1_1$ require settings through the mode resistor RE. When using the P1 port as an external interrupt input, use pins $P1_0$ and $P1_1$ with suitable settings in the mode register RE. When using the P1 port as the count pulse input, use $P1_1$ pin.

Port 2_0 to $P2_3$ (I/O Port with Pull-up Resistor)

Each bit can independently set its direction and can be transferred independently or in combination with other 3-bit. The direction of the bits is determined by the RF register. After reset, the P2 port is set input.

Port $P3_0$ to $P3_3$ (Input Port with Pull-up Resistor)

The data transfers in unit of 4-bit. The port can also be used as A/D analog voltage input. To use the P3 port as the A/D port, set the mode register R3.

Port $P4_0$ to $P4_3$ (I/O port with Pull-up Resistor)

The data transfers in units of 4-bit. When set output, content of each bit can be set. Executing the input instruction (IN) sets the P4 ports ($P4_0$ to $P4_3$) to input; and executing output instruction (OUT, ANP or ORP) sets the port to output. After reset, the P4 port is set input.

Port $P5_0$ to $P5_3$ (I/O port with Pull-up Resistor)

The data transfers in units of 4-bit. When set output, content of each bit can be set. Executing the input instruction (IN) sets the P5 ports ($P5_0$ to $P5_3$) to input; and executing output instruction (OUT, ANP or ORP) sets the port to output. After reset, the P5 port is set input.

Flags

The SM5K3/5K4/5K5 have four flags (C flag and IFA, IFB, IFT interrupt request flags), which are used to perform settings and judgements.

System Clock Generator and Dividers

System Clock Generator

The system clock is the divided-by-two main clock applied through OSC_{IN} and OSC_{OUT} (see Figure 20). The system clock generator is shown in Figure 21.

One system clock cycle period is equal to one instruction execution time when the instruction consists of one word. When the ceramic oscillator runs at 400 kHz, the system clock f_{SYS} is 200 kHz. This means that the instruction execution time is 5 µs/word. Using a 32.768 kHz crystal oscillator generates 16.384 kHz f_{SYS} and the instruction execution time is 61 µs/word. The system clock can be used as count input pulse to the timer.

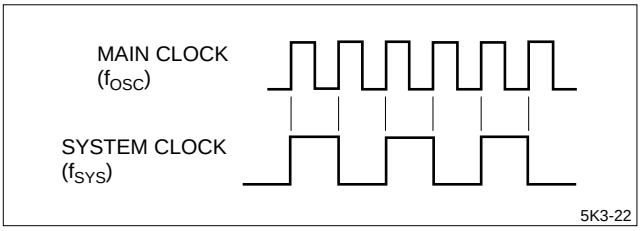


Figure 20. Main Clock and System Clock

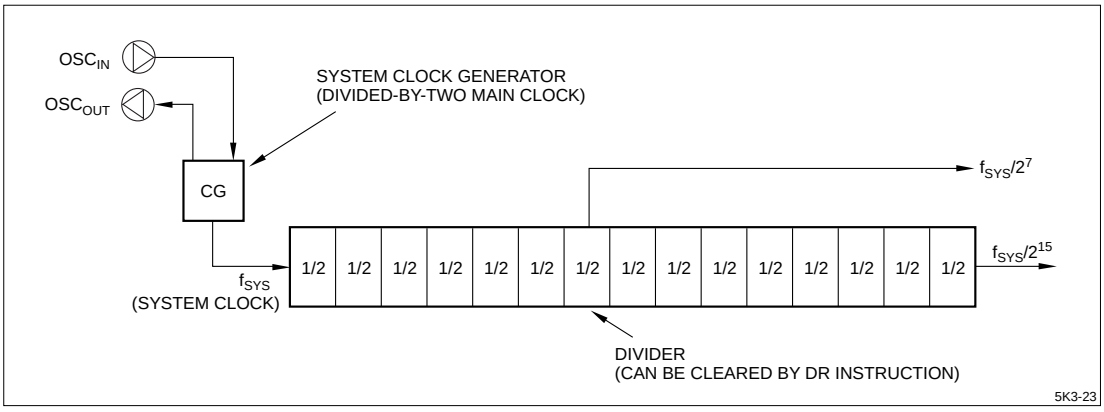


Figure 21. System Clock Generator and Divider

Divider

The divider consists of 15 divided-by-two dividers, providing two ($f_{SYS}/2^7$, $f_{SYS}/2^{15}$) of four count clocks that are fed to the counter RA from the system clock. Its configuration is shown in Figure 21. The divider can be cleared by using the DR instruction.

Oscillator Mask Option

Selection of type of oscillator, ceramic or crystal, is made by mask option.

INSTRUCTION SET

Definition of Symbols

SYMBOL	DEFINITION
M	Content of RAM at the address defined by the B register
←	Transfer direction
∪	Logical OR
∩	Logical AND
⊕	Exclusive OR
Ai	An i bit of A register (i = 3 to 0)
Push	Saves the contents of PC to stack register SR
Pop	Returns the contents saved in the stack register back to PC
Pj	Indicates output latch register or input register, Pj (j = 0 to 5)
Rj	Mode register. Rj register (j = 3, A, B, C, E, F)
ROM ( )	Content stored in ROM location defined by the value in ( ).
CY	Carry in ALU (independent of C flag). The CY (carry) is a signal which is generated when the ALU has been carried by the execution of a command. It is different from the C flag.
X	Used to represent a group of bits in the content of a register or memory. For example, the X in the LDAX instruction denotes the lower two digits (I_1 and I_0) of A register.

- A bit in a register is affixed to the register symbol, e.g. a bit (i = 0, 1, 2, 3 …) of X register is expressing as Si and P (R) register as P (R) i.
- Increment means binary addition of 1_H and decrement addition of F_H.
- Skipping an instruction means to ignore that instruction and to do nothing until starting the next instruction. In this sense, an instruction to be skipped is treated as a NOP instruction. Skipping 1-byte instruction requires one cycle and 2 byte instruction two cycle. Skipping 1-byte, 2-cycle instruction requires one cycle.

ROM Address Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
TR x	80 to BF	$P_L \leftarrow x\ (I_5 - I_0)$
TL xy	E0 to E4 00 to FF	$P_U \leftarrow x\ (I_{11} - I_6)$ $P_L \leftarrow y\ (I_5 - I_0)$
TRS x	C0 to DF	Push $P_U \leftarrow 01_H$, $P_L \leftarrow x\ (I_4, I_3, I_2, I_1, I_0)$
CALL xy	F0 to F7 00 to FF	Push $P_U \leftarrow x\ (I_{11} - I_6)$ $P_L \leftarrow y\ (I_5 - I_0)$
RTN	7D	Pop
RTNS	7E	Pop, skip the next step
RTNI	7F	Pop, IME ← 1

Data Load Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
LAX x	10 to 1F	$A \leftarrow x\ (I_3 - I_0)$
LBMX x	30 to 3F	$B_M \leftarrow x\ (I_3 - I_0)$
LBLX x	20 to 2F	$B_L \leftarrow x\ (I_3 - I_0)$
LDA x	50 to 53	$A \leftarrow M$, $B_{Mi} \leftarrow B_{Mi} \oplus \times\ (I_1 - I_0)$ (i = 1, 0)
EXC x	54 to 57	$M \leftrightarrow A$, $B_{Mi} \leftarrow B_{Mi} \oplus \times\ (I_1 - I_0)$ (i = 1, 0)
EXCI x	58 to 5B	$M \leftrightarrow A$, $B_L \leftarrow B_L + 1$ $B_{Mi} \leftarrow B_{Mi} \oplus \times\ (I_1$ to $I_0)$ (i = 1, 0) Skip the next step, if result of $B_L = 0$
EXCD x	5C to 5F	$M \leftrightarrow A$, $B_L \leftarrow B_L - 1$ $B_{Mi} \leftarrow B_{Mi} \oplus \times\ (I_1$ to $I_0)$ (i = 1, 0) Skip the next step, if result of $B_L = F_H$
EXAX	64	$A \leftrightarrow$ X-reg
ATX	65	X-reg ← A
EXBM	66	$B_M \leftrightarrow A$
EXBL	67	$B_L \leftrightarrow A$
EX	68	$B \leftrightarrow SB$

Arithmetic Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
ADX x	00 to 0F	$A \leftarrow A + x\ (I_3 - I_0)$, Skip the next step, if Cy = 1
ADD	7A	$A \leftarrow A + M$
ADC	7B	$A \leftarrow A + M + C$, C ← Cy Skip the next step, if Cy = 1
COMA	79	$A \leftarrow \overline{A}$
INCB	78	$B_L \leftarrow B_L + 1$,Skip the next step, if result of $B_L = 0$
DECB	7C	$B_L \leftarrow B_L - 1$,Skip the next step, if result of $B_L = F_H$

Test Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
TAM	6F	Skip the next step, if A = M
TC	6E	Skip the next step, if C = 1
TM x	48 to 4B	Skip the next step, if Mi = 1 (i = 3 to 0)
TABL	6B	Skip the next step, if A = B_L
TPB x	4C to 4F	Skip the next step, if P (R) i = 1, (i = I_1, I_0)
TA	6C	Skip the next step, if IFA = 1, IFA ← 0
TB	6D	Skip the next step, if IFB = 1, IFB ← 0
TT	69 02	Skip the next step, if IFT = 1, IFT ← 0

Bit Operation Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
SM x	44 to 47	Mi ← 1 (i = 3 to 0)
RM x	40 to 43	Mi ← 0 (i = 3 to 0)
SC	61	C ← 1
RC	60	C ← 0
IE	63	IME ← 1 (Interrupt enable)
ID	62	IME ← 0 (Interrupt disable)

I/O Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
INL	70	A ← P1
OUTL	71	P0 ← A
ANP	72	Pj ← Pj ∩ A (j = 0, 2, 4, 5)
ORP	73	Pj ← Pj ∪ A (j = 0, 2, 4, 5)
IN	74	A ← Pj (j = 1 to 5), X-reg, A ← Rj (j = 8, 9, A, B), A ← Rj (j = C, E, F)
OUT	75	Pj ← A (j = 0, 2, 4, 5), Rj ← X-reg, A (j = 8, 9, B) RA ← RB Rj ← A (j = 3, C, E, F)

Table Search Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
PAT	6A	Push P_U ← 04_H, P_L ← (X_1, X_0, A) X-reg ← ROM_H, A ← ROM_L Pop

Divider Operation Instruction

MNE-MONIC	MACHINE CODE	OPERATIONS
DR	69 03	Divider (f_0 - f_{15}) clear

Special Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
STOP	76	Standby mode (STOP)
HALT	77	Standby mode (HALT)
NOP	00	No operation

SYSTEM CONFIGURATION EXAMPLE

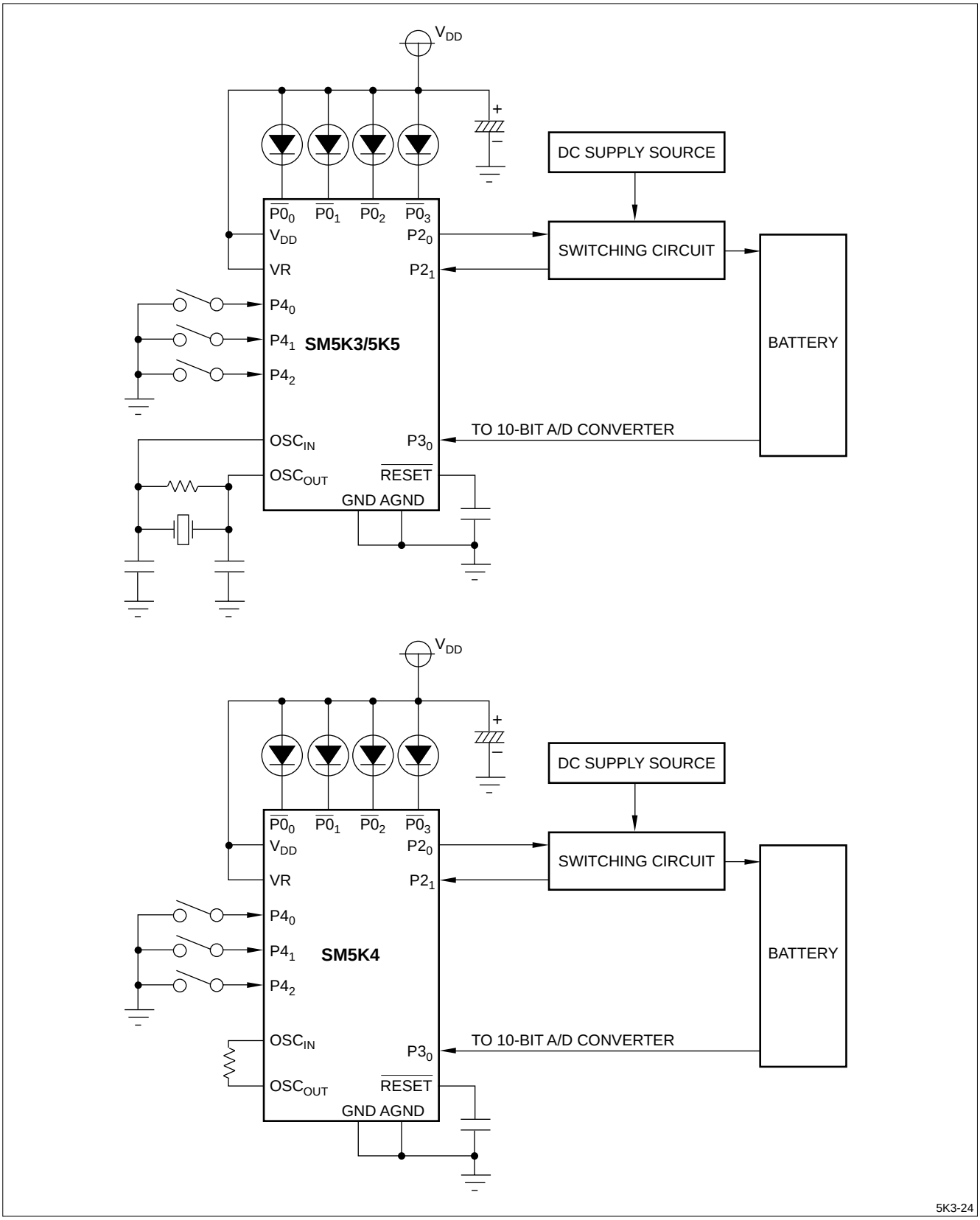


Figure 22. Example of a Charger Controller

LIFE SUPPORT POLICY

SHARP components should not be used in medical devices with life support functions or in safety equipment (or similiar applications where component failure would result in loss of life or physical harm) without the written approval of an officer of the SHARP Corporation.

LIMITED WARRANTY

SHARP warrants to its Customer that the Products will be free from defects in material and workmanship under normal use and service for a period of one year from the date of invoice. Customer's exclusive remedy for breach of this warranty is that SHARP will either (i) repair or replace, at its option, any Product which fails during the warranty period because of such defect (if Customer promptly reported the failure to SHARP in writing) or, (ii) if SHARP is unable to repair or replace, refund the purchase price of the Product upon its return to SHARP. This warranty does not apply to any Product which has been subjected to misuse, abnormal service or handling, or which has been altered or modified in design or construction, or which has been serviced or repaired by anyone other than Sharp. The warranties set forth herein are in lieu of, and exclusive of, all other warranties, express or implied. ALL EXPRESS AND IMPLIED WARRANTIES, INCLUDING THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR USE AND FITNESS FOR A PARTICULAR PURPOSE, ARE SPECIFICALLY EXCLUDED. In no event will Sharp be liable, or in any way responsible, for any incidental or consequential economic or property damage.

The above warranty is also extended to Customers of Sharp authorized distributors with the following exception: reports of failures of Products during the warranty period and return of Products that were purchased from an authorized distributor must be made through the distributor. In case Sharp is unable to repair or replace such Products, refunds will be issued to the distributor in the amount of distributor cost.

SHARP reserves the right to make changes in specifications at any time and without notice. SHARP does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied.

SHARP®

NORTH AMERICA

SHARP Microelectronics
of the Americas
5700 NW Pacific Rim Blvd., M/S 20
Camas, WA 98607, U.S.A.
Phone: (360) 834-2500
Telex: 49608472 (SHARPCAM)
Facsimile: (360) 834-8903
http://www.sharpsma.com

EUROPE

SHARP Electronics (Europe) GmbH
Microelectronics Division
Sonninstraße 3
20097 Hamburg, Germany
Phone: (49) 40 2376-2286
Telex: 2161867 (HEEG D)
Facsimile: (49) 40 2376-2232

ASIA

SHARP Corporation
Integrated Circuits Group
2613-1 Ichinomoto-Cho
Tenri-City, Nara, 632, Japan
Phone: (07436) 5-1321
Telex: LABOMETA-B J63428
Facsimile: (07436) 5-1532

Reference Code SMT98159