

128M X 64 Bits (1GB) 200-Pin DDR SDRAM SO-DIMM (PC1600/PC2100)

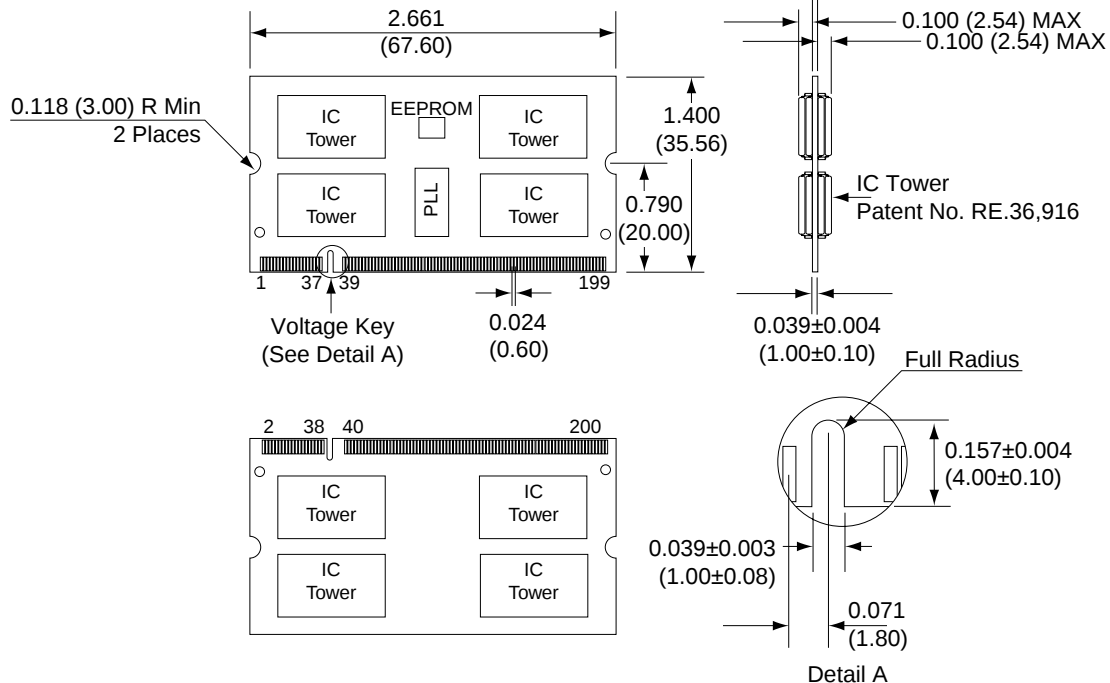
FEATURES

- PC1600/PC2100 Compliant
(PC266A 133MHz—7.5ns@CL=2)
(PC266B 133MHz—7.5ns@CL=2.5)
(PC200 100MHz—10ns@CL=2)
- 200-Pin SO-DIMM form factor
- SimpleTech Patented IC Tower stacking technology
- Auto and self refresh capability
(8192 cycles/64ms refresh)
- SSTL_2 compatible inputs and outputs
- +2.5V $\pm$ 0.2V VDD
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0 and /CK0), and bi-directional data strobe (DQS)
- Four internal banks for concurrent operation
- Auto Precharge option for each burst access
- Burst lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect with EEPROM

PACKAGE DIMENSIONS

Module Dimensions

Units are in inches (millimeters). Tolerances are ± 0.005 (± 0.127) unless otherwise specified.



Left Key Position:
VDD=VDDO=2.5V

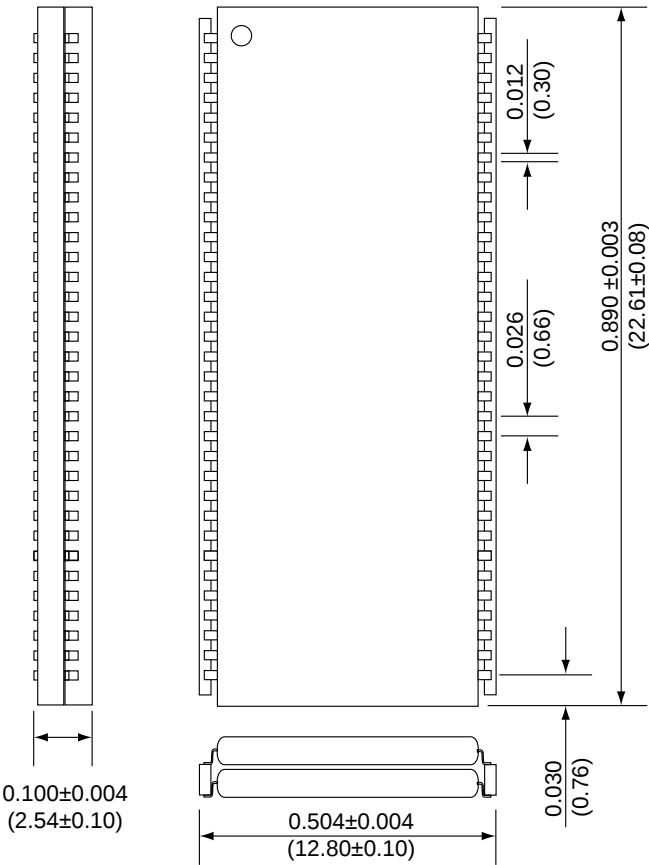
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(continued)

PACKAGE DIMENSIONS (continued)

IC Tower Dimensions

Units are in inches (millimeters). Tolerances are ± 0.005 (± 0.127) unless otherwise specified.



PIN CONFIGURATION (*=Not Used; /=Active Low)**Pinout**

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	2	VREF	51	VSS	52	VSS	101	A ₉	102	A ₈	151	DQ ₄₂	152	DQ ₄₆
3	VSS	4	VSS	53	DQ ₁₉	54	DQ ₂₃	103	VSS	104	VSS	153	DQ ₄₃	154	DQ ₄₇
5	DQ ₀	6	DQ ₄	55	DQ ₂₄	56	DQ ₂₈	105	A ₇	106	A ₆	155	VDD	156	VDD
7	DQ ₁	8	DQ ₅	57	VDD	58	VDD	107	A ₅	108	A ₄	157	VDD	158	/CK ₁ *
9	VDD	10	VDD	59	DQ ₂₅	60	DQ ₂₉	109	A ₃	110	A ₂	159	VSS	160	CK ₁ *
11	DQS ₀	12	DM ₀ \DQS ₉	61	DQS ₃	62	DM ₃ \DQS ₁₂	111	A ₁	112	A ₀	161	VSS	162	VSS
13	DQ ₂	14	DQ ₆	63	VSS	64	VSS	113	VDD	114	VDD	163	DQ ₄₈	164	DQ ₅₂
15	VSS	16	VSS	65	DQ ₂₆	66	DQ ₃₀	115	A ₁₀ \AP	116	BA ₁	165	DQ ₄₉	166	DQ ₅₃
17	DQ ₃	18	DQ ₇	67	DQ ₂₇	68	DQ ₃₁	117	BA ₀	118	/RAS	167	VDD	168	VDD
19	DQ ₈	20	DQ ₁₂	69	VDD	70	VDD	119	/WE	120	/CAS	169	DQS ₆	170	DM ₆ \DQS ₁₅
21	VDD	22	VDD	71	CB ₀ *	72	CB ₄ *	121	/S ₀	122	/S ₁	171	DQ ₅₀	172	DQ ₅₄
23	DQ ₉	24	DQ ₁₃	73	CB ₁ *	74	CB ₅ *	123	DU(A ₁₃)*	124	DU(BA ₂)*	173	VSS	174	VSS
25	DQS ₁	26	DM ₁ \DQS ₁₀	75	VSS	76	VSS	125	VSS	126	VSS	175	DQ ₅₁	176	DQ ₅₅
27	VSS	28	VSS	77	DQS ₈ *	78	DM ₈ \DQS ₁₇ *	127	DQ ₃₂	128	DQ ₃₆	177	DQ ₅₆	178	DQ ₆₀
29	DQ ₁₀	30	DQ ₁₄	79	CB ₂ *	80	CB ₆ *	129	DQ ₃₃	130	DQ ₃₇	179	VDD	180	VDD
31	DQ ₁₁	32	DQ ₁₅	81	VDD	82	VDD	131	VDD	132	VDD	181	DQ ₅₇	182	DQ ₆₁
33	VDD	34	VDD	83	CB ₃ *	84	CB ₇ *	133	DQS ₄	134	DM ₄ \DQS ₁₃	183	DQS ₇	184	DM ₇ \DQS ₁₆
35	CK ₀	36	VDD	85	DU	86	DU(/RESET)*	135	DQ ₃₄	136	DQ ₃₈	185	VSS	186	VSS
37	/CK ₀	38	VSS	87	VSS	88	VSS	137	VSS	138	VSS	187	DQ ₅₈	188	DQ ₆₂
39	VSS	40	VSS	89	CK ₂ *	90	VSS	139	DQ ₃₅	140	DQ ₃₉	189	DQ ₅₉	190	DQ ₆₃
41	DQ ₁₆	42	DQ ₂₀	91	/CK ₂ *	92	VDD	141	DQ ₄₀	142	DQ ₄₄	191	VDD	192	VDD
43	DQ ₁₇	44	DQ ₂₁	93	VDD	94	VDD	143	VDD	144	VDD	193	SDA	194	SA ₀
45	VDD	46	VDD	95	CKE ₁	96	CKE ₀	145	DQ ₄₁	146	DQ ₄₅	195	SCL	196	SA ₁
47	DQS ₂	48	DM ₂ \DQS ₁₁	97	DU	98	DU	147	DQS ₅	148	DM ₅ \DQS ₁₄	197	VDDSPD	198	SA ₂
49	DQ ₁₈	50	DQ ₂₂	99	A ₁₂	100	A ₁₁	149	VSS	150	VSS	199	VDDID*	200	DU

Pin Description

Pin Symbol	Pin Function	Pin Symbol	Pin Function
CK(0:2)	Clock inputs, positive line	DQ(0:63)	Data input/output
/CK(0:2)	Clock inputs, negative line	CB(0:7)	Data check bits input/output
CKE(0:1)	Clock enables	DM(0:8)\DQS(9:17)	Low data masks/high data strobes
/RAS	Row address strobe	DQS(0:8)	Low data strobes
/CAS	Column address strobe	/RESET	Register initialization
/WE	Write enable	VDD	Core power
/S(0:1)	Chip selects	VSS	Ground
A(0:9,11:13)	Address inputs	VREF	Input/output reference
A ₁₀ /AP	Address input/Autoprecharge	VDDSPD	SPD power
BA(0:2)	SDRAM bank address	VDDID	VDD identification flag
SCL	SPD clock input		
SDA	SPD data input/output	DU	Don't Use
SA(0:2)	SPD address		

[illegible]

Notes: 1. Unless otherwise noted, all series resistors are 22 Ω .
2. DQ wiring may differ from that described in this drawing; however DQ, DQS, DM, CKE, and /S relationships are maintained as shown.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I²C; Current sink capability of SDA driver ≤3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported			Hex Value		
		PC266A	PC266B	PC200	PC266A	PC266B	PC200
0	# of bytes written into serial memory at module manufacturer	128 bytes			80h		
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)			08h		
2	Fundamental memory type	DDR SDRAM			07h		
3	# of row addresses on this assembly	13			0Dh		
4	# of column addresses on this assembly	11			0Bh		
5	# of physical banks on this assembly	2 banks			02h		
6	Data width of this assembly	64 bits			40h		
7	...Data width of this assembly (continued)	—			00h		
8	Voltage interface level of this assembly	SSTL 2.5V			04h		
9	SDRAM cycle time at CL=2.5 (t _{CYC})	7ns	7.5ns	8ns	70h	75h	80h
10	SDRAM access time from clock at CL=2.5 (t _{AC})	0.75ns	0.75ns	0.8h	75h	75h	80h
11	DIMM configuration type	none			00h		
12	Refresh rate/type	7.8μs, Self -refresh			82h		
13	SDRAM width	8 bits			08h		
14	Error Checking SDRAM data width	none			00h		
15	Min. CLK delay for back-to-back rand. col. addr.	t _{CCD} =1 CLK			01h		
16	SDRAM device attributes: burst lengths supported	2,4,8			0Eh		
17	SDRAM device attributes: # of banks on SDRAM device	4 banks			04h		
18	SDRAM device attributes: CAS latency	CAS latency = 2.0, 2.5			0Ch		
19	SDRAM device attributes: CS latency	CS latency = 0			01h		
20	SDRAM device attributes: Write latency	Write Latency = 1			02h		
21	SDRAM module attributes	Differential clock, PLL			24h		
22	SDRAM device attributes: general	V _{DD} ±0.2V			00h		
23	Minimum clock cycle time at CL=2 (t _{CYC})	7.5ns	8ns	10ns	75h	80h	10h
24	Max. data access time form clock at CL=2 (t _{AC})	0.75ns	0.75ns	0.8ns	75h	75h	80h
25	Minimum clock cycle time at CL=1.5 (t _{CYC})	N/A			00h		
26	Max. data access time from clock at CL=1.5 (t _{AC})	N/A			00h		
27	Minimum row precharge time (t _{RP})	20.0ns			50h		
28	Minimum row active to row active delay (t _{RRD})	15.0ns			3Ch		
29	Minumum RAS to CAS (t _{RCD})	20.0ns			50h		
30	Minumum RAS pulse width (t _{RAS})	45ns	45ns	50ns	2Dh	2Dh	32h
31	Module bank density	512MB			80h		
32	Min. command and address signal setup time (t _{AS})	1.1ns	1.1ns	1.2ns	E0h	E0h	C0h
33	Min. command and address signal hold time (t _{AH})	1.1ns	1.1ns	1.2ns	E0h	E0h	C0h
34	Min. data/data mask signal input setup time (t _{DS})	0.5ns	0.5ns	0.6ns	50h	50h	60h
35	Min. data/data mask signal input hold time (t _{DH})	0.5ns	0.5ns	0.6ns	50h	50h	60h

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Byte #	Function Described	Function Supported			Hex Value		
		PC266A	PC266B	PC200	PC266A	PC266B	PC200
36-61	Superset information (may be used in future)	no superset			00h		
62	SPD revision	JEDEC 1			00h		
63	Checksum for bytes 0-62	JEDEC calculation			xxh		
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code			7Fh		
65	Man. JEDEC ID code (continued)	SimpleTech's ID			A8h		
66-71					00h		
72	Manufacturing location	SimpleTech USA			01h		
73-90	Manufacturer's part number				xxh		
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)			01h		
92					00h		
93	Manufacturing date	Year (BCD)			yy		
94		Calender Week (BCD)			ww		
95	Assembly serial number	Tester number			ss		
96		Serial number (bits 7-0)			ss		
97		Serial number (bits 15-8)			ss		
98		Serial number (bits 23-16)			ss		
99-127	Manufacture's specific data				xxh		
128-255		Undefined			00h		