

**64M X 72 Bits (512MB) SDRAM 168-Pin Registered DIMM ECC (PC133)****FEATURES**

- PC133 Compliant  
(Option A:  $t_{CYC}=7.5ns@CL=3$ )  
(Option D:  $t_{CYC}=7.5ns@CL=2,3$ )
- Burst Mode Operation
- Auto and self refresh capability  
(8192 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V  $\pm 0.3V$  power supply
- MRS cycle with address key programs
  - CAS Latency (CL=2 or 3)
  - Burst Length (1, 2, 4, 8)
  - Data Type (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with 256 Byte EEPROM
- ECC

**GENERAL DESCRIPTION**

The SimpleTech SL72R8F64M8H-A75xV is a 64M x 72 bits Synchronous Dynamic RAM (SDRAM) Dual In-line Memory Module (DIMM).

This module consists of eighteen CMOS 8M x 8 bits x 4 banks SDRAMs in 54-pin 400-mil TSOP-II packages. The SDRAMs are mounted on a 168-pin glass epoxy substrate.

A serial EEPROM using the two pin I<sup>2</sup>C protocol is also mounted to provide for the Serial Presence Detects (SPD). PLL circuits supply clocks to the SDRAMs. Decoupling capacitors are also mounted. Damping resistors are added to the data signals. Control and address signals are registered.

The module has gold edge connections and is intended for mounting into 168-pin DIMM edge connector sockets keyed for 3.3V power supply.

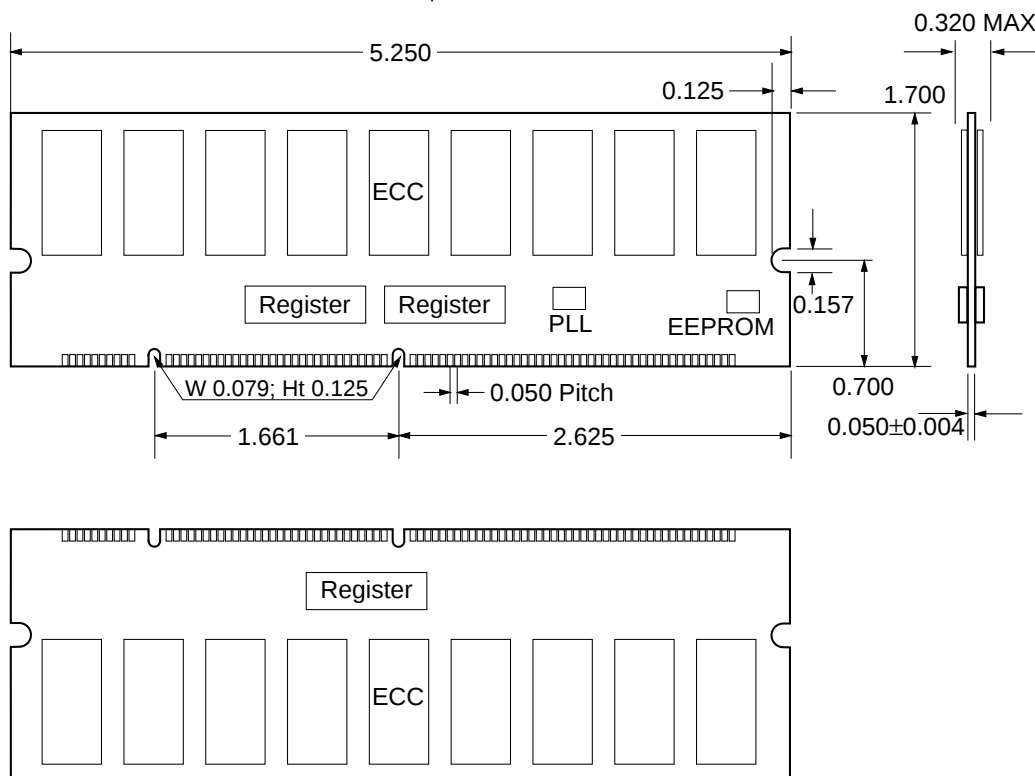
The module is PC133 compliant.

**ORDERING INFORMATION**

| SimpleTech<br>Part Number | PC133 133MHz Parameters |           |          |          |                                         |
|---------------------------|-------------------------|-----------|----------|----------|-----------------------------------------|
|                           | CL                      | $t_{RCD}$ | $t_{RP}$ | $t_{RC}$ | Comment                                 |
| SL72R8F64M8H-A75AV        | 3clks                   | 20ns      | 20ns     | 67.5ns   | Refer to option A in this specification |
| SL72R8F64M8H-A75DV        | 2clks                   | 15ns      | 15ns     | 67.5ns   | Refer to option D in this specification |

**MODULE DIMENSIONS**

Units are in inches. Tolerances are  $\pm 0.005$  unless otherwise specified.



814-1

## PIN CONFIGURATION

## Pin Symbols

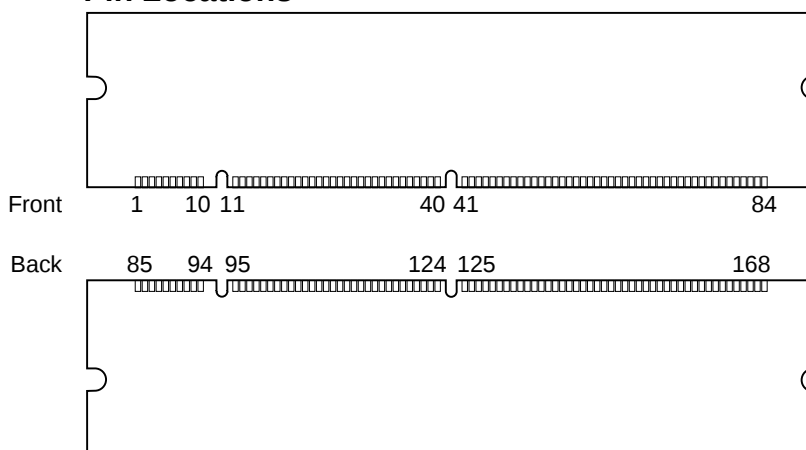
| Pin | Symbol | Pin | Symbol           | Pin | Symbol | Pin | Symbol | Pin | Symbol           | Pin | Symbol           |
|-----|--------|-----|------------------|-----|--------|-----|--------|-----|------------------|-----|------------------|
| 1   | VSS    | 25  | NC               | 49  | VDD    | 73  | VDD    | 97  | DQ41             | 121 | A9               |
| 2   | DQ0    | 26  | VDD              | 50  | NC     | 74  | DQ28   | 98  | DQ42             | 122 | BA0              |
| 3   | DQ1    | 27  | $\overline{WE}$  | 51  | NC     | 75  | DQ29   | 99  | DQ43             | 123 | A11              |
| 4   | DQ2    | 28  | DQMB0            | 52  | CB2    | 76  | DQ30   | 100 | DQ44             | 124 | VDD              |
| 5   | DQ3    | 29  | DQMB1            | 53  | CB3    | 77  | DQ31   | 101 | DQ45             | 125 | CK1              |
| 6   | VDD    | 30  | $\overline{S}_0$ | 54  | VSS    | 78  | VSS    | 102 | VDD              | 126 | A12              |
| 7   | DQ4    | 31  | NC               | 55  | DQ16   | 79  | CK2    | 103 | DQ46             | 127 | VSS              |
| 8   | DQ5    | 32  | VSS              | 56  | DQ17   | 80  | NC     | 104 | DQ47             | 128 | CKE0             |
| 9   | DQ6    | 33  | A0               | 57  | DQ18   | 81  | NC     | 105 | CB4              | 129 | $\overline{S}_3$ |
| 10  | DQ7    | 34  | A2               | 58  | DQ19   | 82  | SDA    | 106 | CB5              | 130 | DQMB6            |
| 11  | DQ8    | 35  | A4               | 59  | VDD    | 83  | SCL    | 107 | VSS              | 131 | DQMB7            |
| 12  | VSS    | 36  | A6               | 60  | DQ20   | 84  | VDD    | 108 | NC               | 132 | A13*             |
| 13  | DQ9    | 37  | A8               | 61  | NC     | 85  | VSS    | 109 | NC               | 133 | VDD              |
| 14  | DQ10   | 38  | A10/AP           | 62  | NC     | 86  | DQ32   | 110 | VDD              | 134 | NC               |
| 15  | DQ11   | 39  | BA1              | 63  | CKE1   | 87  | DQ33   | 111 | $\overline{CAS}$ | 135 | NC               |
| 16  | DQ12   | 40  | VDD              | 64  | VSS    | 88  | DQ34   | 112 | DQMB4            | 136 | CB6              |
| 17  | DQ13   | 41  | VDD              | 65  | DQ21   | 89  | DQ35   | 113 | DQMB5            | 137 | CB7              |
| 18  | VDD    | 42  | CK0              | 66  | DQ22   | 90  | VDD    | 114 | $\overline{S}_1$ | 138 | VSS              |
| 19  | DQ14   | 43  | VSS              | 67  | DQ23   | 91  | DQ36   | 115 | $\overline{RAS}$ | 139 | DQ48             |
| 20  | DQ15   | 44  | NC               | 68  | VSS    | 92  | DQ37   | 116 | VSS              | 140 | DQ49             |
| 21  | CB0    | 45  | $\overline{S}_2$ | 69  | DQ24   | 93  | DQ38   | 117 | A1               | 141 | DQ50             |
| 22  | CB1    | 46  | DQMB2            | 70  | DQ25   | 94  | DQ39   | 118 | A3               | 142 | DQ51             |
| 23  | VSS    | 47  | DQMB3            | 71  | DQ26   | 95  | DQ40   | 119 | A5               | 143 | VDD              |
| 24  | NC     | 48  | NC               | 72  | DQ27   | 96  | VSS    | 120 | A7               | 144 | DQ52             |
|     |        |     |                  |     |        |     |        |     |                  | 145 | NC               |
|     |        |     |                  |     |        |     |        |     |                  | 146 | NC               |
|     |        |     |                  |     |        |     |        |     |                  | 147 | REGE             |
|     |        |     |                  |     |        |     |        |     |                  | 148 | VSS              |
|     |        |     |                  |     |        |     |        |     |                  | 149 | DQ53             |
|     |        |     |                  |     |        |     |        |     |                  | 150 | DQ54             |
|     |        |     |                  |     |        |     |        |     |                  | 151 | DQ55             |
|     |        |     |                  |     |        |     |        |     |                  | 152 | VSS              |
|     |        |     |                  |     |        |     |        |     |                  | 153 | DQ56             |
|     |        |     |                  |     |        |     |        |     |                  | 154 | DQ57             |
|     |        |     |                  |     |        |     |        |     |                  | 155 | DQ58             |
|     |        |     |                  |     |        |     |        |     |                  | 156 | DQ59             |
|     |        |     |                  |     |        |     |        |     |                  | 157 | VDD              |
|     |        |     |                  |     |        |     |        |     |                  | 158 | DQ60             |
|     |        |     |                  |     |        |     |        |     |                  | 159 | DQ61             |
|     |        |     |                  |     |        |     |        |     |                  | 160 | DQ62             |
|     |        |     |                  |     |        |     |        |     |                  | 161 | DQ63             |
|     |        |     |                  |     |        |     |        |     |                  | 162 | VSS              |
|     |        |     |                  |     |        |     |        |     |                  | 163 | CK3              |
|     |        |     |                  |     |        |     |        |     |                  | 164 | NC               |
|     |        |     |                  |     |        |     |        |     |                  | 165 | SA0              |
|     |        |     |                  |     |        |     |        |     |                  | 166 | SA1              |
|     |        |     |                  |     |        |     |        |     |                  | 167 | SA2              |
|     |        |     |                  |     |        |     |        |     |                  | 168 | VDD              |

(Asterisk (\*) indicates that the pin is not used in this module.)

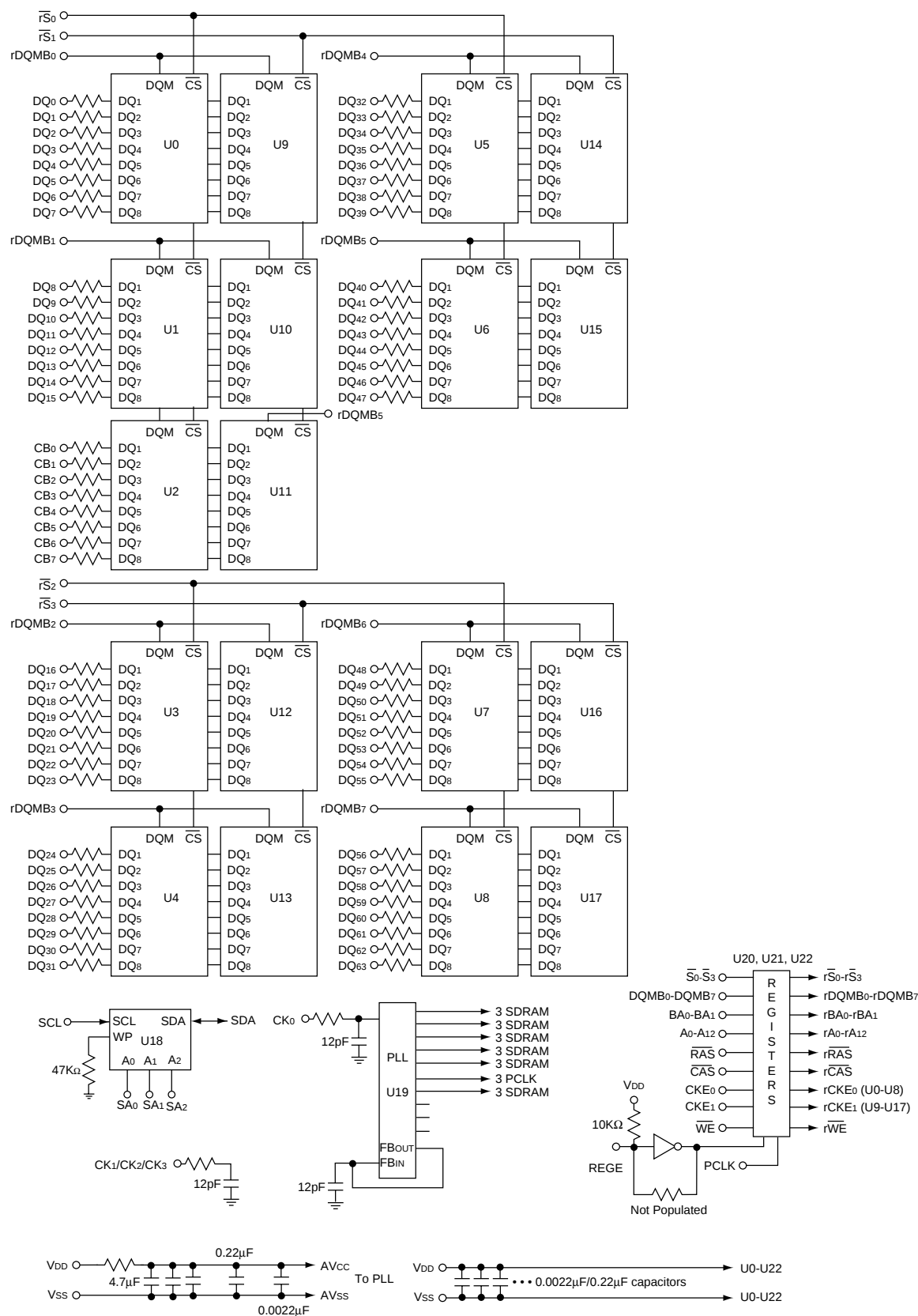
## Pin Functions

| Pin Symbol                          | Pin Function              |
|-------------------------------------|---------------------------|
| A0-A9, A11, A12                     | Address Inputs            |
| A10/AP                              | Address/Autoprecharge     |
| BA0, BA1                            | SDRAM Bank Address        |
| DQ0-DQ63                            | Data Inputs/Outputs       |
| CB0-CB7                             | Check Bits Inputs/Outputs |
| $\overline{WE}$                     | Write Enable              |
| CK0-CK3                             | Clock Inputs              |
| CKE0, CKE1                          | Clock Enables             |
| $\overline{RAS}$                    | Row Address Strobe        |
| $\overline{CAS}$                    | Column Address Strobe     |
| DQMB0-DQMB7                         | Data Mask                 |
| $\overline{S}_0$ - $\overline{S}_3$ | Chip Selects              |
| REGE                                | Register Enable           |
| SDA                                 | SPD Data Input/Output     |
| SCL                                 | SPD Clock Input           |
| SA0-SA2                             | SPD Address Input         |
| VDD                                 | Power (+3.3V)             |
| VSS                                 | Ground                    |
| NC                                  | No Connection             |

## Pin Locations



## FUNCTIONAL BLOCK DIAGRAM



All resistors are 10Ω unless otherwise specified.  
DQ wiring may differ from that described in this drawing;  
however, DQ/DQMB relationships is maintained as shown.

## SERIAL PRESENCE DETECTS

Serial PD Interface Protocol: I<sup>2</sup>C; Current sink capability of SDA driver  
 ≤3mA; Maximum clock frequency: 100 KHz

| Byte # | Function Described                                           | Function Supported         |          | Hex Value |          |
|--------|--------------------------------------------------------------|----------------------------|----------|-----------|----------|
|        |                                                              | Option A                   | Option D | Option A  | Option D |
| 0      | # of bytes written into serial memory at module manufacturer | 128 bytes                  |          | 80h       |          |
| 1      | Total # of bytes of SPD memory device                        | 256Bytes (2K-bit)          |          | 08h       |          |
| 2      | Fundamental memory type                                      | SDRAM                      |          | 04h       |          |
| 3      | # of row addresses on this assembly                          | 13                         |          | 0Dh       |          |
| 4      | # of column addresses on this assembly                       | 10                         |          | 0Ah       |          |
| 5      | # of module banks on this assembly                           | 2 banks                    |          | 01h       |          |
| 6      | Data width of this assembly                                  | 72 bits                    |          | 48h       |          |
| 7      | ...Data width of this assembly (continued)                   | —                          |          | 00h       |          |
| 8      | Voltage interface standard of this assembly                  | LVTTL                      |          | 01h       |          |
| 9      | SDRAM cycle time at CL=3 (tCYC)                              | 7.5ns                      | 7.5ns    | 75h       | 75h      |
| 10     | SDRAM access time from clock at CL=3 (tAC)                   | 5.4ns                      | 5.4ns    | 54h       | 54h      |
| 11     | DIMM configuration type                                      | ECC                        |          | 02h       |          |
| 12     | Refresh rate/type                                            | 8.7μs, Self-refresh        |          | 82h       |          |
| 13     | SDRAM width                                                  | 8 bits                     |          | 08h       |          |
| 14     | Error Checking DRAM data width                               | 8 bits                     |          | 08h       |          |
| 15     | Min. CLK delay for back-to-back rand. col. addr.             | tCCD=1 CLK                 |          | 01h       |          |
| 16     | SDRAM device attributes: burst lengths supported             | 1,2,4,8                    |          | 0Fh       |          |
| 17     | SDRAM device attributes: # of banks on SDRAM device          | 4 banks                    |          | 04h       |          |
| 18     | SDRAM device attributes: CAS latency                         | CAS latency = 2,3          |          | 06h       |          |
| 19     | SDRAM device attributes: CS latency                          | CS latency = 0             |          | 01h       |          |
| 20     | SDRAM device attributes: Write latency                       | Write Latency = 0          |          | 01h       |          |
| 21     | SDRAM module attributes                                      | Registered/Buffered/PLL    |          | 1Fh       |          |
| 22     | SDRAM device attributes: general                             | VCC10%, B/R, S/W, P/A, A/P |          | 0Eh       |          |
| 23     | Minimum clock cycle time at CL=2 (tCYC)                      | 10ns                       | 75ns     | A0h       | 75h      |
| 24     | Max. data access time form clock at CL=2 (tAC)               | 6ns                        | 5.4ns    | 60h       | 54h      |
| 25     | Minimum clock cycle time at CL=1 (tCYC)                      | —                          | —        | 00h       | 00h      |
| 26     | Max. data access time from clock at CL=1 (tAC)               | —                          | —        | 00h       | 00h      |
| 27     | Minimum row precharge time (tRP)                             | 20ns                       | 15ns     | 14h       | 0Fh      |
| 28     | Minimum row active to row active delay (tRRD)                | 15ns                       | 15ns     | 0Fh       | 0Fh      |
| 29     | Minumum RAS to CAS (tRCD)                                    | 20ns                       | 15ns     | 14h       | 0Fh      |
| 30     | Minumum RAS pulse width (tRAS)                               | 45ns                       | 45ns     | 2Dh       | 2Dh      |
| 31     | Module bank density                                          | 256MB                      |          | 40h       |          |
| 32     | Min. command and address signal setup time (tAS)             | 1.5ns                      |          | 15h       |          |
| 33     | Min. command and address signal hold time (tAH)              | 0.8ns                      |          | 08h       |          |
| 34     | Min. data signal input setup time (tDS)                      | 1.5ns                      |          | 15h       |          |
| 35     | Min. data signal input hold time (tDH)                       | 0.8ns                      |          | 08h       |          |
| 36-61  | Superset information (may be used in future)                 | —                          |          | 00h       |          |
| 62     | SPD revision                                                 | 2                          |          | 02h       |          |
| 63     | Checksum for bytes 0-62                                      | JEDEC calc                 |          | xxh       |          |
| 64     | Manufacturer's JEDEC ID code per JEP-106E                    | Continuation code          |          | 7Fh       |          |
| 65     | Man. JEDEC ID code (continued)                               | SimpleTech's ID            |          | A8h       |          |

continued on the next page

**SERIAL PRESENCE DETECTS** *(continued)*

| Byte # | Function Described            | Function Supported                             |          | Hex Value |          |
|--------|-------------------------------|------------------------------------------------|----------|-----------|----------|
|        |                               | Option A                                       | Option D | Option A  | Option D |
| 66-71  | —                             | —                                              |          | 00h       |          |
| 72     | Manufacturing location        | SimpleTech USA (1)                             |          | 01h       |          |
| 73-90  | Manufacturer's part number    |                                                |          | xxh       |          |
| 91     | PCB Revision code             | Eng(00), RevA(01), RevB(02)                    |          | 01h       |          |
| 92     | —                             | —                                              |          | FFh       |          |
| 93     | Manufacturing date            | Year(BCD format)                               |          | yyh       |          |
| 94     | —                             | Calender Week(BCD format)                      |          | wwh       |          |
| 95     | Assembly serial number        | Tester Number                                  |          | ssh       |          |
| 96     | —                             | serial#(bits7-0)                               |          | ssh       |          |
| 97     | —                             | serial#(bits15-8)                              |          | ssh       |          |
| 98     | —                             | serial#(bits23-16)                             |          | ssh       |          |
| 99-125 | Manufacturer's specific data  |                                                |          | xxh       |          |
| 126    | Intel specification frequency | 100MHz                                         |          | 64h       |          |
| 127    | Intel specification details   | CLK0; junc temp.TBD;<br>CL2,CL3; concurrent AP |          | 8Fh       |          |
| 128+   | —                             |                                                |          | 00h       |          |