

64M X 72 Bits (512MB) DDR SDRAM 184-Pin Registered DIMM ECC (PC1600/PC2100)**FEATURES**

- PC1600/PC2100 Compliant
(PC266A 133MHz—7.5ns@CL=2)
(PC266B 133MHz—7.5ns@CL=2.5)
(PC200 100MHz—10ns@CL=2)
- 184-Pin DIMM form factor
- Auto and self refresh capability
(8192 cycles/64ms refresh)
- SSTL_2 compatible inputs and outputs
- $+2.5V \pm 0.2V$ V_{DD} and V_{DDQ}
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0 and /CK0), and bi-directional data strobe (DQS)
- Four internal banks for concurrent operation
- Auto Precharge option for each burst access
- Burst lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect with EEPROM
- ECC

GENERAL DESCRIPTION

The SimpleTech SL72E8F64M8M-A###W is a 64M x 72 bits Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Dual In-line Memory Module (DIMM).

This module consists of eighteen CMOS 8M x 8 bits x 4 banks DDR SDRAMs in 66-pin 400-mil TSOP-II packages. The DDR SDRAMs are mounted on a 184-pin glass epoxy substrate.

A serial EEPROM using the two pin IIC protocol is also mounted to provide for the Serial Presence Detects (SPD). PLL circuits supply clocks to the DDR SDRAMs. Decoupling capacitors of 0.22μF are also mounted. Damping resistors are added to the DQ, DM, and DQS signals.

The module has gold edge connections and is intended for mounting into 184-pin DIMM edge connector sockets keyed for 2.5V V_{DD} and V_{DDQ}.

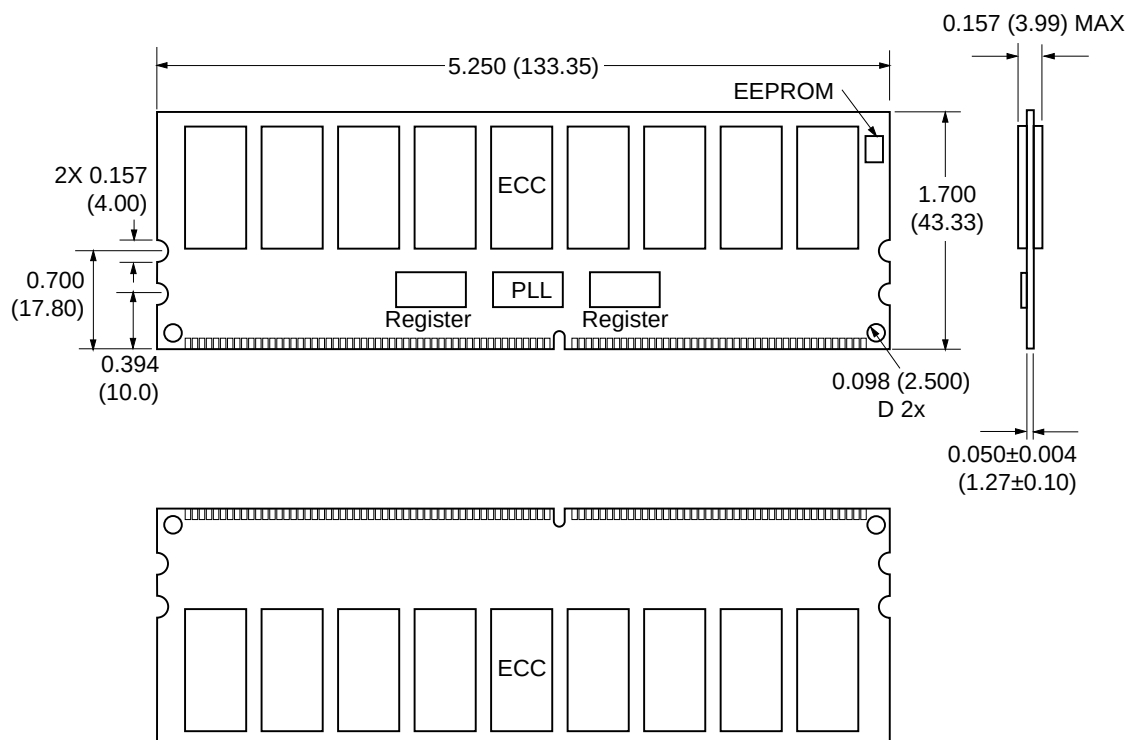
The module is available in three component options: PC266A, PC266B, and PC200. The module is PC1600 or PC2100 compliant.

ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL72E8F64M8M-A75DW	2	133	2.1 GB/s
SL72E8F64M8M-A75EW	2.5	133	2.1 GB/s
SL72E8F64M8M-A10DW	2	100	1.6 GB/s

PACKAGE DIMENSIONS

Units are in inches (millimeters). Tolerances are ± 0.005 (± 0.15) unless otherwise specified.



* "Preliminary" indicates that this product is in design. Parameters may change.

PIN CONFIGURATION (*=Not Used; /=Active Low)

Pinout

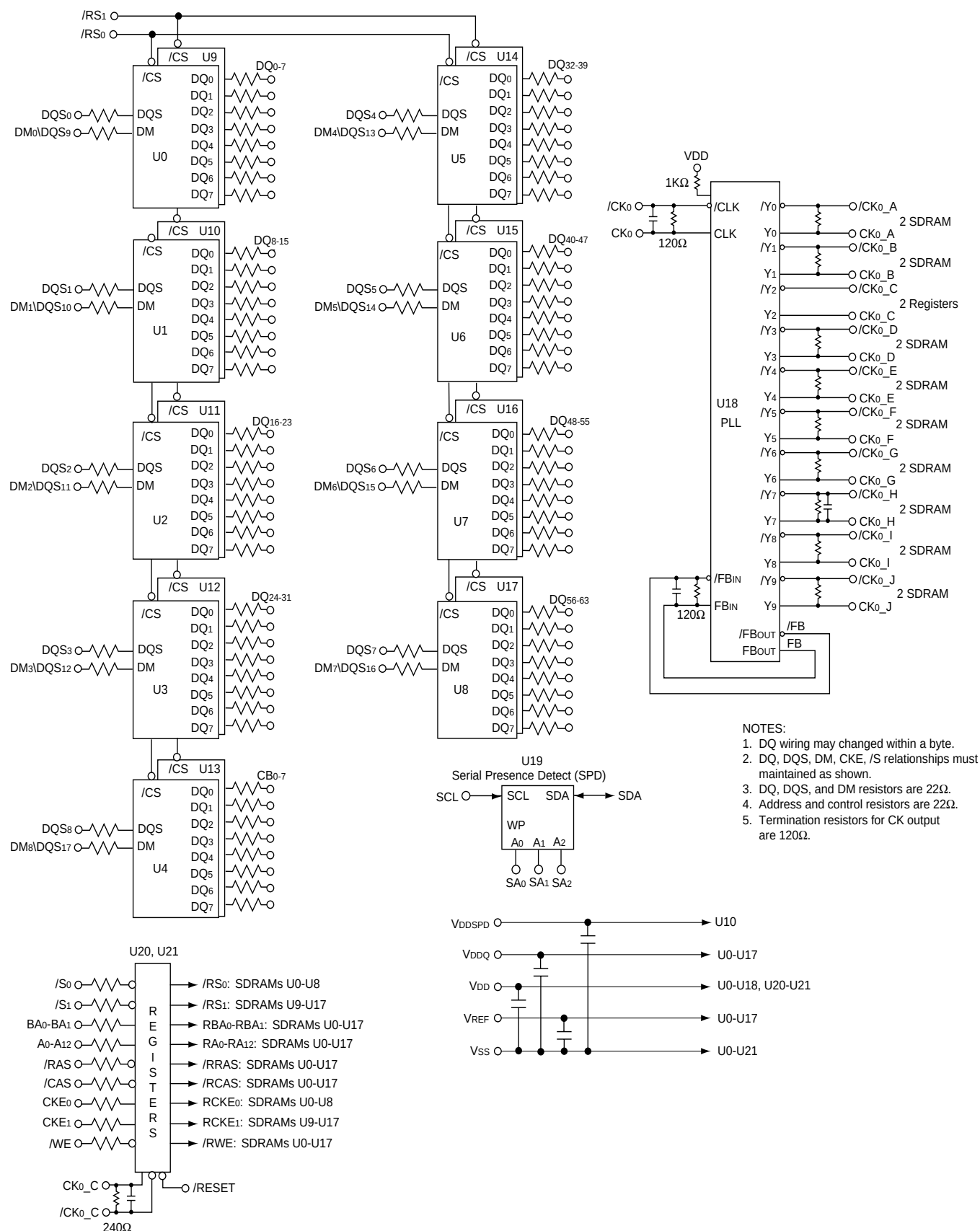
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	93	VSS	32	A5	124	VSS	62	VDDQ	154	/RAS
2	DQ0	94	DQ4	33	DQ24	125	A6	63	/WE	155	DQ45
3	VSS	95	DQ5	34	VSS	126	DQ28	64	DQ41	156	VDDQ
4	DQ1	96	VDDQ	35	DQ25	127	DQ29	65	/CAS	157	/S0
5	DQS0	97	DM0\DQS9	36	DQS3	128	VDDQ	66	VSS	158	/S1
6	DQ2	98	DQ6	37	A4	129	DM3\DQS12	67	DQS5	159	DM5\DQS14
7	VDD	99	DQ7	38	VDD	130	A3	68	DQ42	160	VSS
8	DQ3	100	VSS	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	VSS	70	VDD	162	DQ47
10	/RESET	102	NC	41	A2	133	DQ31	71	/S2*	163	/S3*
11	VSS	103	A13*	42	VSS	134	CB4	72	DQ48	164	VDDQ
12	DQ8	104	VDDQ	43	A1	135	CB5	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	CB0	136	VDDQ	74	VSS	166	DQS3
14	DQS1	106	DQ13	45	CB1	137	CK0	75	CK2*	167	FETEN*
15	VDDQ	107	DM1\DQS10	46	VDD	138	/CK0	76	/CK2*	168	VDD
16	CK1*	108	VDD	47	DQS8	139	VSS	77	VDDQ	169	DM6\DQS15
17	/CK1*	109	DQ14	48	A0	140	DM8\DQS17	78	DQS6	170	DQ54
18	VSS	110	DQ15	49	CB2	141	A10	79	DQ50	171	DQ55
19	DQ10	111	CKE1	50	VSS	142	CB6	80	DQ51	172	VDDQ
20	DQ11	112	VDDQ	51	CB3	143	VDDQ	81	VSS	173	NC
21	CKE0	113	BA2*	52	BA1	144	CB7	82	VDDID*	174	DQ60
22	VDDQ	114	DQ20	Key		Key		83	DQ56	175	DQ61
23	DQ16	115	A12	53	DQ32	145	VSS	84	DQ57	176	VSS
24	DQ17	116	VSS	54	VDDQ	146	DQ36	85	VDD	177	DM7\DQS16
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	VSS	118	A11	56	DQS4	148	VDD	87	DQ58	179	DQ63
27	A9	119	DM2\DQS11	57	DQ34	149	DM4\DQS13	88	DQ59	180	VDDQ
28	DQ18	120	VDD	58	VSS	150	DQ38	89	VSS	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	NC	182	SA1
30	VDDQ	122	A8	60	DQ35	152	VSS	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	VDDSPD

Pin Description

Pin Symbol	Pin Description
A0-A12, A13*	SDRAM address bus
BA0-BA1, BA2*	SDRAM bank select
DQ0-DQ63	DIMM memory data bus
CB0-CB7	DIMM ECC check bits
/RAS	SDRAM row address strobe
/CAS	SDRAM column address strobe
/WE	SDRAM write strobe
/S0, /S1, /S2*, /S3*	SDRAM chip select lines (Physical banks 0, 1, 2, and 3)
CKE0, CKE1	SDRAM clock enable lines
DQS0-DQS8	SDRAM low data strobes
DM(0-8)\DQS(9-17)	SDRAM low data masks/high data strobes (x4, x8-based x72 DIMMs)
VDDID*	VDD Identification flag
CK0, CK1*, CK2*	SDRAM clock (positive line of differential pair)

Pin Symbol	Pin Description
/CK0, /CK1*, /CK2*	SDRAM clock (negative line of differential pair)
SCL	IIC serial bus clock for EEPROM
SDA	IIC serial bus data line for EEPROM
SA0-SA2	IIC slave address select for EEPROM
VDD	SDRAM positive power supply
VDDQ	SDRAM I/O driver positive power supply
VREF	SDRAM I/O reference supply
VSS	Power supply return (ground)
VDDSPD	Serial EEPROM positive power supply (2.5 volts)
NC	Spare pins (no connect)
/RESET	Reset pin (forces register inputs low)
FETEN*	FET enable line

FUNCTIONAL BLOCK DIAGRAM



SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: IIC; Current sink capability of SDA driver - 3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported			Hex Value		
		PC266A	PC266B	PC200	PC266A	PC266B	PC200
0	# of bytes written into serial memory at module manufacturer	128 bytes			80h		
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)			08h		
2	Fundamental memory type	DDR SDRAM			07h		
3	# of row addresses on this assembly	13			0Dh		
4	# of column addresses on this assembly	10			0Ah		
5	# of physical banks on this assembly	2 banks			02h		
6	Data width of this assembly	72 bits			48h		
7	...Data width of this assembly (continued)	—			00h		
8	Voltage interface level of this assembly	SSTL 2.5V			04h		
9	SDRAM cycle time at CL=2.5 (t _{CYC})	7ns	7.5ns	8ns	70h	75h	80h
10	SDRAM access time from clock at CL=2.5 (t _{AC})	0.75ns	0.75ns	0.8ns	75h	75h	80h
11	DIMM configuration type	ECC			02h		
12	Refresh rate/type	7.8μs, Self -refresh			82h		
13	SDRAM width	8 bits			08h		
14	Error Checking SDRAM data width	8 bits			08h		
15	Min. CLK delay for back-to-back rand. col. addr.	t _{CCD} =1 CLK			01h		
16	SDRAM device attributes: burst lengths supported	2,4,8			0Eh		
17	SDRAM device attributes: # of banks on SDRAM device	4 banks			04h		
18	SDRAM device attributes: CAS latency	CAS latency = 2.0, 2.5			0Ch		
19	SDRAM device attributes: CS latency	CS latency = 0			01h		
20	SDRAM device attributes: Write latency	Write Latency = 1			02h		
21	SDRAM module attributes	Registered with PLL, Differential clock			26h		
22	SDRAM device attributes: general	V _{DD} ±0.2V			00h		
23	Minimum clock cycle time at CL=2 (t _{CYC})	7.5ns	8ns	10ns	75h	80h	10h
24	Max. data access time form clock at CL=2 (t _{AC})	0.75ns	0.75ns	0.8ns	75h	75h	80h
25	Minimum clock cycle time at CL=1.5 (t _{CYC})	N/A			00h		
26	Max. data access time from clock at CL=1.5 (t _{AC})	N/A			00h		
27	Minimum row precharge time (t _{RP})	20.0ns			50h		
28	Minimum row active to row active delay (t _{RRD})	15.0ns			3Ch		
29	Minumum RAS to CAS (t _{RCD})	20.0ns			50h		
30	Minumum RAS pulse width (t _{RAS})	45ns	45ns	50ns	2Dh	2Dh	32h
31	Module bank density	256MB			40h		
32	Min. command and address signal setup time (t _{AS})	1.1ns	1.1ns	1.2ns	E0h	E0h	C0h
33	Min. command and address signal hold time (t _{AH})	1.1ns	1.1ns	1.2ns	E0h	E0h	C0h
34	Min. data/data mask signal input setup time (t _{DS})	0.5ns	0.5ns	0.6ns	50h	50h	60h
35	Min. data/data mask signal input hold time (t _{DH})	0.5ns	0.5ns	0.6ns	50h	50h	60h

continued on the next page

Byte #	Function Described	Function Supported			Hex Value		
		PC266A	PC266B	PC200	PC266A	PC266B	PC200
36-61	Superset information (may be used in future)	no superset			00h		
62	SPD revision	JEDEC 1			00h		
63	Checksum for bytes 0-62	JEDEC calculation			xxh		
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code			7Fh		
65	Man. JEDEC ID code (continued)	SimpleTech's ID			A8h		
66-71					FFh		
72	Manufacturing location	SimpleTech USA			01h		
73-90	Manufacturer's part number				xxh		
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)			01h		
92					FFh		
93	Manufacturing date	Year (BCD)			yy		
94		Calender Week (BCD)			ww		
95	Assembly serial number	Tester number			ss		
96		Serial number (bits 7-0)			ss		
97		Serial number (bits 15-8)			ss		
98		Serial number (bits 23-16)			ss		
99	Manufacture's specific data	S			53h		
100		i			69h		
101		l			6Ch		
102		i			69h		
103		c			63h		
104		o			6Fh		
105		n			6Eh		
106		T			54h		
107		e			65h		
108		c			63h		
109		h			68h		
110-127	Reserved	Undefined			00h		
128-255	Open for Customer Use	Undefined			00h		

Note: SiliconTech mentioned in the SPD refers to the former name of SimpleTech's OEM Division