

OVERVIEW

The SM5010 series are crystal oscillator module ICs, that incorporate oscillator and output buffer circuits. High-frequency capacitors and feedback resistors are built-in, eliminating the need for external components to make a stable fundamental-harmonic oscillator.

FEATURES

- Inverter amplifier feedback resistor built-in
- Capacitors C_G , C_D built-in
- Standby function
- Power-save pull-up resistor built-in (5010CL×)
- 16 mA ($V_{DD} = 4.5$ V) drive capability (5010AN×, AK×, BN×, BK×, CL×, DN×)
- 4 mA ($V_{DD} = 4.5$ V) drive capability (5010AH×, BH×)
- Output three-state function
- 2.7 to 5.5 V supply voltage
- Oscillator frequency output (f_O , $f_O/2$, $f_O/4$, $f_O/8$ determined by internal connection)
- 8-pin SOP (SM5010×××S)
- Chip form (CF5010×××)

SERIES CONFIGURATION

Version ¹	Output frequency	3V operating		5V operating			R_D [Ω]	Built-in capacitance		Input level (5V)	Output duty level	Standby function
		Output load (max) [pF]	Recommended operating frequency range [MHz]	Output load (max) [pF]	Recommended operating frequency range [MHz]	Output current [mA]		C_G [pF]	C_D [pF]			
SM5010AN1S	f_O	15	30	50	30	16	—	29	29	TTL	CMOS	No
SM5010AN2S	$f_O/2$	15	30	50	30	16	—	29	29	TTL	CMOS/TTL	No
SM5010AN3S	$f_O/4$	15	30	50	30	16	—	29	29	TTL	CMOS/TTL	No
SM5010AN4S	$f_O/8$	15	30	50	30	16	—	29	29	TTL	CMOS/TTL	No
SM5010AK1S	f_O	—	—	15	30	16	—	29	29	TTL	TTL	No
SM5010AH1S	f_O	15	16	15	30	4	—	29	29	TTL	CMOS	No
SM5010AH2S	$f_O/2$	15	16	15	30	4	—	29	29	TTL	CMOS	No
SM5010AH3S	$f_O/4$	15	16	15	30	4	—	29	29	TTL	CMOS	No
SM5010AH4S	$f_O/8$	15	16	15	30	4	—	29	29	TTL	CMOS	No
SM5010BN1S	f_O	15	30	50	30	16	820	22	22	TTL	CMOS	No
SM5010BN2S	$f_O/2$	15	30	50	30	16	820	22	22	TTL	CMOS/TTL	No
SM5010BN3S	$f_O/4$	15	30	50	30	16	820	22	22	TTL	CMOS/TTL	No
SM5010BN4S	$f_O/8$	15	30	50	30	16	820	22	22	TTL	CMOS/TTL	No
SM5010BK1S	f_O	—	—	15	30	16	820	22	22	TTL	TTL	No
SM5010BH1S	f_O	15	16	15	30	4	820	22	22	TTL	CMOS	No
SM5010BH2S	$f_O/2$	15	16	15	30	4	820	22	22	TTL	CMOS	No
SM5010BH3S	$f_O/4$	15	16	15	30	4	820	22	22	TTL	CMOS	No
SM5010BH4S	$f_O/8$	15	16	15	30	4	820	22	22	TTL	CMOS	No
SM5010CL1S	f_O	15	30	50	30	16	—	18	18	CMOS	CMOS	Yes
SM5010CL2S	$f_O/2$	15	30	50	30	16	—	18	18	CMOS	CMOS	Yes
SM5010CL3S	$f_O/4$	15	30	50	30	16	—	18	18	CMOS	CMOS	Yes
SM5010CL4S	$f_O/8$	15	30	50	30	16	—	18	18	CMOS	CMOS	Yes
SM5010DN1S	f_O	15	30	50	30	16	820	—	—	TTL	CMOS	No

1. Chip form devices have designation CF5010×××.

Note: Recommended operating frequency is not the guaranteed value but is measured using NPC's standard crystal.

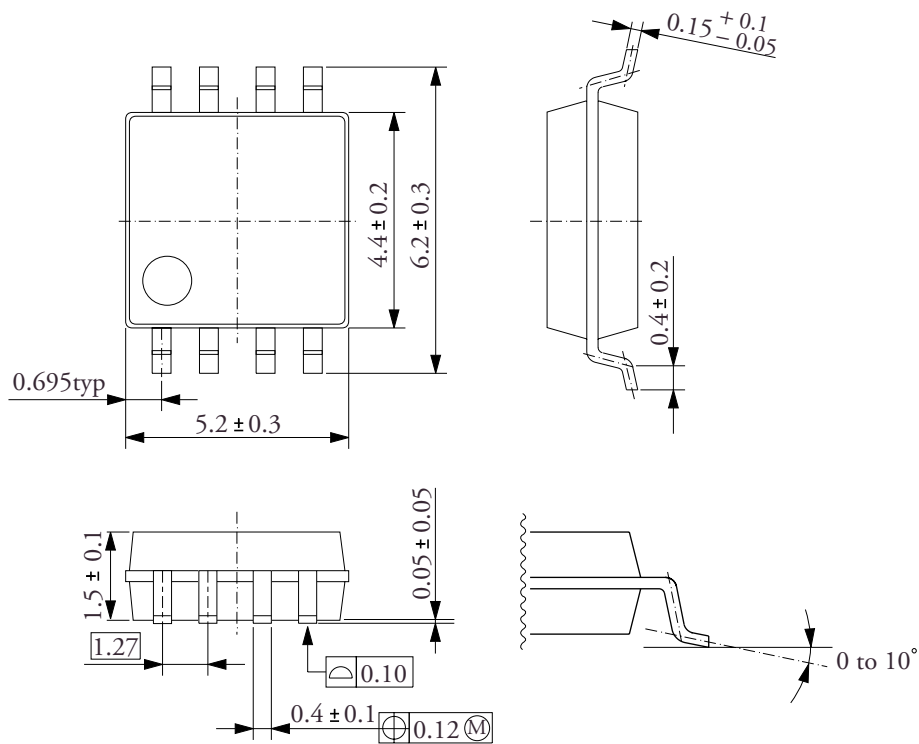
ORDERING INFORMATION

Device	Package
SM5010×××S	8-pin SOP
CF5010×××-1	Chip form

PACKAGE DIMENSIONS

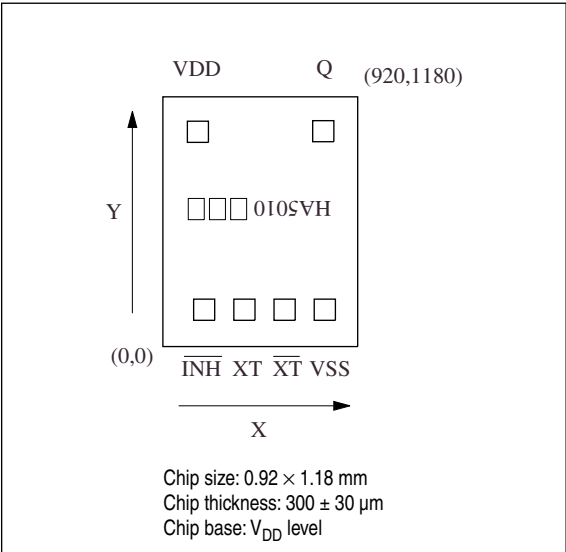
(Unit:mm)

- 8-pin SOP



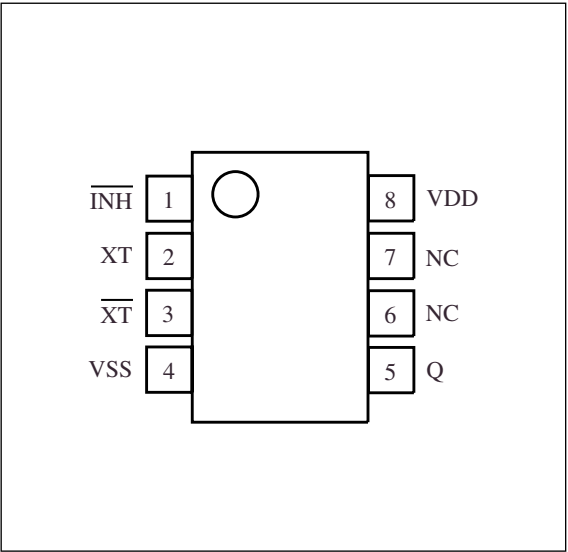
PAD LAYOUT

(Unit:μm)



PINOUT

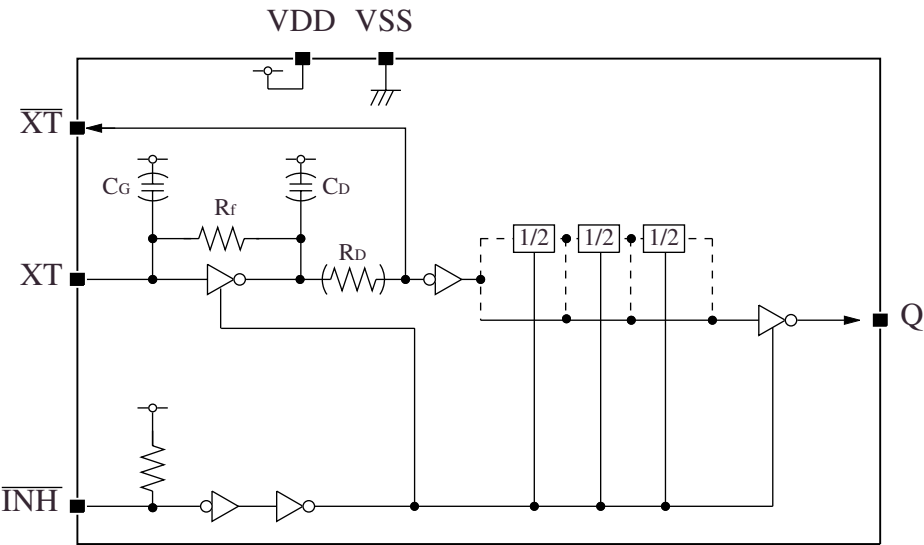
(Top view)



PIN DESCRIPTION and PAD DIMENSIONS

Number	Name	I/O	Description	Pad dimensions [μm]	
				X	Y
1	INH	I	Output state control input. High impedance when LOW. In the case of the 5010CLx, the oscillator stops and Power-saving pull-up resistor built in.	195	174.4
2	XT	I	Amplifier input.	385	174.4
3	XT	O	Amplifier output.	575	174.4
4	VSS	–	Ground	765	174.4
5	Q	O	Output. Output frequency (f _O , f _O /2, f _O /4, f _O /8) determined by internal connection	757.6	1017.6
6	NC	–	No connection	–	–
7	NC	–	No connection	–	–
8	VDD	–	Supply voltage	165.4	1014.6

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

 $V_{SS} = 0\text{ V}$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		-0.5 to 7.0	V
Input voltage range	V_{IN}		-0.5 to $V_{DD} + 0.5$	V
Output voltage range	V_{OUT}		-0.5 to $V_{DD} + 0.5$	V
Operating temperature range	T_{opr}		-40 to 85	°C
Storage temperature range	T_{stg}	Chip form	-65 to 150	°C
		8-pin SOP	-55 to 125	
Output current	I_{OUT}	5010×H×	10	mA
		5010×N×, ×K×, CL×	25	
Power dissipation	P_D	8-pin SOP	500	mW

Recommended Operating Conditions

3V operation

 $V_{SS} = 0\text{ V}$

Parameter	Symbol	Series	Condition	Rating			Unit
				min	typ	max	
Supply voltage	V_{DD}	×N×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	2.7	—	3.6	V
		×H×	$2 \leq f \leq 16\text{ MHz}$, $C_L \leq 15\text{ pF}$	2.7	—	3.6	
		CL×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	2.7	—	3.6	
Input voltage	V_{IN}	×N×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	V_{SS}	—	V_{DD}	V
		×H×	$2 \leq f \leq 16\text{ MHz}$, $C_L \leq 15\text{ pF}$	V_{SS}	—	V_{DD}	
		CL×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	V_{SS}	—	V_{DD}	
Operating temperature	T_{OPR}	×N×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	-10	—	+70	°C
		×H×	$2 \leq f \leq 16\text{ MHz}$, $C_L \leq 15\text{ pF}$	-10	—	+70	
		CL×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	-20	—	+80	

5V operation

 $V_{SS} = 0\text{ V}$

Parameter	Symbol	Series	Condition	Rating			Unit
				min	typ	max	
Supply voltage	V_{DD}	×N×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 50\text{ pF}$	4.5	—	5.5	V
		×K×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	4.5	—	5.5	
		×H×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	4.5	—	5.5	
		CL×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 50\text{ pF}$	4.5	—	5.5	
Input voltage	V_{IN}	×N×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 50\text{ pF}$	V_{SS}	—	V_{DD}	V
		×K×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	V_{SS}	—	V_{DD}	
		×H×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	V_{SS}	—	V_{DD}	
		CL×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 50\text{ pF}$	V_{SS}	—	V_{DD}	
Operating temperature	T_{OPR}	×N×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 50\text{ pF}$	-40	—	+85	°C
		×K×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	-40	—	+85	
		×H×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 15\text{ pF}$	-40	—	+85	
		CL×	$2 \leq f \leq 30\text{ MHz}$, $C_L \leq 50\text{ pF}$	-40	—	+85	

Electrical Characteristics

5010×N× series

3 V operation: $V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -10$ to 70 °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 2.7 V, I _{OH} = 8 mA		2.1	2.4	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 2.7 V, I _{OL} = 8 mA		–	0.3	0.4	V
Output leakage current	I _Z	Q: Measurement cct 2, $\overline{\text{INH}}$ = LOW, V _{DD} = 3.6 V, V _{OH} = V _{DD}		–	–	10	μA
		Q: Measurement cct 2, $\overline{\text{INH}}$ = LOW, V _{DD} = 3.6 V, V _{OL} = V _{SS}		–	–	10	
HIGH-level input voltage	V _{IH}	$\overline{\text{INH}}$		2.0	–	–	V
LOW-level input voltage	V _{IL}	$\overline{\text{INH}}$		–	–	0.5	V
Current consumption	I _{DD}	Measurement cct 3, load cct 1, $\overline{\text{INH}}$ = open, C _L = 15 pF, f = 30 MHz	5010×N1	–	5	10	mA
			5010×N2	–	3.5	7	
			5010×N3	–	2.5	5	
			5010×N4	–	2	4	
$\overline{\text{INH}}$ pull-up resistance	R _{UP1}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5		80	200	500	kΩ
Oscillator amplifier output resistance	R _D	Design value	5010B××	690	820	940	Ω
Built-in capacitance	C _G	Design value, determined by the internal wafer pattern	5010A××	26	29	32	pF
			5010B××	20	22	24	
	C _D		5010A××	26	29	32	
			5010B××	20	22	24	

5010×N×, ×K× series

5 V operation: $V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -40$ to 85 °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 4.5 V, I _{OH} = 16 mA		3.9	4.2	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 4.5 V, I _{OL} = 16 mA		–	0.3	0.4	V
Output leakage current	I _Z	Q: Measurement cct 2, $\overline{\text{INH}}$ = LOW, V _{DD} = 5.5 V, V _{OH} = V _{DD}		–	–	10	μA
		Q: Measurement cct 2, $\overline{\text{INH}}$ = LOW, V _{DD} = 5.5 V, V _{OL} = V _{SS}		–	–	10	
HIGH-level input voltage	V _{IH}	$\overline{\text{INH}}$		2.0	–	–	V
LOW-level input voltage	V _{IL}	$\overline{\text{INH}}$		–	–	0.8	V
Current consumption	I _{DD}	Measurement cct 3, load cct 1, INH = open, C _L = 50 pF, f = 30 MHz	5010×N1	–	15	30	mA
			5010×N2	–	9	18	
			5010×N3	–	6	12	
			5010×N4	–	5	10	
		Measurement cct 3, load cct 2, INH = open, C _L = 15 pF, f = 30 MHz	5010×K×	–	10	20	
INH pull-up resistance	R _{UP1}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5		80	200	500	kΩ
Oscillator amplifier output resistance	R _D	Design value	5010B×	690	820	940	Ω
Built-in capacitance	C _G	Design value, determined by the internal wafer pattern	5010A×	26	29	32	pF
			5010B×	20	22	24	
	C _D		5010A×	26	29	32	
			5010B×	20	22	24	

SM5010 series

5010×H× series

3 V operation: $V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -10$ to 70 °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 2.7 V, I _{OH} = 2 mA		2.1	2.4	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 2.7 V, I _{OL} = 2 mA		–	0.3	0.5	V
Output leakage current	I _Z	Q: Measurement cct 2, $\overline{\text{INH}}$ = LOW, V _{DD} = 3.6 V, V _{OH} = V _{DD}	–	–	10	μA	
		Q: Measurement cct 2, $\overline{\text{INH}}$ = LOW, V _{DD} = 3.6 V, V _{OL} = V _{SS}	–	–	10		
HIGH-level input voltage	V _{IH}	$\overline{\text{INH}}$		2.0	–	–	V
LOW-level input voltage	V _{IL}	$\overline{\text{INH}}$		–	–	0.5	V
Current consumption	I _{DD}	Measurement cct 3, load cct 1, INH = open, C _L = 15 pF, f = 16 MHz	5010×H1	–	3	6	mA
			5010×H2	–	2	4	
			5010×H3	–	1.5	3	
			5010×H4	–	1.5	2.5	
$\overline{\text{INH}}$ pull-up resistance	R _{UP1}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5		80	200	500	kΩ
Oscillator amplifier output resistance	R _D	Design value	5010B××	690	820	940	Ω
Built-in capacitance	C _G	Design value, determined by the internal wafer pattern	5010A××	26	29	32	pF
			5010B××	20	22	24	
	C _D		5010A××	26	29	32	
			5010B××	20	22	24	

5 V operation: $V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -40$ to 85 °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 4.5 V, I _{OH} = 4 mA		3.9	4.2	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 4.5 V, I _{OL} = 4 mA		–	0.3	0.5	V
Output leakage current	I _Z	Q: Measurement cct 2, $\overline{\text{INH}}$ = LOW, V _{DD} = 5.5 V, V _{OH} = V _{DD}		–	–	10	μA
		Q: Measurement cct 2, $\overline{\text{INH}}$ = LOW, V _{DD} = 5.5 V, V _{OL} = V _{SS}		–	–	10	
HIGH-level input voltage	V _{IH}	$\overline{\text{INH}}$		2.0	–	–	V
LOW-level input voltage	V _{IL}	$\overline{\text{INH}}$		–	–	0.8	V
Current consumption	I _{DD}	Measurement cct 3, load cct 1, $\overline{\text{INH}}$ = open, C _L = 15 pF, f = 30 MHz	5010×H1	–	9	18	mA
			5010×H2	–	6	12	
			5010×H3	–	5	10	
			5010×H4	–	4	8	
$\overline{\text{INH}}$ pull-up resistance	R _{UP1}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5		80	200	500	kΩ
Oscillator amplifier output resistance	R _D	Design value	5010B××	690	820	940	Ω
Built-in capacitance	C _G	Design value, determined by the internal wafer pattern	5010A××	26	29	32	pF
			5010B××	20	22	24	
	C _D		5010A××	26	29	32	
			5010B××	20	22	24	

SM5010 series

5010CL× series

3 V operation: $V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -20$ to 80 °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, $V_{DD} = 2.7$ V, $I_{OH} = 8$ mA	2.2	2.4	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, $V_{DD} = 2.7$ V, $I_{OL} = 8$ mA	–	0.3	0.4	V
Output leakage current	I_Z	Q: Measurement cct 2, $\overline{INH} = \text{LOW}$, $V_{DD} = 3.6$ V, $V_{OH} = V_{DD}$	–	–	10	μA
		Q: Measurement cct 2, $\overline{INH} = \text{LOW}$, $V_{DD} = 3.6$ V, $V_{OL} = V_{SS}$	–	–	10	
HIGH-level input voltage	V_{IH}	$\overline{INH}$	$0.7V_{DD}$	–	–	V
LOW-level input voltage	V_{IL}	$\overline{INH}$	–	–	$0.3V_{DD}$	V
Current consumption	I_{DD}	Measurement cct 3, load cct 1, $\overline{INH} = \text{open}$, $C_L = 15$ pF, $f = 30$ MHz	5010CL1	–	5	mA
			5010CL2	–	3.5	
			5010CL3	–	2.5	
			5010CL4	–	2	
Standby current	I_{ST}	Measurement cct 6, $\overline{INH} = \text{LOW}$	–	–	5	μA
$\overline{INH}$ pull-up resistance	R_{UP1}	Measurement cct 4	40	100	250	$k\Omega$
	R_{UP2}		2	4	15	$M\Omega$
Feedback resistance	R_f	Measurement cct 5	80	200	500	$k\Omega$
Built-in capacitance	C_G	Design value, determined by the internal wafer pattern	16	18	20	pF
	C_D		16	18	20	

5 V operation: $V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -40$ to 85 °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, $V_{DD} = 4.5$ V, $I_{OH} = 16$ mA	4.0	4.2	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, $V_{DD} = 4.5$ V, $I_{OL} = 16$ mA	–	0.3	0.4	V
Output leakage current	I_Z	Q: Measurement cct 2, $\overline{INH} = \text{LOW}$, $V_{DD} = 5.5$ V, $V_{OH} = V_{DD}$	–	–	10	μA
		Q: Measurement cct 2, $\overline{INH} = \text{LOW}$, $V_{DD} = 5.5$ V, $V_{OL} = V_{SS}$	–	–	10	
HIGH-level input voltage	V_{IH}	$\overline{INH}$	$0.7V_{DD}$	–	–	V
LOW-level input voltage	V_{IL}	$\overline{INH}$	–	–	$0.3V_{DD}$	V
Current consumption	I_{DD}	Measurement cct 3, load cct 1, $\overline{INH} = \text{open}$, $C_L = 50$ pF, $f = 30$ MHz	5010CL1	–	15	mA
			5010CL2	–	9	
			5010CL3	–	6	
			5010CL4	–	5	
Standby current	I_{ST}	Measurement cct 6, $\overline{INH} = \text{LOW}$	–	–	10	μA
$\overline{INH}$ pull-up resistance	R_{UP1}	Measurement cct 4	40	100	250	$k\Omega$
	R_{UP2}		1	2	8	$M\Omega$
Feedback resistance	R_f	Measurement cct 5	80	200	500	$k\Omega$
Built-in capacitance	C_G	Design value, determined by the internal wafer pattern	16	18	20	pF
	C_D		16	18	20	

Switching Characteristics

5010×N× series

3 V operation: $V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -10$ to 70 °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $C_L = 15$ pF, $0.1V_{DD}$ to $0.9V_{DD}$	–	3.0	6.0	ns
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $C_L = 15$ pF, $0.9V_{DD}$ to $0.1V_{DD}$	–	3.0	6.0	ns
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 3.0$ V, $T_a = 25$ °C, $C_L = 15$ pF, $f = 30$ MHz	40	–	60	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 3.0$ V, $T_a = 25$ °C, $C_L = 15$ pF	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

1. Determined by the lot monitor.

5010×N×, ×K× series

5 V operation (5010×N×): $V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -40$ to 85 °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$	$C_L = 15$ pF	–	2.0	4.0	ns
	t_{r2}		$C_L = 50$ pF	–	4.0	8.0	
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$	$C_L = 15$ pF	–	2.0	4.0	ns
	t_{f2}		$C_L = 50$ pF	–	4.0	8.0	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 5.0$ V, $T_a = 25$ °C, $C_L = 50$ pF, $f = 30$ MHz		45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 5.0$ V, $T_a = 25$ °C, $C_L = 15$ pF		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns

1. Determined by the lot monitor.

5 V operation (5010AN2, AN3, AN4, BN2, BN3, BN4, ×K×): $V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -40$ to 85 °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r3}	Measurement cct 6, load cct 2, $C_L = 15$ pF, $0.4V$ to $2.4V$	–	1.5	3.0	ns
Output fall time	t_{f3}	Measurement cct 6, load cct 2, $C_L = 15$ pF, $2.4V$ to $0.4V$	–	1.5	3.0	ns
Output duty cycle ¹	Duty	Measurement cct 6, load cct 2, $V_{DD} = 5.0$ V, $T_a = 25$ °C, $C_L = 15$ pF, $f = 30$ MHz	45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 2, $V_{DD} = 5.0$ V, $T_a = 25$ °C, $C_L = 15$ pF	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

1. Determined by the lot monitor.

5010×H× series

3 V operation: $V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -10$ to 70 °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $C_L = 15$ pF, $0.1V_{DD}$ to $0.9V_{DD}$	–	15	30	ns
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $C_L = 15$ pF, $0.9V_{DD}$ to $0.1V_{DD}$	–	15	30	ns
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 3.0$ V, $T_a = 25$ °C, $C_L = 15$ pF, $f = 16$ MHz	40	–	60	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 3.0$ V, $T_a = 25$ °C, $C_L = 15$ pF	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

1. Determined by the lot monitor.

5 V operation: $V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -40$ to 85 °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$	$C_L = 15$ pF	–	5	10	ns
	t_{r2}		$C_L = 50$ pF	–	13	26	
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$	$C_L = 15$ pF	–	5	10	ns
	t_{f2}		$C_L = 50$ pF	–	13	26	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 5.0$ V, $T_a = 25$ °C, $C_L = 15$ pF, $f = 30$ MHz		45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 5.0$ V, $T_a = 25$ °C, $C_L = 15$ pF		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns

1. Determined by the lot monitor.

5010CL× series

3 V operation: $V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -20$ to 80 °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t _{r1}	Measurement cct 6, load cct 1, 0.1V _{DD} to 0.9V _{DD}	C _L = 15 pF	–	2.0	4.0	ns
	t _{r4}		C _L = 30 pF	–	3.0	6.0	
Output fall time	t _{f1}	Measurement cct 6, load cct 1, 0.9V _{DD} to 0.1V _{DD}	C _L = 15 pF	–	2.0	4.0	ns
	t _{f4}		C _L = 30 pF	–	3.0	6.0	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, V _{DD} = 3.0 V, Ta = 25 °C, C _L = 15 pF, f = 30MHz		45	–	55	%
Output disable delay time ²	t _{PLZ}	Measurement cct 7, load cct 1, V _{DD} = 3.0 V, Ta = 25 °C, C _L = 15 pF		–	–	100	ns
Output enable delay time ²	t _{PZL}			–	–	100	ns

1. Determined by the lot monitor.

2. Oscillator stop function is built-in. When $\overline{INH}$ goes LOW, normal output stops. When $\overline{INH}$ goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

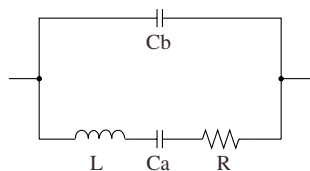
5 V operation: $V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -40$ to 85 °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t _{r1}	Measurement cct 6, load cct 1, 0.1V _{DD} to 0.9V _{DD}	C _L = 15 pF	–	1.5	3.0	ns
	t _{r2}		C _L = 50 pF	–	4.0	8.0	
Output fall time	t _{f1}	Measurement cct 6, load cct 1, 0.9V _{DD} to 0.1V _{DD}	C _L = 15 pF	–	1.5	3.0	ns
	t _{f2}		C _L = 50 pF	–	4.0	8.0	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, V _{DD} = 5.0 V, Ta = 25 °C, C _L = 50 pF, f = 30MHz		40	–	60	%
Output disable delay time ²	t _{PLZ}	Measurement cct 7, load cct 1, V _{DD} = 5.0 V, Ta = 25 °C, C _L = 15 pF		–	–	100	ns
Output enable delay time ²	t _{PZL}			–	–	100	ns

1. Determined by the lot monitor.

2. Oscillator stop function is built-in. When $\overline{INH}$ goes LOW, normal output stops. When $\overline{INH}$ goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

Current consumption and Output waveform with NPC's standard crystal



f (MHz)	R (Ω)	L (mH)	Ca (fF)	Cb (pF)
30	17.2	4.36	6.46	2.26

FUNCTIONAL DESCRIPTION

Standby Function

AH, AK, AN, BH, BK, BN, DN series

When $\overline{\text{INH}}$ goes LOW, the output on Q becomes high impedance, but internally the oscillator does not stop.

CL series

When $\overline{\text{INH}}$ goes LOW, the oscillator stops and the oscillator output on Q becomes high impedance.

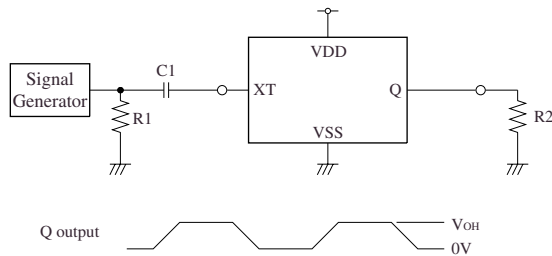
Version	$\overline{\text{INH}}$	Q	Oscillator
AH, AK, AN, BH, BK, BN, DN series	HIGH (or open)	Any f_O , $f_O/2$, $f_O/4$ or $f_O/8$ output frequency	Normal operation
	LOW	High impedance	Normal operation
CL series	HIGH (or open)	Any f_O , $f_O/2$, $f_O/4$ or $f_O/8$ output frequency	Normal operation
	LOW	High impedance	Stopped

Power-save Pull-up Resistance (CL series only)

The $\overline{\text{INH}}$ pull-up resistance changes in response to the input level (HIGH or LOW). When $\overline{\text{INH}}$ goes LOW (standby state), the pull-up resistance becomes large to reduce the current consumption during standby.

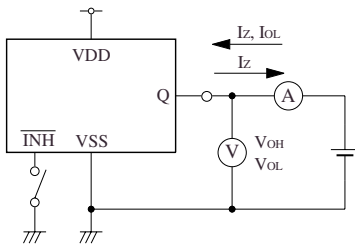
MEASUREMENT CIRCUITS

Measurement cct 1

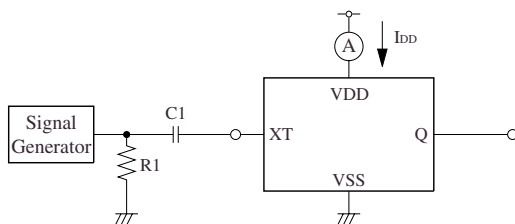


2.0V_{P-P}, 10MHz sine wave input signal (3V operation)
 3.5V_{P-P}, 10MHz sine wave input signal (5V operation)
 C1 : 0.001μF
 R1 : 50Ω
 R2 : 263Ω (5010×N×, ×K×/ 3V operation)
 245Ω (5010×N×, ×K×/ 5V operation)
 1050Ω (5010×H×/ 3V operation)
 975Ω (5010×H×/ 5V operation)
 275Ω (5010CL×/ 3V operation)
 250Ω (5010CL×/ 5V operation)

Measurement cct 2

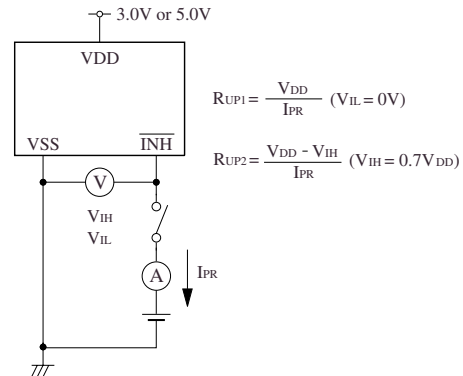


Measurement cct 3

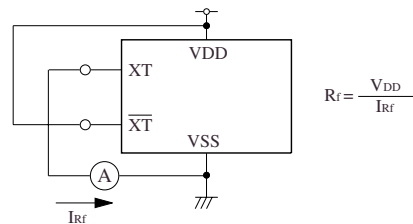


2.0V_{P-P}, 30MHz sine wave input signal (3V operation)
 3.5V_{P-P}, 30MHz sine wave input signal (5V operation)
 C1 : 0.001μF
 R1 : 50Ω

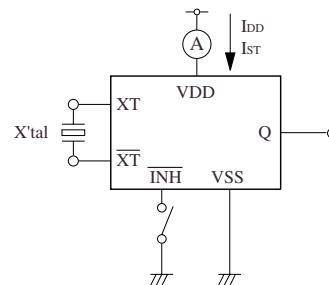
Measurement cct 4



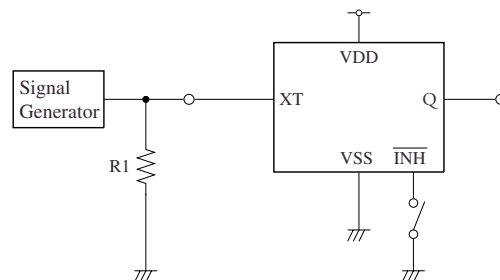
Measurement cct 5



Measurement cct 6

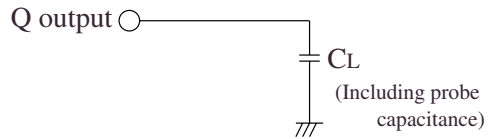


Measurement cct 7



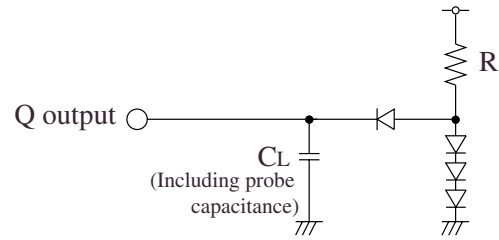
R1 : 50Ω

Load cct 1



$C_L = 15\text{pF}$: DUTY, I_{DD} , t_{r1} , t_{f1}
 $C_L = 30\text{pF}$: t_{r4} , t_{f4}
 $C_L = 50\text{pF}$: t_{r2} , t_{f2}

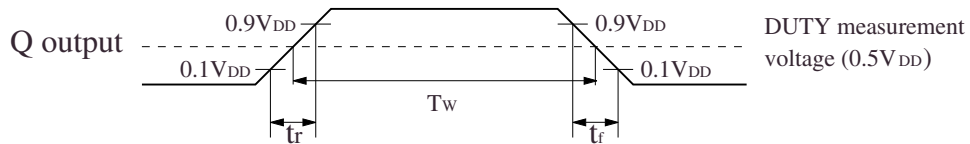
Load cct 2



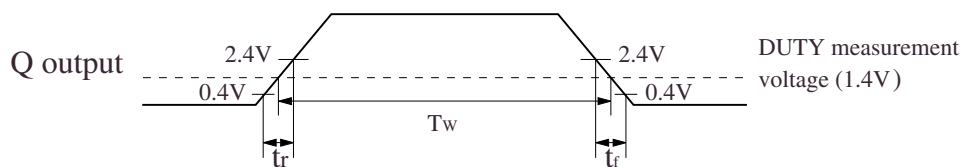
$C_L = 15\text{pF}$: DUTY, I_{DD} , t_{r3} , t_{f3}
 $R = 400\Omega$

Switching Time Measurement Waveform

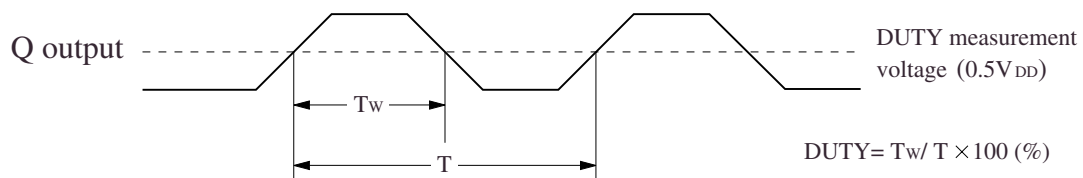
Output duty level (CMOS)



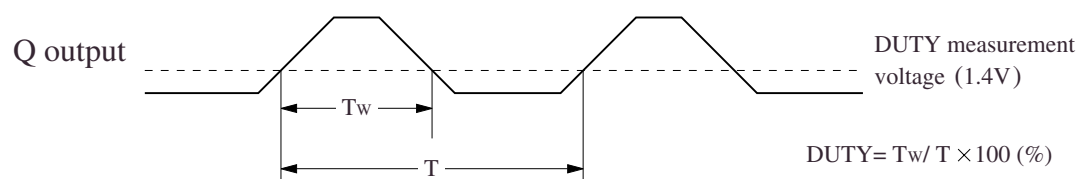
Output duty level (TTL)



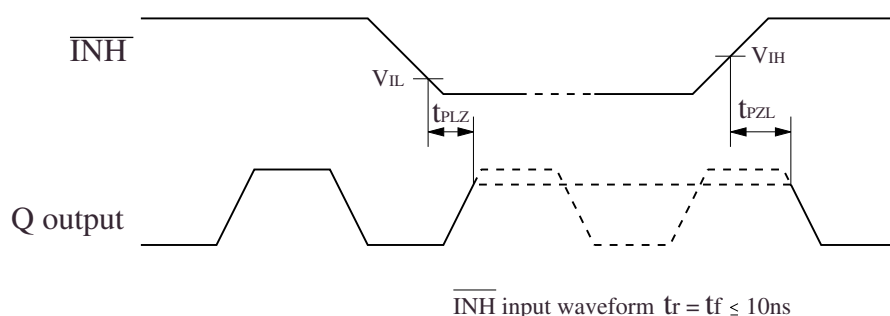
Output duty cycle (CMOS)



Output duty cycle (TTL)



Output Enable/Disable Delay



Note (CL series only) : when the device is in standby, the oscillator stops. When standby is released, the oscillator starts and stable oscillator output occurs after a short delay.

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