NIPPON PRECISION CIRCUITS INC.

SM8707D/E

Clock Generator for DVD Players

OVERVIEW

The SM8707D/E is a clock generator IC that generates 3 clocks with 6 outputs from a 27MHz master clock for application in DVD players. The SM8707D/E also supports the 44.1kHz and 48kHz sampling frequencies, and the sampling frequency can be switched while the device is operating.

FEATURES

- 27MHz master clock
  (internal PLL reference clock)
- Generated clocks
  - SM8707D
    - Video system output: 27MHz
    - Audio system output: 512fs
      384fs (fs = 44.1kHz)
      768fs (fs = 48kHz)
    - Signal processor system output:
      16.9344MHz, 33.8688MHz
  - SM8707E
    - Video system output: 27MHz
    - Audio system output: 512fs
    - Signal processor system output:
      33.8688MHz
- Sampling frequency fs: 44.1/48kHz
- Low jitter output
  - SM8707D
    : 20ps typ. (1-sigma, video system output)
    : 70ps typ. (1-sigma, audio and signal processor system outputs)
  - SM8707E
    : 20ps typ. (1-sigma, video system output)
    : 55ps typ. (1-sigma, audio and signal processor system outputs)
- Supply voltage: 3.3V ± 0.3V
- 16-pin VSOP package

APPLICATIONS

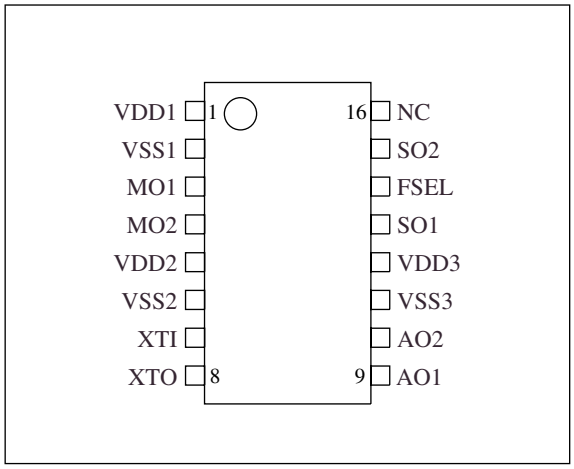
- DVD players
- DVD car navigation system

ORDERING INFORMATION

Device	Package
SM8707DV	16-pin VSOP
SM8707EV	

PINOUT

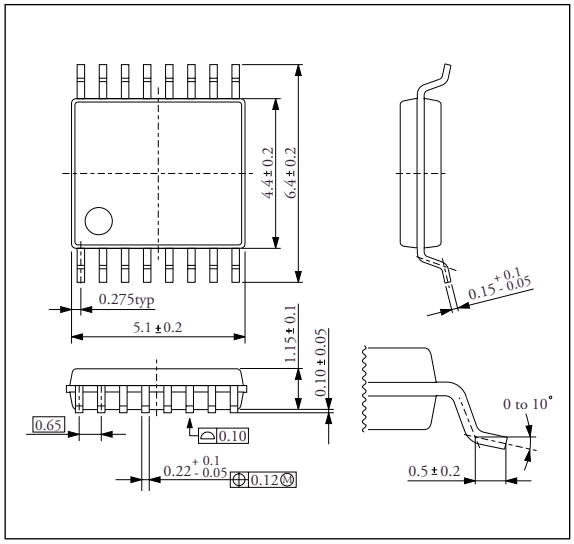
(Top view)



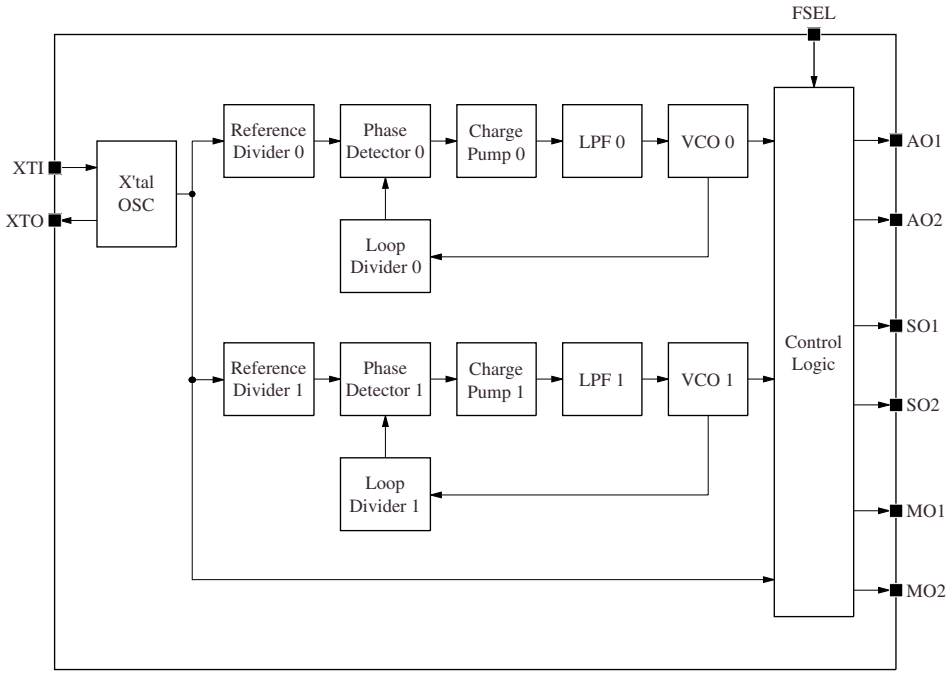
PACKAGE DIMENSIONS

(Unit: mm)

Weight: 0.07g



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	VDD1	–	Supply 1 for digital block
2	VSS1	–	Ground 1 for digital block
3	MO1	O	Video system output 1 (27MHz fixed)
4	MO2	O	Video system output 2 (27MHz fixed)
5	VDD2	–	Supply 2 for analog block
6	VSS2	–	Ground 2 for analog block
7	XTI	I	Crystal oscillator connection or external clock input
8	XTO	O	Crystal oscillator connection
9	AO1	O	<SM8707D> Audio system output 1 (384fs/768fs output) FSEL = LOW, fs = 48kHz: 768fs FSEL = HIGH, fs = 44.1kHz: 384fs <SM8707E> Audio system output 1 (512fs output)
10	AO2	O	Audio system output 2 (512fs output)
11	VSS3	–	Ground 3 for digital block
12	VDD3	–	Supply 3 for digital block
13	SO1	O	<SM8707D> Signal processor system output 1 (16.9344MHz fixed) <SM8707E> Signal processor system output 1 (33.8688MHz fixed)
14	FSEL	I	<SM8707D> Sampling frequency select FSEL = LOW: fs = 48kHz FSEL = HIGH: fs = 44.1kHz (with internal pull-up resistor, Schmitt-trigger input) <SM8707E> Sampling frequency select FSEL = HIGH: fs = 48kHz FSEL = LOW: fs = 44.1kHz (with internal pull-up resistor, Schmitt-trigger input)
15	SO2	O	Signal processor system output 2 (33.8688MHz fixed)
16	NC	–	No connection (leave pin open circuit or connect to VDD)

Note: Unless otherwise noted, VDD applies to VDD1, VDD2, and VDD3. Similarly, VSS applies to VSS1, VSS2, and VSS3.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD1} , V_{DD2} , V_{DD3}		– 0.3 to + 6.5	V
Supply voltage deviation	$V_{DD1} - V_{DD2}$, $V_{DD1} - V_{DD3}$, $V_{DD2} - V_{DD3}$		± 0.1	V
Input voltage range	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D		165	mW
Storage temperature range	T_{stg}		– 55 to + 125	°C

Recommended Operating Conditions

$V_{SS} = V_{SS1} = V_{SS2} = V_{SS3} = 0V$ unless otherwise noted.

SM8707D

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage ranges[1, 2, 3]	V_{DD1} , V_{DD2} , V_{DD3}		+ 3.0	–	+ 3.6	V
Output load capacitance 1	C_{L1}	MO1, MO2, SO1, SO2 outputs	–	–	25	pF
Output load capacitance 2	C_{L2}	AO1, AO2 outputs	–	–	15	pF
Master clock frequency	f_{XTAL}	When using crystal oscillator	–	27.0000	–	MHz
Operating temperature range	T_{opr}		– 40	–	+ 85	°C

1. The supply voltage is defined relative to V_{SS} = 0V
2. The supply voltages applied on VDD1, VDD2, and VDD3 should be derived from a common supply source.
3. If the supply voltages on VDD1, VDD2, and VDD3 are from different sources, they should be applied simultaneously. The SM8707D may be damaged if the supply voltage timing is different.

SM8707E

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage ranges[1, 2, 3]	V_{DD1} , V_{DD2} , V_{DD3}		+ 3.0	–	+ 3.6	V
Output load capacitance 1	C_{L1}	MO1 output	–	–	40	pF
Output load capacitance 2	C_{L2}	MO2 output	–	–	25	pF
Output load capacitance 3	C_{L3}	SO1, SO2, AO1, AO2 outputs	–	–	15	pF
Master clock frequency	f_{XTAL}	When using crystal oscillator	–	27.0000	–	MHz
Operating temperature range	T_{opr}		– 10	–	+ 75	°C

1. The supply voltage is defined relative to V_{SS} = 0V
2. The supply voltages applied on VDD1, VDD2, and VDD3 should be derived from a common supply source.
3. If the supply voltages on VDD1, VDD2, and VDD3 are from different sources, they should be applied simultaneously. The SM8707E may be damaged if the supply voltage timing is different.

DC Electrical Characteristics

SM8707D: f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 40 to + 85 °C unless otherwise noted.

SM8707E: f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 10 to + 75 °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	V_{DD} = 3.3V, Ta = 25°C, fs = 48kHz, Crystal oscillator, no load on all outputs	–	35	45	mA
HIGH-level input voltage	V_{IH}	FSEL, XTI, V_{DD} = 3.3V	0.8 V_{DD}	–	–	V
LOW-level input voltage	V_{IL}		–	–	0.2 V_{DD}	V
HIGH-level input current[1]	I_{IH1}	FSEL, V_{IN} = V_{DD}	–	–	1	µA
LOW-level input current[1]	I_{IL1}	FSEL, V_{IN} = 0V	– 100	–	–	µA
HIGH-level input current	I_{IH2}	XTI, V_{IN} = V_{DD}	–	–	40	µA
LOW-level input current	I_{IL2}	XTI, V_{IN} = 0V	– 40	–	–	µA
HIGH-level output voltage	V_{OH}	All outputs excluding XTO, I_{OH} = – 2mA	V_{DD} – 0.4	–	–	V
LOW-level output voltage	V_{OL}	All outputs excluding XTO, I_{OL} = 2mA	–	–	0.4	V

1. FSEL pin has Schmitt-trigger input and built-in pull-up resistor.

AC Electrical Characteristics

SM8707D

f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 40 to + 85 °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
External input clock frequency[1]	f_{XTI}	XTI, applies to external clock input use only	–	27.0000	–	MHz
Output clock rise time[2]	t_r	MO1, MO2, SO1, SO2, C_L = 25 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	ns
		AO1, AO2, C_L = 15pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	
Output clock fall time[2]	t_f	MO1, MO2, SO1, SO2, C_L = 25pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	ns
		AO1, AO2, C_L = 15pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	
Output clock jitter[3]	t_{jitter} (1-sigma)	MO1, MO2, Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	–	20	–	ps
		SO1, SO2, Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	–	70	–	
		AO1, AO2, Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	–	70	–	
Output clock duty cycle[2]	Dt	MO1, MO2, SO1, SO2, Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	45	50	55	%
		AO1, AO2, Ta = 25°C, C_L =15 pF, V_O = 0.5V_{DD}	45	50	55	
Settling time[2]	t_S	All outputs excluding XTO	–	–	1	µs
Power-up time[2,4]	t_P	All outputs excluding XTO	–	1	5	ms

1. When using an external clock input, the XTI duty should be 50% with 3.3V clock signal amplitude level. The input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.
2. The numeric values are measured values obtained using the circuit in Figure 1 and the NPC standard evaluation board.
3. The numeric values are measured values obtained using the circuit in Figure 2 and the NPC standard evaluation board.
4. This is the time, after the supply is turned ON from the OFF state, until the output clock reaches ± 0.1% of the specified frequency.

SM8707E

f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 10 to + 75 °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
External input clock frequency[1]	f_{XTI}	XTI, applies to external clock input use only	–	27.0000	–	MHz
Output clock rise time[2]	t_r	MO1, C_L = 40 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	ns
		MO2, C_L = 25 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	
		SO1, SO2, AO1, AO2, C_L = 15pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	
Output clock fall time[2]	t_f	MO1, C_L = 40pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	ns
		MO2, C_L = 25pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	
		SO1, SO2, AO1, AO2, C_L = 15pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	
Output clock jitter[3]	t_{jitter} (1-sigma)	MO1, Ta = 25°C, C_L = 40pF, V_O = 0.5V_{DD}	–	20	–	ps
		MO2, Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	–	20	–	
		SO1, SO2, AO1, AO2, Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	–	55	–	
Output clock duty cycle[2]	Dt	MO1, Ta = 25°C, C_L = 40pF, V_O = 0.5V_{DD}	45	50	55	%
		MO2, Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	45	50	55	
		SO1, SO2, AO1, AO2, Ta = 25°C, C_L =15 pF, V_O = 0.5V_{DD}	45	50	55	
Settling time[2]	t_S	AO1, AO2	–	–	1	µs
Power-up time[2,4]	t_P	All outputs excluding XTO	–	1	5	ms

1. When using an external clock input, the XTI duty should be 50% with 3.3V clock signal amplitude level. The input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.
2. The numeric values are measured values obtained using the circuit in Figure 1 and the NPC standard evaluation board.
3. The numeric values are measured values obtained using the circuit in Figure 2 and the NPC standard evaluation board.
4. This is the time, after the supply is turned ON from the OFF state, until the output clock reaches ± 0.1% of the specified frequency.

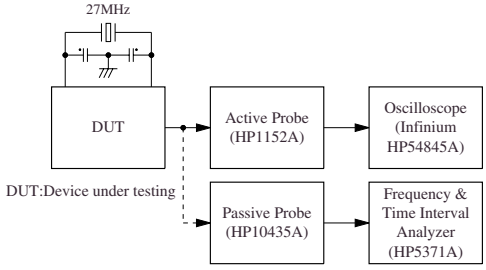


Figure 1. Measurement circuit 1

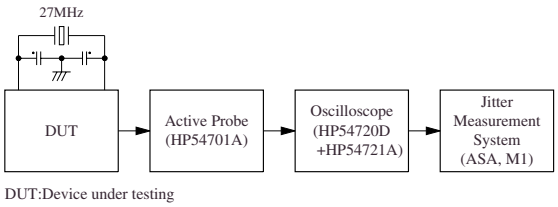


Figure 2. Measurement circuit 2

FUNCTIONAL DESCRIPTION

27MHz Master Clock

The SM8707D/E 27MHz master clock circuit is configured, as shown in Figure 3, with the crystal oscillator element connected between XTI (pin 7) and XTO (pin 8).

Alternatively, the 27MHz master clock can be supplied from an external master clock input on XTI, as shown in Figure 4.

If an external input clock on XTI is used, it is recommended that the frequency be 27.0000MHz, with 50% duty, and 3.3V voltage amplitude level.

Furthermore, when using an external clock input, the input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.

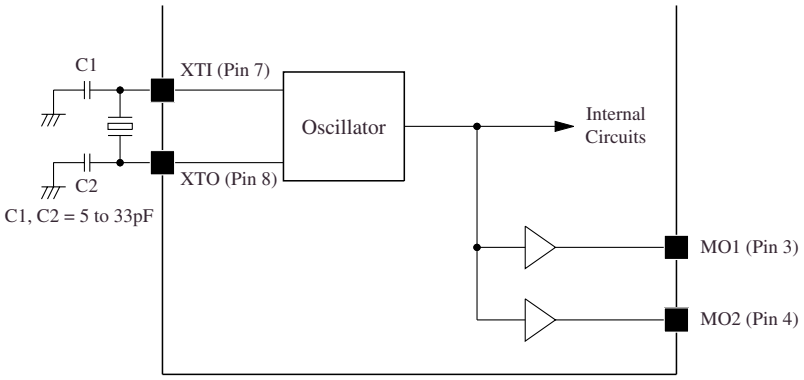


Figure 3. Crystal oscillator connection

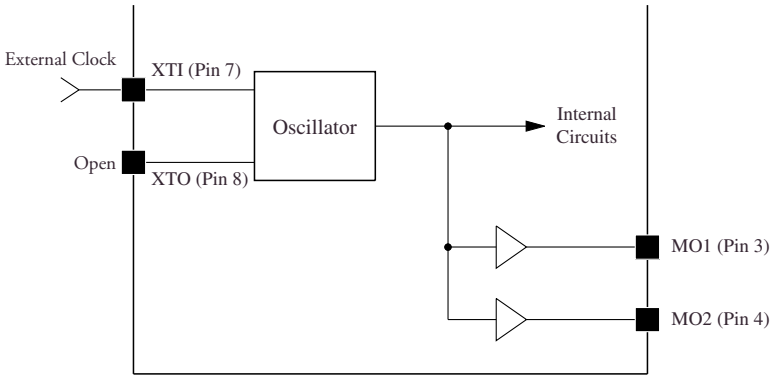


Figure 4. External clock input

Sampling Frequency and Output Clock Frequency

SM8707D

The SM8707D sampling frequency fs can be switched between 44.1kHz when FSEL (pin 14) is HIGH, and 48kHz when FSEL is LOW. The audio output (AO1) is a 384fs frequency clock when FSEL is HIGH (fs = 44.1kHz), and 768fs frequency clock when FSEL is LOW (fs = 48kHz) where fs is determined by the setting on FSEL. The audio output (AO2) is a 512fs frequency clock. In addition, the signal processor output (SO1 and SO2) is a 16.9344MHz, 33.8688MHz frequency clock derived from the master clock. And the video output (MO1 and MO2) is a 27MHz frequency clock, identical to the master clock.

The SM8707D possible output clock frequencies are shown in Table 1.

Table 1. Sampling frequency and output clock frequency (27.0000MHz master clock frequency)

FSEL (Pin 14)	Sampling frequency fs [kHz]	Output clock frequency [MHz]					
		AO1 (Pin 9)	AO2 (Pin 10)	SO1 (Pin 13)	SO2 (Pin 15)	MO1 (Pin 3)	MO2 (Pin 4)
HIGH	44.1	16.9344 (384fs)	22.5792 (512fs)	16.9344	33.8688	27.0000	27.0000
LOW	48	36.8640 (768fs)	24.5760 (512fs)	16.9344	33.8688	27.0000	27.0000

SM8707E

The SM8707E sampling frequency fs can be switched between 44.1kHz when FSEL (pin 14) is LOW, and 48kHz when FSEL is HIGH. The audio output (AO1 and AO2) is a 512fs frequency clock, where fs is determined by the setting on FSEL. In addition, the signal processor output (SO1 and SO2) is a 33.8688MHz frequency clock derived from the master clock. And the video output (MO1 and MO2) is a 27MHz frequency clock, identical to the master clock.

The SM8707E possible output clock frequencies are shown in Table 2.

Table 2. Sampling frequency and output clock frequency (27.0000MHz master clock frequency)

FSEL (Pin 14)	Sampling frequency fs [kHz]	Output clock frequency [MHz]					
		AO1 (Pin 9)	AO2 (Pin 10)	SO1 (Pin 13)	SO2 (Pin 15)	MO1 (Pin 3)	MO2 (Pin 4)
LOW	44.1	22.5792 (512fs)	22.5792 (512fs)	33.8688	33.8688	27.0000	27.0000
HIGH	48	24.5760 (512fs)	24.5760 (512fs)	33.8688	33.8688	27.0000	27.0000

Spike Noise Prevention Function

The SM8707D/E has a spike noise prevention circuit that operates to prevent the generation of spike noise on the audio output clocks when the sampling frequency is switched using FSEL.

The AO1 and AO2 output clock state before and after FSEL changes state is shown in Figure 5 and Figure 6.

When FSEL is switched LOW to HIGH or switched HIGH to LOW, the spike noise circuit stops the AO1 and AO2 outputs for a maximum of 1µs to prevent output spike noise, and then the outputs change to reflect the FSEL setting.

SM8707D

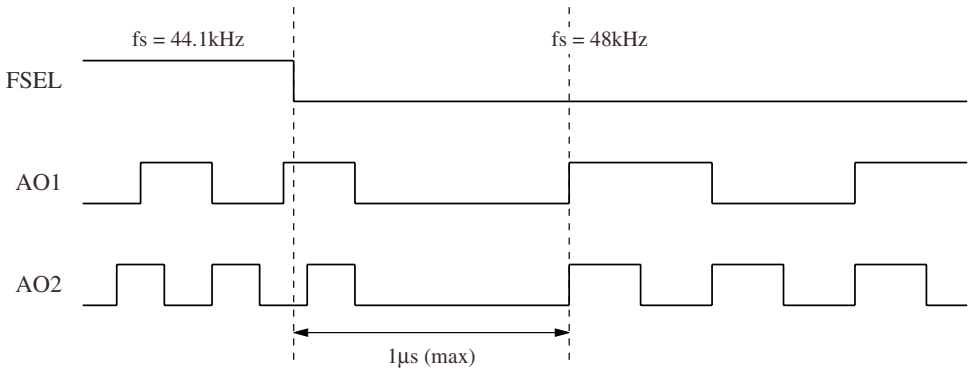


Figure 5. Spike noise prevention circuit timing
(sampling frequency fs = 44.1kHz → fs = 48kHz switching example)

SM8707E

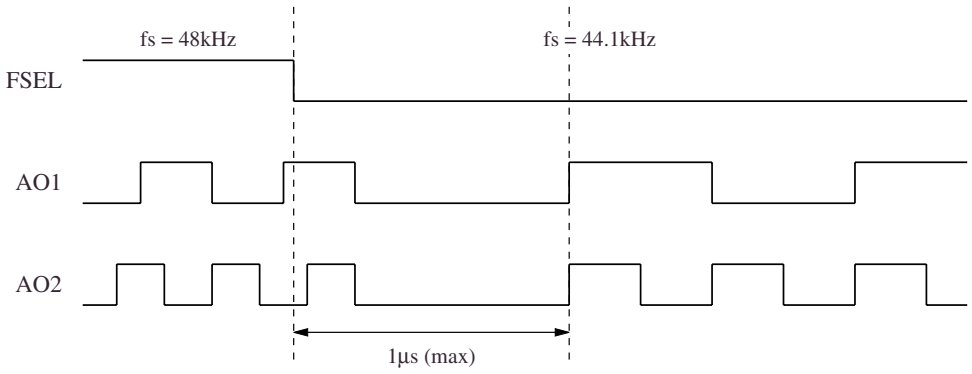


Figure 6. Spike noise prevention circuit timing
(sampling frequency fs = 48kHz → fs = 44.1kHz switching example)

Sampling Frequency Switching Settling Time

The clock output response timing when the sampling frequency fs is switched using FSEL is shown in Figure 7 and Figure 8. The SM8707D/E has a built-in spike noise prevention circuit. As a result, the AO1 and AO2 outputs stop for a fixed interval after FSEL changes state, as described above, and hence the settling time t_s for the audio output clock when switching the sampling frequency is 1µs maximum.

SM8707D

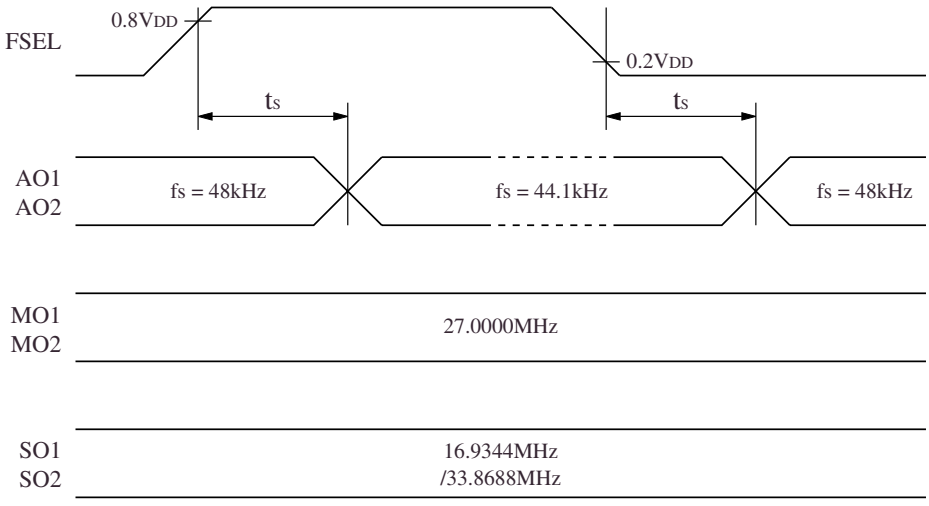


Figure 7. Output signal switching timing

SM8707E

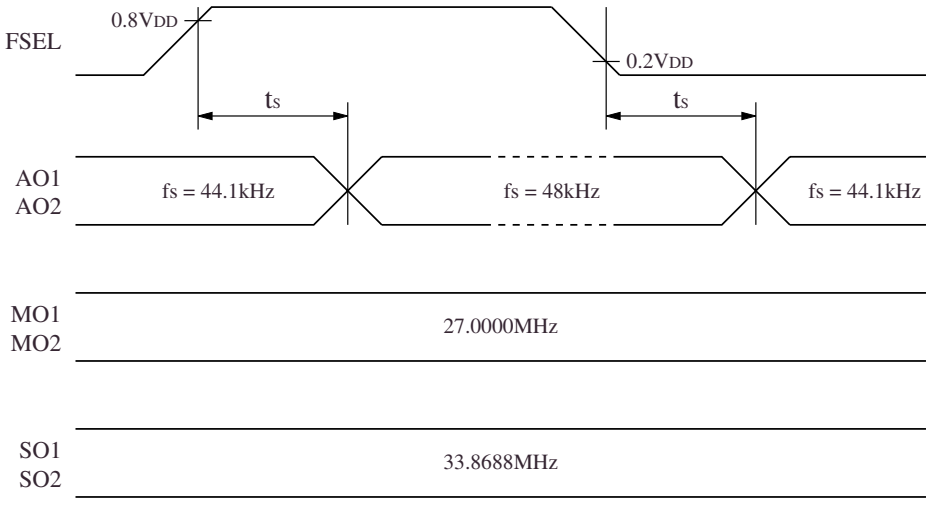


Figure 8. Output signal switching timing

NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, Fukuzumi 2-chome, Koto-ku,
Tokyo 135-8430, Japan
Telephone: +81-3-3642-6661
Facsimile: +81-3-3642-6698
http://www.npc.co.jp/
Email: sales@npc.co.jp

NC0107AE 2001.06