SM561

Spread Spectrum Clock Generator

Features

- 54 to 166 MHz Operating Frequency Range
- Wide (9) Range of Spread Selections
- Accepts Clock and Crystal Inputs
- Low Power Dissipation
  3.3V = 165 mw. (Fin = 120 MHz)
- Frequency Spread Disable Function
- Center Spread Modulation
- Low Cycle-to Cycle Jitter
- 8-pin SOIC package

Applications

- High Resolution VGA Controllers
- LCD Panels and Monitors
- Work Stations and Servers

Benefits

- Peak EMI reduction by 8 to 16dB
- Fast Time to Market
- Cost Reduction

General Description

The CYPRESS SM561 is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high-speed digital electronic systems.

The SM561 uses a Cypress proprietary Phase-Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and frequency modulate the input frequency of the reference clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies of Clock (SSCLK) is greatly reduced.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements and time to market without degrading the system performance.

The SM561 is a very simple and versatile device to use. The frequency and spread % range is selected by programming S0 and S1digital inputs. These inputs use three (3) logic states including High (H), Low (L) and Middle (M) logic levels to select one of the 9 available Frequency Modulation and Spread % ranges. Refer to Table 2 for programming details.

The SM561 is intended for use with applications with a reference frequency in the range of 54 to 166 MHz.

A wide range of digitally selectable spread percentages is made possible by using Three-Level (High, Low and Middle) logic at the S0 and S1 digital control inputs.

The output spread (frequency modulation) is symmetrically centered on the input frequency.

Spread Spectrum Clock Control (SSCC) function enables or disables the frequency spread and is provided for easy comparison of system performance during EMI testing.

The SM561 is available in an 8-pin SOIC package with a 0 to 70°C operating temperature range.

Refer to the SM560 datasheet for operation at frequencies from 27 to 108 MHz.

Block Diagram

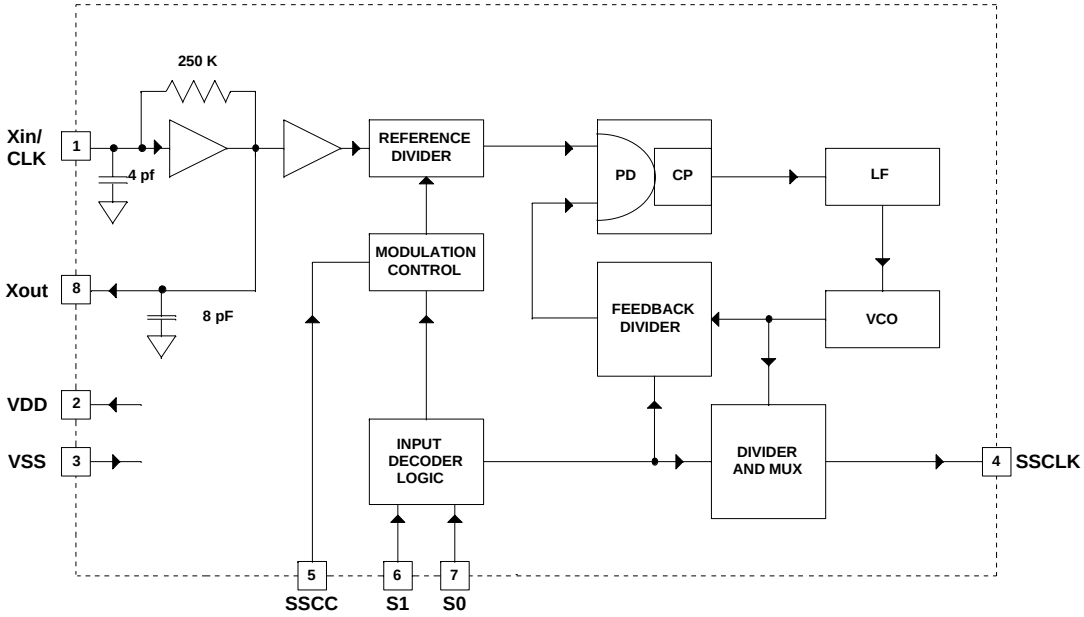


Figure 1. Block Diagram

Ordering Information

Part No.	Package	Operating Temperature Range
SM561BZ	8 Pin SOIC	0 to 70°C

Pin Configuration

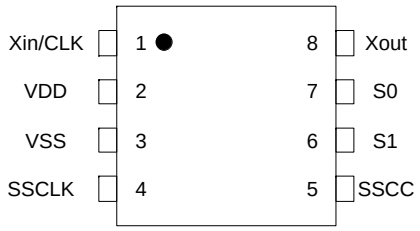


Figure 2. Pin Configuration

Pin Description

Pin #	Symbol	Type	Description
1	Xin/CLK	I	Clock or Crystal connection input. Refer to the Table-2 and 3 for input frequency range selection.
2	VDD	P	Positive power supply.
3	GND	P	Power supply ground.
4	SSCLK	O	Modulated clock output.
5	SSCC	I	Spread Spectrum Clock Control (Enable/Disable) function. SSCG function is enabled when input is high and disabled when input is low. This pin is pulled high internally.
6	S1	I	Tri-Level Logic input control pin used to select Frequency and Bandwidth. Frequency/Bandwidth selection and Tri-Level Logic programming details can be found on page 4.
7	S0	I	Tri-Level Logic input control pin used to select Frequency and Bandwidth. Frequency/Bandwidth selection and Tri-Level Logic programming details can be found on page 4.
8	Xout	O	Oscillator output pin connected to crystal. Leave this pin unconnected If an external clock drives Xin/CLK.

Table 1. Pin Description

Frequency and Spread % Selection

54– 108 MHz (Low Range)

Input Frequency (MHz)	S1=M S0=M	S1=M S0=0	S1=1 S0=0	S1=0 S0=0	S1=0 S0=M
54– 60	3.6	3.1	2.6	2.1	1.8
60 – 70	3.5	3.0	2.5	2.0	1.7
70 – 80	3.3	2.8	2.4	1.9	1.6
80 - 100	3.0	2.5	2.1	1.7	1.4
100 - 108	2.6	2.3	1.9	1.5	1.3

Select the Frequency and Spread % desired and then set S1, S0 as indicated.

108 – 166 MHz (High Range)

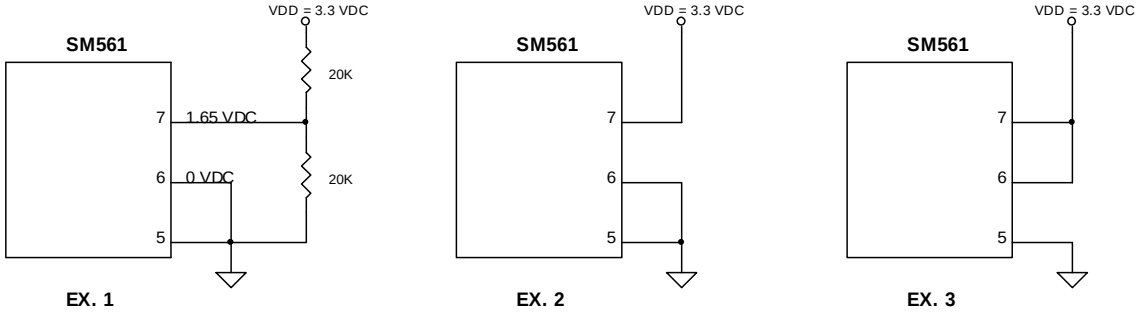
Input Frequency (MHz)	S1=1 S0=M	S1=0 S0=1	S1=1 S0=1	S1=M S0=1
108 – 120	2.3	1.7	1.1	0.9
120 – 130	2.3	1.7	1.1	0.9
130 – 140	2.3	1.7	1.1	0.9
140 – 150	2.2	1.6	1.1	0.9
150 - 166	2.1	1.5	1.0	0.8

Select the Frequency and Spread % desired and then set S1, S0 as indicated.

Table 2. Frequency and Spread % Selection

Tri-Level Logic

With binary logic, 4 states can be programmed with 2 control lines where as Tri-Level Logic can program 9 logic states using 2 control lines. Tri-Level Logic in the SM561 is implemented by defining a third logic state in addition to the standard logic “1” and “0”. Pin 6 and 7 of the SM561 recognize a logic state by the voltage applied to the respective pin. These states are defined as “0” (Low), “M” (Middle) and “1” (One). Each of these states have a defined voltage range that is interpreted by the SM561 as a “0”, “M” or “1” logic state. Refer to table 5 for voltage ranges for each logic state. By using two equal value resistors (typically 20K) the “M” state can be easily programmed. Pins 6 or 7 can be tied directly to ground or VDD for Logic “0” or “1” respectively.
See examples below;



Absolute Maximum Ratings

Supply Voltage(AVDD or DVDD): +6V
AVDD - DVDD: +/-300mV
AGND - DGND: +/-300mV
Junction Temperature (10-sec. soldering): +300°C

Operating Temperature: 0 to 70°C
Storage Temperature: -65 to +150°C

Note: Operation at any Absolute Maximum Rating is not implied.

DC Electrical Characteristics

Test Conditions: VDD=3.3V, Temp. =25°C and CL (Pin 4) =15pF, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Power Supply Range	2.97	3.3	3.63	V	+/- 10 %
VINH	Input High Voltage	0.85VDD	VDD	VDD	V	S0 and S1 only.
VINM	Input Middle Voltage	0.40VDD	0.50VDD	0.60VDD	V	S0 and S1 only.
VINL	Input Low Voltage	0.0	0.0	0.15VDD	V	S0 and S1 only.
VOH1	Output High Voltage	2.4	-	-	V	IOH = 6 ma
VOH2	Output High Voltage	2.0	-	-	V	IOH = 20 ma
VOL1	Output Low Voltage	-	-	0.4	V	IOH = 6 ma
VOL2	Output Low Voltage	-	-	1.2	V	IOH = 20 ma
Cin1	Input Capacitance	3	4	5	pF	Xin/CLK (Pin 1)
Cin2	Input Capacitance	6	8	10	pF	Xout (Pin 8)
Cin2	Input Capacitance	3	4	5	pF	S0, S1, SSCC (Pins 7,6,5)
IDD1	Power Supply Current	-	35	45	ma	FIN = 65 MHz
IDD2	Power Supply Current	-	50	55	ma	Fin = 166 MHz

Table 5

Electrical Timing Characteristics

Test Conditions: VDD=3.3V, T=25°C and CL=15pF unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
ICLKFR	Input Clock Frequency Range	54		166	MHz	VDD = 3.30V
Trise	Clock Rise Time (Pin 4)	1.2	1.4	1.6	ns	SSCLK1 @ 0.4 – 2.4V
Tfall	Clock Fall Time (Pin 4)	1.2	1.4	1.6	ns	SSCLK1 @ 0.4 – 2.4V
DTYin	Input Clock Duty Cycle	20	50	80	%	XIN/CLK (Pin 1)
DTYout	Output Clock Duty Cycle	45	50	55	%	SSCLK1 (Pin 4)
JCC1	Cycle-to-Cycle Jitter	-	125	175	ps	Fin < 140 MHz
JCC2	Cycle-to-Cycle Jitter	-	150	200	ps	Fin > 140 MHz

Table 6

SSCG Theory of Operation

The SM561 is a Phase Lock Loop (PLL) type clock generator using a proprietary Cypress design. By precisely controlling the bandwidth of the output clock, the SM561 becomes a Low EMI clock generator. The theory and detailed operation of the SM561 will be discussed in the following sections.

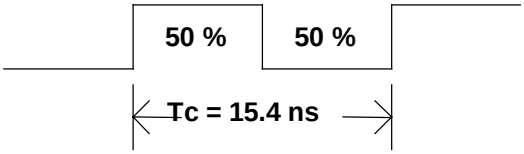
EMI

All digital clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50 %. Because of this 50/50-duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e.; 3rd, 5th, 7th etc. It is possible to reduce the amount of energy contained in the fundamental and odd harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for Electro-Magnetic Interference (EMI). Conventional methods of reducing EMI have been to use shielding, filtering, multi-layer PCB's etc. The SM561 uses the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q.

SSCG

SSCG uses a patented technology of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle to cycle. The SM561 takes a narrow band digital reference clock in the range of 27 - 108 MHz and produces a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to a clock when SSCG is applied, consider a 65 MHz clock with a 50 % duty cycle. From a 65 MHz clock we know the following;

Clock Frequency = fc = 65 MHz.
Clock Period = Tc = 1/65 MHz = 15.4 ns.



If this clock is applied to the Xin/CLK pin of the SM561, the output clock at pin 4 (SSCLK) will be sweeping back and forth between two frequencies. These two frequencies, F1 and F2, are used to calculate to total amount of spread or bandwidth applied to the reference clock at pin 1. As the clock is making the transition from f1 to f2, the amount of time and sweep waveform play a very important role in the amount of EMI reduction realized from an SSCG clock.

The modulation domain analyzer is used to visualize the sweep waveform and sweep period. Figure 3 shows the modulation profile of a 65 MHz SSCG clock. Notice that the actual sweep waveform is not a simple sine or sawtooth waveform. Figure 4 is a scan of the same SSCG clock using a spectrum analyzer. In this scan you can see a 6.48 dB reduction in the peak RF energy when using the SSCG clock.

Modulation Rate

Spectrum Spread Clock Generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (Fmax) and minimum frequency of the clock (Fmin) determine this band of frequencies. The time required to transition from Fmin to Fmax and back to Fmin is the period of the Modulation Rate, Tmr. Modulation Rates of SSCG clocks are most commonly referred to in terms of frequency or Fmod = 1/Tmod.

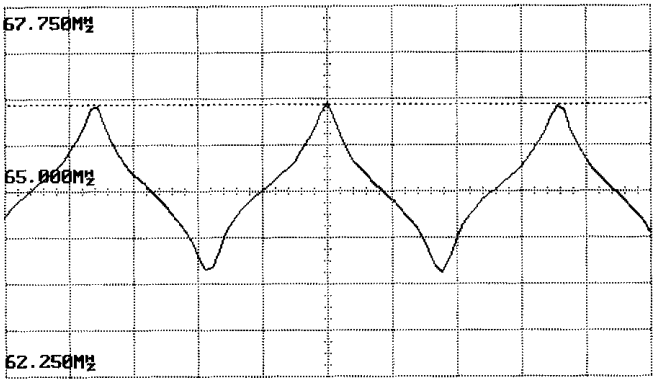
The input clock frequency, Fin, and the internal divider count, Cdiv, determine the Modulation Rate. In some SSCG clock generators, the selected range determines the internal divider count. In other SSCG clocks, the internal divider count is fixed over the operating range of the part. The SM560 and SM561 have a fixed divider count, as listed below;

Device	**Cdiv**	
SM560	1166	(All Ranges)
SM561	2332	(All Ranges)

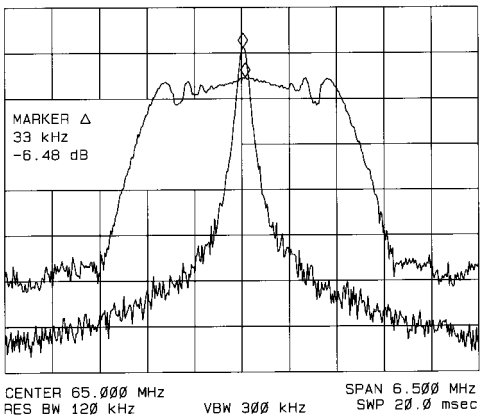
Example:

Device = SM560
Fin = 65 MHz
Range = S1 = 1, S0 = 0
Then;

Modulation Rate = Fmod = 65 MHz/2332 = 27.9 kHz.



Modulation Profile



Spectrum Analyzer

Figure 3. SSCG Clock, SM561, Fin = 65 MHz

SM561 Application Schematic

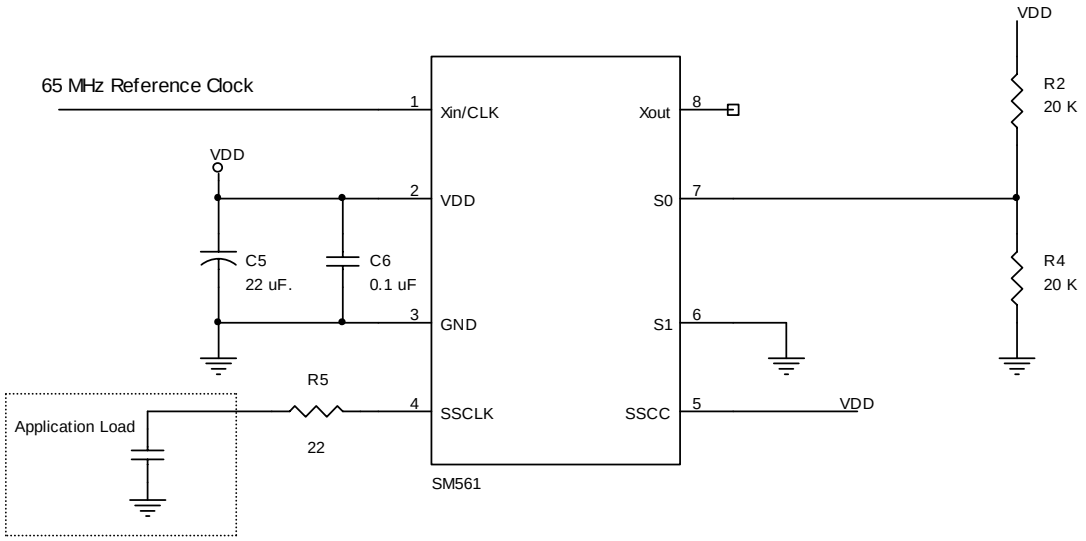
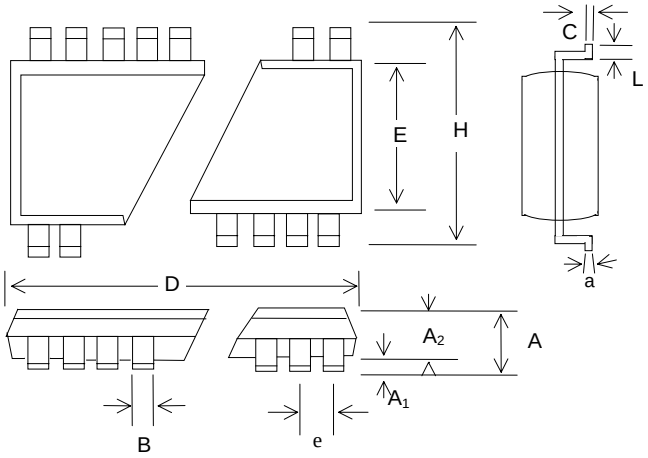


Figure 4. Application Schematic

The schematic in figure 2 above demonstrates how the SM561 is configured in a typical application. This application is using a 65 MHz reference clock connected to pin 1. Because an external reference clock is used, pin 8 (Xin/CLK) is left unconnected.

Figure 2 also demonstrates how to properly use the tri-level logic employed in the SM561. Notice that resistors R2 and R4 create a voltage divider that places VDD/2 on pin 7 to satisfy the voltage requirement for an “M” state. With this configuration, the SM561 will produce an SSCG clock that is at a center frequency of 65 MHz. Referring to table 2, range “0, M” at 65 MHz will generate a modulation profile that has a 1.7 % peak to peak spread.

8 PIN SOIC Packing Drawing



8 Pin SOIC Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.053	-	0.069	1.35	-	1.75
A_1	0.004	-	0.010	0.10	-	0.25
A2	0.047	-	0.059	1.20	-	1.50
B	0.013	-	0.020	0.33	-	0.51
C	0.007	-	0.010	0.19	-	0.25
D	0.189	-	0.197	4.80	-	5.00
E	0.150	-	0.157	3.80	-	4.00
e	0.050 BSC			1.27 BSC		
H	0.228	-	0.244	5.80	-	6.20
L	0.016	-	0.050	0.40	-	1.27
a	0º	-	8º	0º	-	8º

Notes:

NOTICE

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