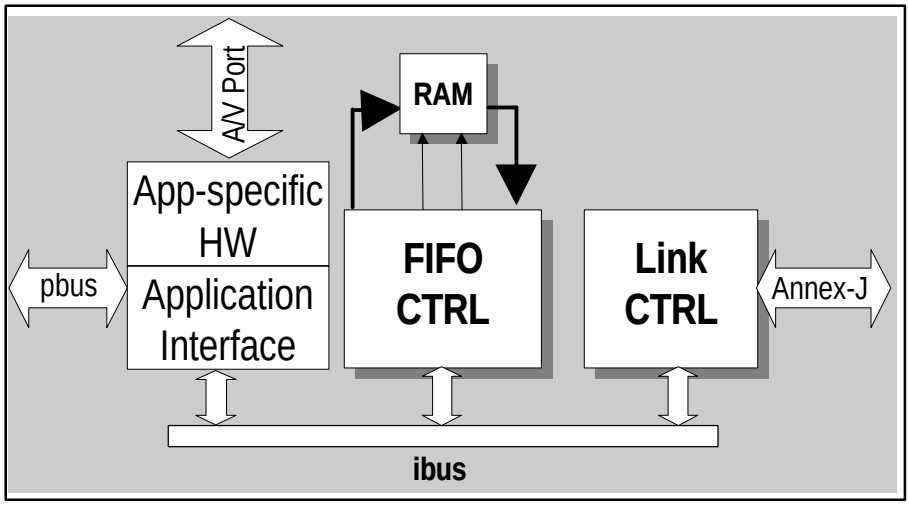
SL770
IEEE1394a Audio/Video Link Layer

Bus Interface

D A T A S H E E T



SL770 Audio/Video Link Layer for IEEE 1394a Block Diagram

Major product features:

- Compliant with IEEE 1394a Link Layer specification
- Supports IEC 61883 standard
- Supports transfer rates of 100, 200 or 400 Mbps
- Works with the FlexFire SL730 Mixed Signal PHY Layer core or with commercial PHY chips
- Based on parameterized building blocks that can be configured for a wide range of A/V applications
- Performs jitter compensation
- Supports CIP, PCR and FCP
- Provides full Link Layer support plus some Transaction Layer and Bus Management functions

IEEE 1394a Audio/Video Link Layer

What is IEEE-1394?

IEEE-1394, known as FireWire, is a high-speed digital serial interface bus standard that allows video and audio consumer devices to communicate quickly, reliably and inexpensively with a PC and with each other. Scalable performance and the support of both asynchronous and isochronous transfers makes FireWire an ideal technology for a wide variety of peripherals and applications including disk controllers, digital cameras, audio/video devices, small networks, high speed printers and entertainment equipment.

FlexFire™ Architecture

The FlexFire architecture is based on a set of parameterized building blocks that can be quickly and easily configured to support a wide range of 1394 applications.

The FlexFire 1394a core family includes general purpose and application-specific cores for both Link Layer and Physical Layer (PHY) Layer controllers.

SL770 Audio/Video Link Layer Controller

The SL770 provides the interface to connect MPEG-2/DVC devices to the high speed 1394 serial bus, at speeds up to 400 Megabits per second.

The core can be used in set-top boxes, digital TV/VCRs, video PCs or any application that requires MPEG-2/DVC format isochronous data transfer according to the IEC 61883 specification.

The SL770 Audio / Video Link Layer core can be integrated with the SL730 Mixed Signal Physical Layer(PHY) core for a single-chip 1394a audio/video solution.

The SL770 is available in synthesizable RTL and includes a comprehensive testbench and validation suite, synthesis scripts and user documentation.

Ibus

The internal blocks of the SL755 are connected via a common bus called Ibus (see Figure 1). Ibus is a multiple-master, multiple-target bus that operates in the 50MHz Sclk (from the PHY) regime. It employs a three-phase pipeline protocol; comprising arbitration, addressing and data transfer phases. The data transfer path is 32-bits wide and supports only full quadlet read and write transfers. Therefore, Ibus provides a 200 MBs, low latency communication path between the SL755 internal units.

Link Controller Block

The internal link controller block provides a low level link protocol implementation. It connects packet parameters from the FIFOs, formats them into packets and coordinates with the PHY to transmit them. It also receives packets from the PHY, performs standard compliant format checking and reporting and, when appropriate, extracts parameters from the packets and stores them into the FIFOs. This block also includes four quadlets worth of buffering to accommodate for latency in access to the Ibus.

FIFO Controller Block

The FIFO Controller block provides the smart pointer management needed by the SL770 FIFOs. The FIFO RAM, which is external to the SL770, is used as the actual FIFO storage. FIFOs are implemented within this RAM storage by using re-circulating pointers.

By employing the FIFO controller, the SL770 supports run time location and sizing of the FIFOs within the FIFO RAM and run-time programmability of the FIFO types. Streaming mode, group input and group output FIFO types are supported.

Additional Features:

- Supports asynchronous and isochronous transfers including multi-channel isochronous receive
- Cycle master capable
- 8, 16, and 32-bit application bus interfaces to common embedded processors
- Dynamically configurable FIFO functionality, number and size
- Detects late packet and sequence errors
- Performs 32-bit CRC generation and error detection

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