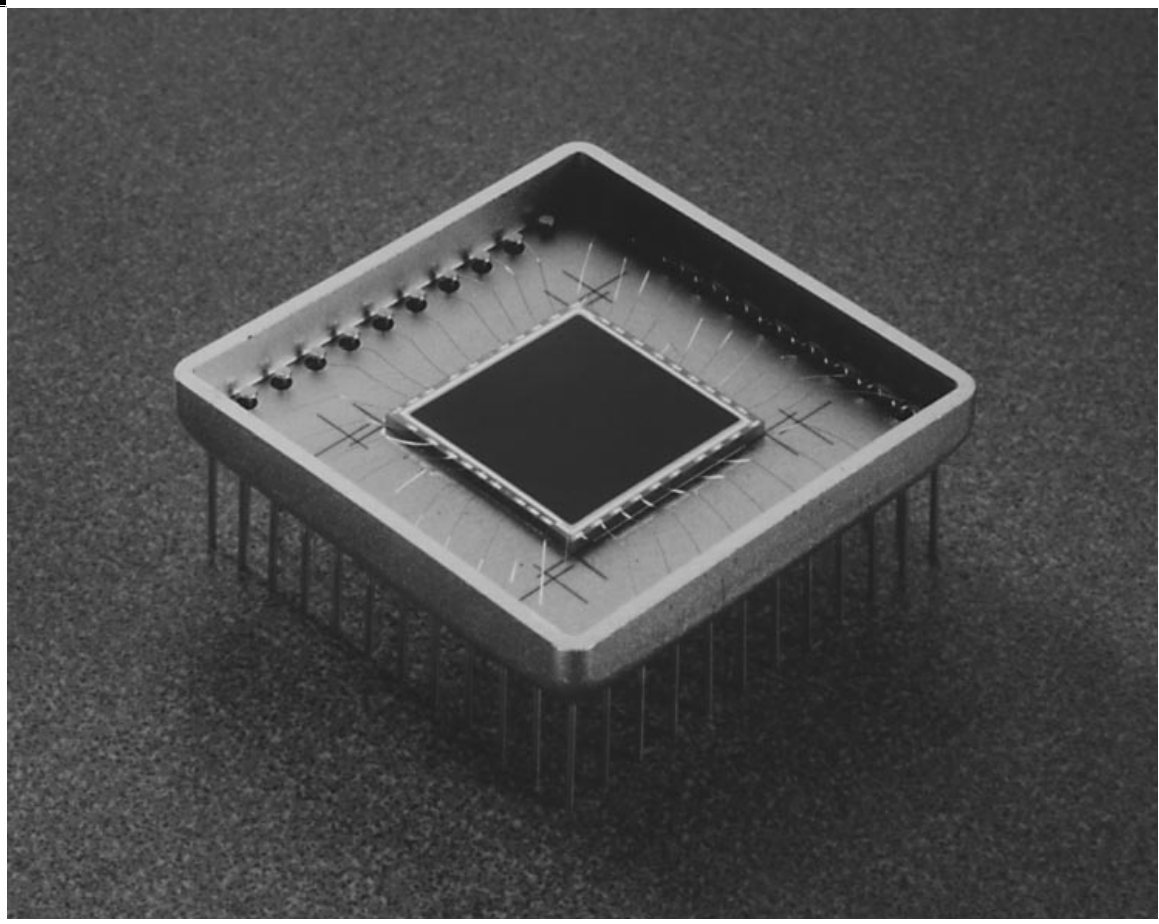

512 x 512 pixel format (24μm square)

■

Front-illuminated or thinned, back-illuminated versions

■

Unique thinning and Quantum Efficiency enhancement processes

■

Excellent QE from IR to UV

■

Anti-reflection coating for visible region

■

Mechanical Rigidity

■

MPP technology

■

Low dark current

■

Excellent charge transfer efficiency (CTE) at all signal levels

■

On-chip output MOSFET for low noise

■

Wide dynamic range

■

Selectable bi-directional read-out of imaging data

■

Applications include astronomy, machine vision, medical imaging, and scientific imaging

SITe 512 x 512 Scientific-Grade CCD

SI-502A CCD Imager: *Ideal for applications with small-area imaging requirements*

General Description

The SI-502A CCD Imager is a silicon charge-coupled device designed to efficiently image scenes at low light levels from UV to near infrared. The sensor is fabricated as a 512 x 512 pixel, full frame area imager that utilizes a buried channel, three level polysilicon gate process. Features include a buried channel with a mini-channel for high transfer efficiency, multi-phase pinned (MPP) operation for low dark current, and lightly doped drain (LDD) output amplifier for low read noise. The device is available in a front illuminated version or a thinned, back-illuminated version that provides superior quantum efficiency.

SITe's unique thinning and back surface enhancement process provides increased blue and UV response in a flat and fully supported die. It is more rugged and easier to uniformly cool than fragile edge-supported chips. The CCD imager is mounted in a non-hermetic metal package without a window.

Functional Description

Imaging Area

As shown in the functional diagram, Figure 2, the imaging area of the SI-502A consists of 512 columns, each of which contains 512 picture elements (pixels). Each pixel measures 24µm x 24µm. The columns are isolated from each other by channel-stop regions.

Three levels of polysilicon are used to fabricate the three gate electrodes which form the basic CCD cell (pixel). All of the pixels in a given row are defined by the same three gates. Corresponding gates in each row are connected in parallel at both edges of the array. The clock signals used to drive the imaging area gates are brought in from both edges of the array, thus increasing the rate at which the rows can be shifted. By applying suitable voltages to the three gate phases (see timing section) potential wells are formed at each pixel site. If an optical image is focused onto the array, an electronic analog of the scene will be collected as photoelectronic charge in the potential wells.

To read out a frame, the signal charge collected in the imaging array is transferred along the columns a row at a time to one of the two serial registers and from there to an autput amplifier. Charge can be transferred to either amplifier; however, the array cannot be read out through both amplifiers simultaneously.

Serial Registers

The functional diagram (Figure 2) illustrates the relationship between the imaging array and the serial registers. The charge collected in the imaging section is transferred through the transfer gate into the serial register phase 1 gate. The serial register has one pixel for each column in the imaging array, plus 15 extra pixels at each end for a total of 527. The extra pixels serve as a dark reference and ensure that the signal chain is stabilized when the image data is received at the output.

Each serial register is provided with an input diode and a sampling gate to allow elecrical injection of charge into the device (generally used only for testing purposes). The output of both serial registers is terminated in a summing well, a DC-biased last gate (which serves to decouple the serial clock pulses from the output node), and an output amplifier. The summing well is a separately clocked gate equal in charge capacity to the other serial gates. It can be used to provide on-chip (noiseless) charge summing of consecutive serial pixels. Similarly, it is possible to sum pixels into the serial register by performing repetitive parallel transfers with the serial clocks fixed. In this manner, it is possible to collect and detect as one pixel the sum of the charge in sub-arrays of the imaging section, provided that the sum is less than the full well charge. The well capacity of a pixel in the serial register is greater than that of a parallel pixel to ensure that the CTE remains high.

Output Structure

The imager has two output MOSFETs that are located at opposite corners of the device at the ends of the extended serial registers. Figure 1 presents a schematic diagram of the output configuration.

In operation, a positive pulse is applied to the reset gate (RGx). This sets the potential of the floating diffusion to the potential applied to the reset transistor drain (RDx). The reset gate voltage is then turned off and the output node (the floating diffusion) is isolated from the rest of the circuit. Charge from the serial pixel is then transferred to the output node on the falling edge of the summing well (SWx) clock signal. The addition of charge on the output node causes a change in the voltage on the gate of the output MOSFET. This change in voltage is sensed at OUTx.

Timing

Typical clock timing for the SITe SI-502A CCD Imager is shown in Figure 3, which gives the sequence for moving charge packets through the serial register and parallel array. A minimum of 527 serial shifts (5l2 pixels in the image and 15 in the extended register) are required to clear the serial register after a parallel line transfer or integration period. A minimum of 512 parallel shifts are required to read out a complete image frame. The sequence for a typical full-frame readout is shown in figure 4.

The parallel timing of figure 3 is for MPP operation where all of the parallel gates are held low during the integration period. When operating in the non-MPP mode, P1, P2, or both P1 and P2 are held high during integration. For full MPP operation, the parallel gates are all held low during serial readout as well as the integration period.

The serial and reset gates may be clocked continuously during the integration period to drain off charge collected in the serial register. The input sample gate may be tied to the lower serial clock rail if it is not used or clocked as shown when an electrical input is required. Typical timing for the operation of an external signal clamp and sample charge detection circuit is included in the output timing diagrams for reference.

Multi-Phase Pinned (MPP) Operation

The multi-phase pinned (MPP) technology used on the SI-502A allows the device to be operated totally inverted during integration and line readout. The main advantage of this mode of operation is that it results in much lower dark current than conventional CCD operation. Other

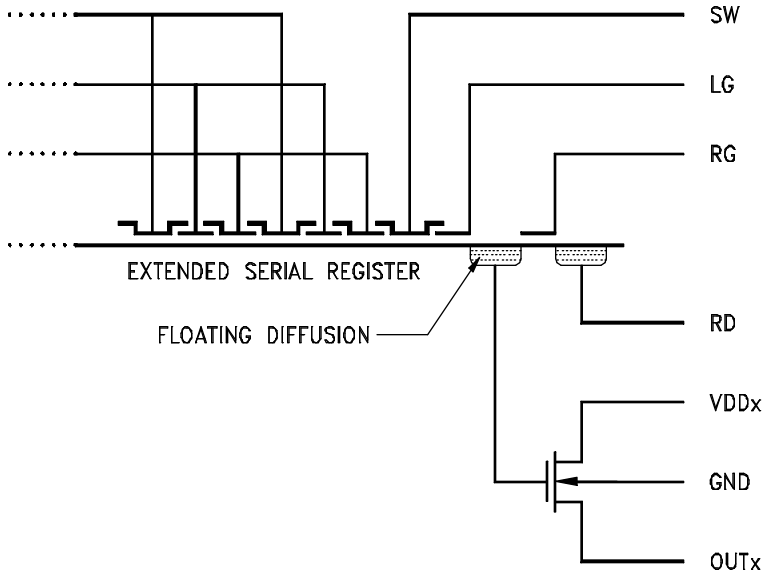

FIGURE 1 *Output Structure*

advantages of MPP operation are the reduction of the surface residual image defect and a greater tolerance for ionizing radiation environments.

To operate the CCD in the MPP mode, the array clocks are biased sufficiently negative to invert the n-buried channel and “pin” the surface potential beneath each phase to the substrate potential. This allows holes from the p+ channel stop to populate the surface states at the silicon/silicon dioxide interface, minimizing surface dark current generation.

To enable all three phases of the array to be inverted and still retain well capacity, MPP devices have an extra implant under the phase 3 gates. During integration, this creates a potential barrier between each pixel allowing signal charge to accumulate under phases 1 and 2 at each pixel site. A consequence of this mode of operation is that the total well capacity is about 50 percent of that of a standard CCD if all the parallel clocks are operated at the same voltages. A larger well capacity can be obtained if phase 3 parallel clock high rail is operated about 3 volts higher than the phase 1 and phase 2 high rails.

DEVICE SPECIFICATIONS

Measured at -45 deg. C, unless otherwise indicated, 45 kpixels/sec and standard voltages using a dual slope CDS circuit (8 µs integration time)

	Minimum	*Typical*	*Maximum*
Format		512 x 512 pixels	
Pixel Size		24 µm x 24 µm	
Imaging Area		12.3 mm x 12.3 mm	
Dark current (MPP), *20° C equivalent*		50 pa/cm^2	70 pa/cm^2
Readout noise Front		5 electrons	7 electrons
Back		7 electrons	9 electrons
Full Well signal	300,000 electrons	350,000 electrons	
Output gain	1.0 µV/ electron	1.5 µV/ electron	
CTE per pixel	0.99995	0.99999	

TABLE 1 *Device specifications, SI-502A*

DC OPERATING CONDITIONS

TERMINAL	ITEM	MIN	STANDARD	MAX	UNIT
VDDx	OUTPUT DRAIN SUPPLY	22	24	26	V
RDx	RESET DRAIN	13	15	17	V
LGx	LAST GATE	-4	-2	0	V
SUB,PKG	SUB & PACKAGE CONNECTION		0		V
ID	INPUT DIODE SUPPLY	5	15	26	V
GNDx	MOSFET GROUND REFERENCE		0		V
OUTx	MOSFET OUTPUT (LOAD)	5	20	50	kohms

GATE TO SUBSTRATE VOLTAGES

TERMINAL	ITEM		MIN	STANDARD	MAX	P TO P MAX	UNIT
RGx	RESET GATE	LOW RAIL	-5	0	5	20	V
		HIGH RAIL	5	12	15		V
S#x	SERIAL GATE	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V
SWx	SUMMING WELL	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V
P#x	PARALLEL GATE	LOW RAIL	-10	-9	0	20	V
		HIGH RAIL	0	4	10		V
P3		HIGH RAIL	0	7	10		V
TGx	TRANSFER GATE	LOW RAIL	-10	-9	0	20	V
		HIGH RAIL	0	7	10		V
SG	SAMPLE GATE	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V

TABLE 2 *DC operating conditions and clock voltages,* SI-502A

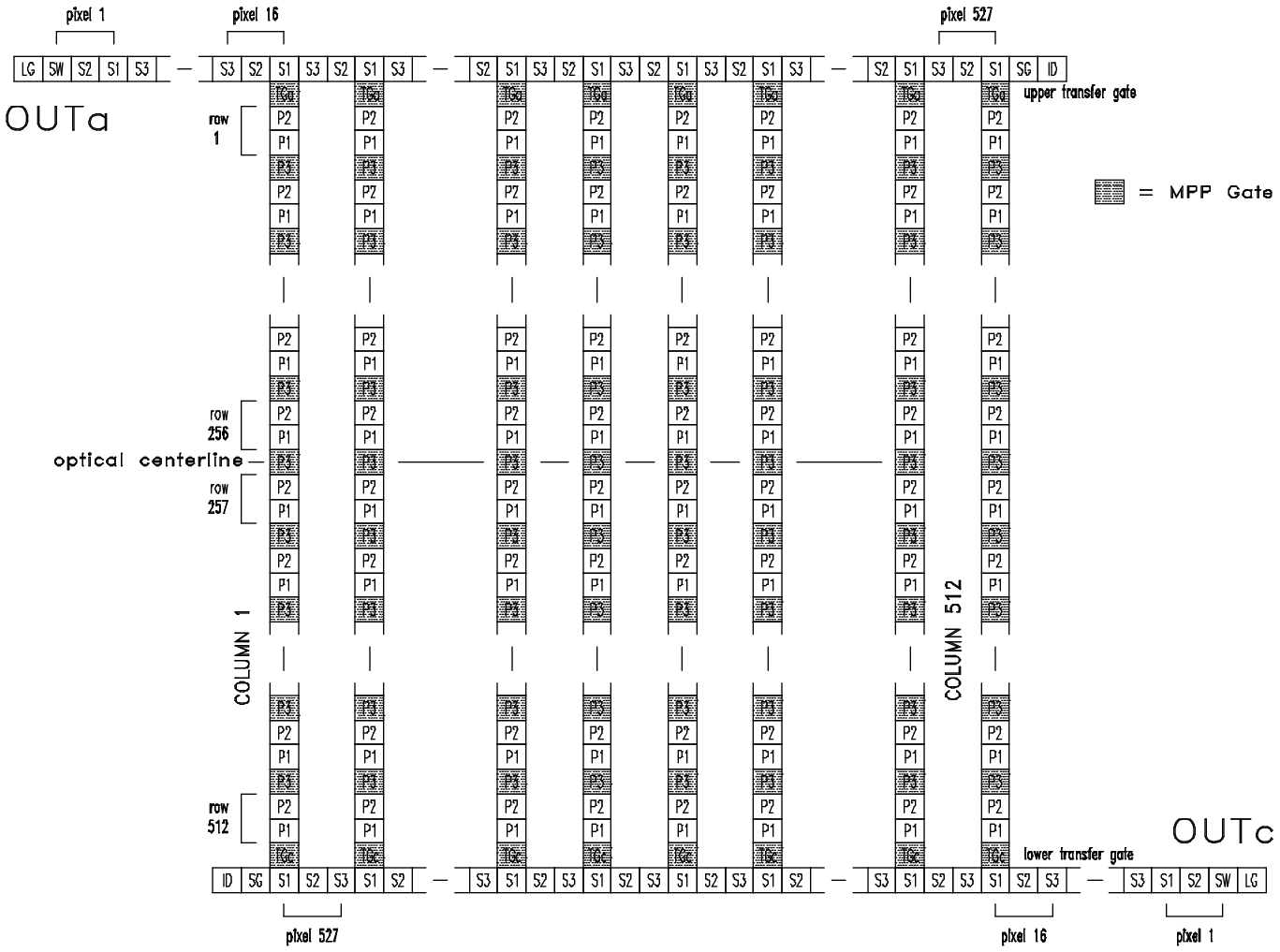

FIGURE 2 SI-502A *functional diagram*

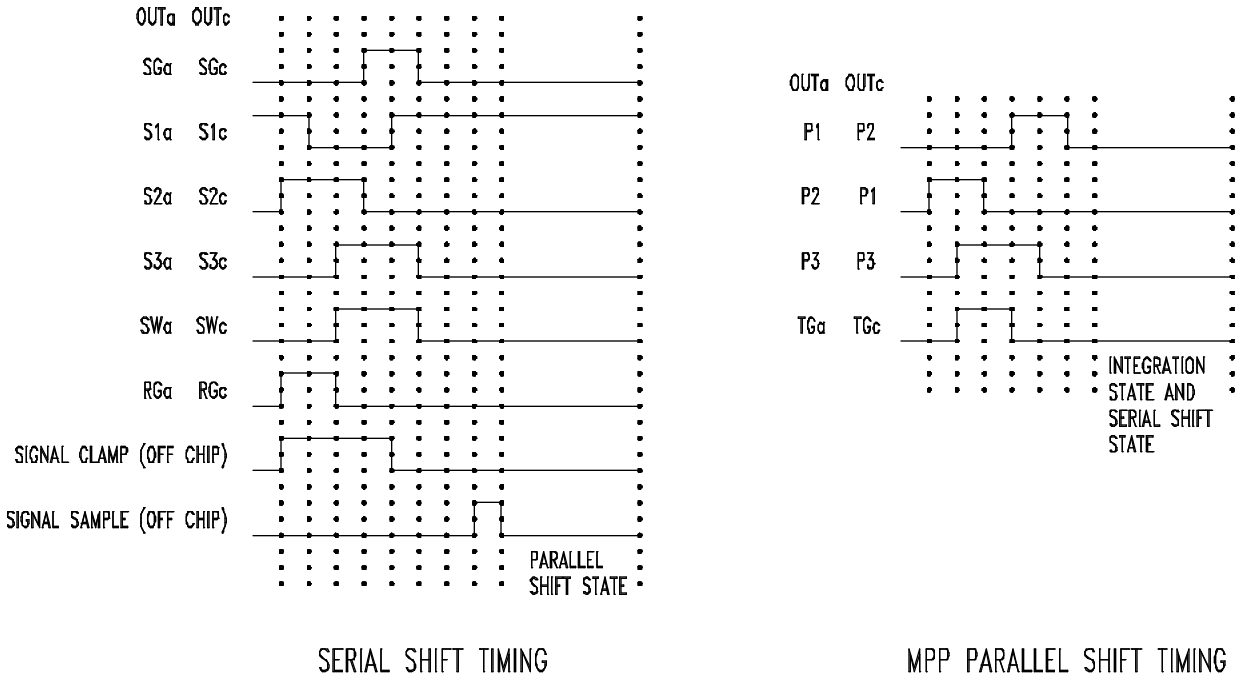

FIGURE 3 SI-502A *Serial and Parallel timing for both A and C outputs*

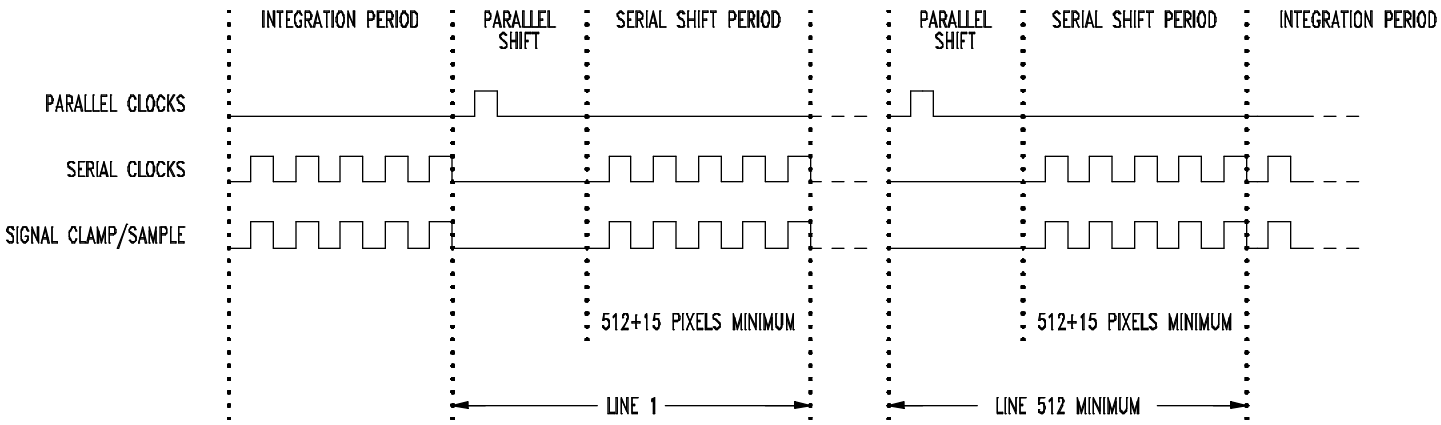

FIGURE 4 SI-502A *Typical full-frame readout*

SI-502A PIN DEFINITION

FRONT PIN #	BACK PIN #	FUNCTION	REGISTERS	SYMBOL
1	12	Substrate and Package Ground		SUB
2	11	Output transistor source, a output	a register	OUTa
3	10	Output Ground Reference	a register	GNDa
4	9	Transfer gate, upper serial register	a register	TGa
5	8	Parallel phase 3	image area	P3
6	7	Parallel phase 1	image area	P1
7	6	Parallel phase 2	image area	P2
8	5	Transfer gate, lower serial register	c register	TGc
9	4	Input diode	c register	IDc
10	3	input sample gate	c register	SGc
11	2	Serial phase 1, c register	c register	S1c
12	1	Substrate and Package Ground		SUB
13	44			N/C
14	43	Serial phase 2, c register	c register	S2c
15	42	*Temp. sense resistor		TR1
16	41	*Temp. sense resistor		TR2
17	40	Serial phase 3, c register	c register	S3c
18	39	Summing well, c output	c register	SWc
19	38	Last gate, c output	c register	LGc
20	37	Reset Gate, c output	c register	RGc
21	36	Reset Drain Supply, c output	c register	RDc
22	35			N/C
23	34			N/C
24	33	Output transistor drain, c output	c register	VDDc
25	32	Output transistor source, c output	c register	OUTc
26	31	Output Ground Reference	c register	GNDc
27	30	Transfer gate, lower serial register	c register	TGc
28	29	Parallel phase 3	image area	P3
29	28	Parallel phase 1	image area	P1
30	27	Parallel phase 2	image area	P2
31	26	Transfer gate, upper serial register	a register	TGa
32	25	Input diode	a register	IDa
33	24	input sample gate	a register	SGa
34	23			N/C
35	22			N/C
36	21	Serial phase 3, a register	a register	S3a
37	20	Serial phase 2, a register	a register	S2a
38	19	Serial phase 1, a register	a register	S1a
39	18	Summing well, a output	a register	SWa
40	17	Last gate, a output	a register	LGa
41	16	Reset transistor gate, a output	a register	RGa
42	15	Reset transistor drain, a output	a register	RDa
43	14	Output transistor drain, a output	a register	VDDa
44	13			N/C

TABLE 3 SI-502A *pin definitions*

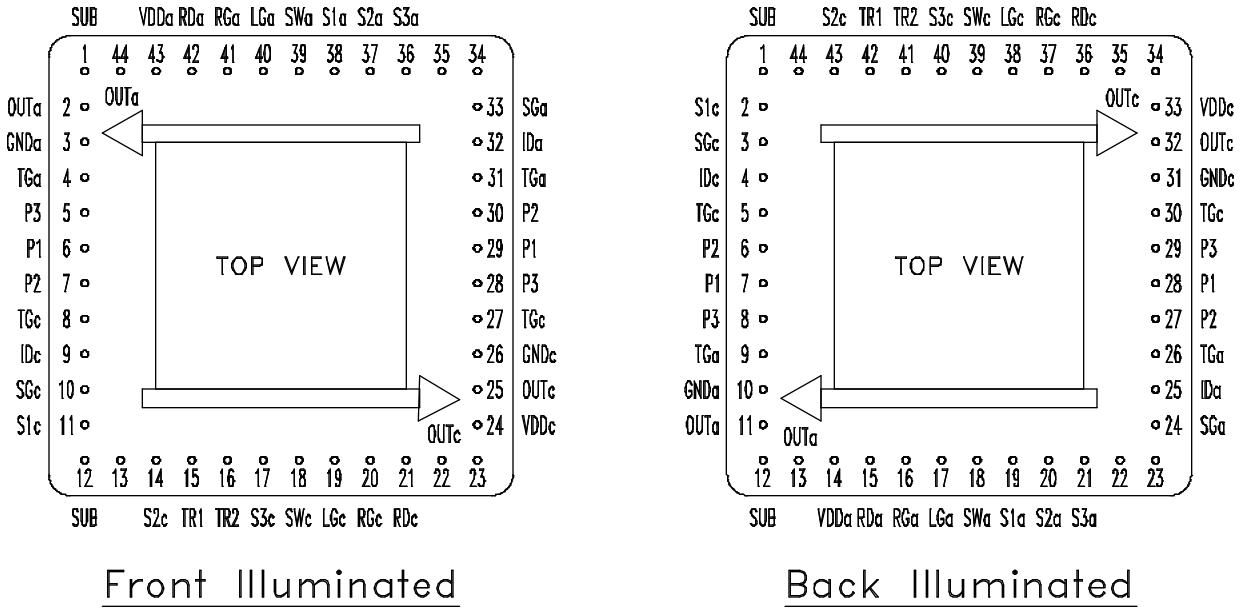

FIGURE 5 SI-502A *pin labels*

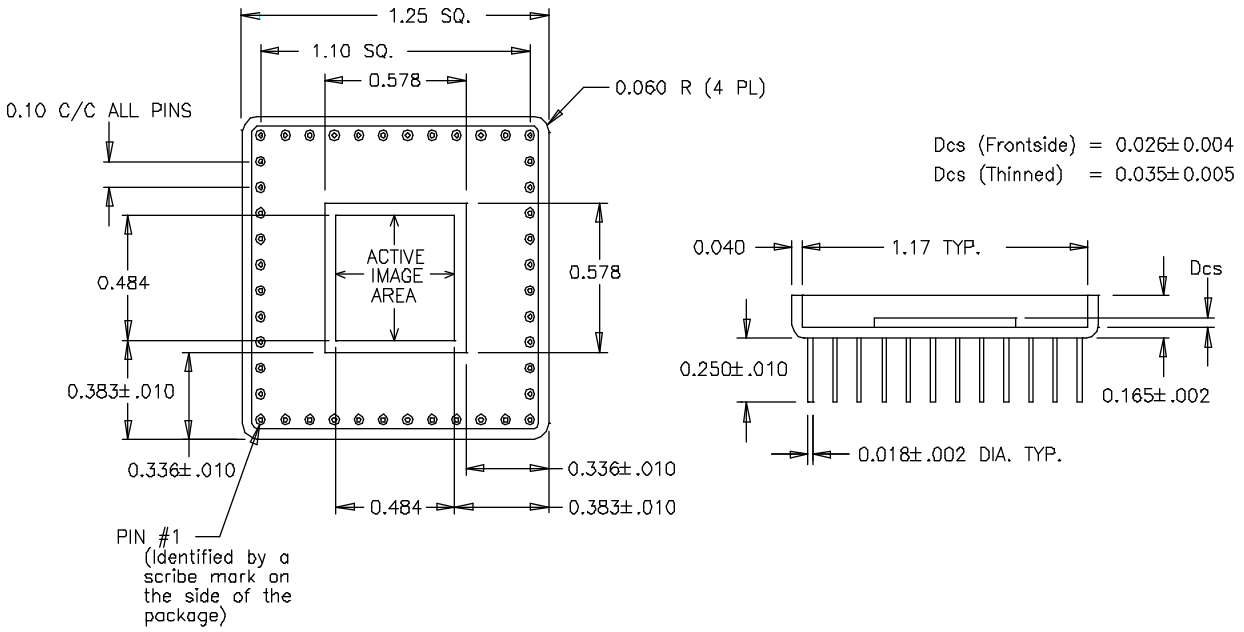

FIGURE 6 SI-502A *package configuration*

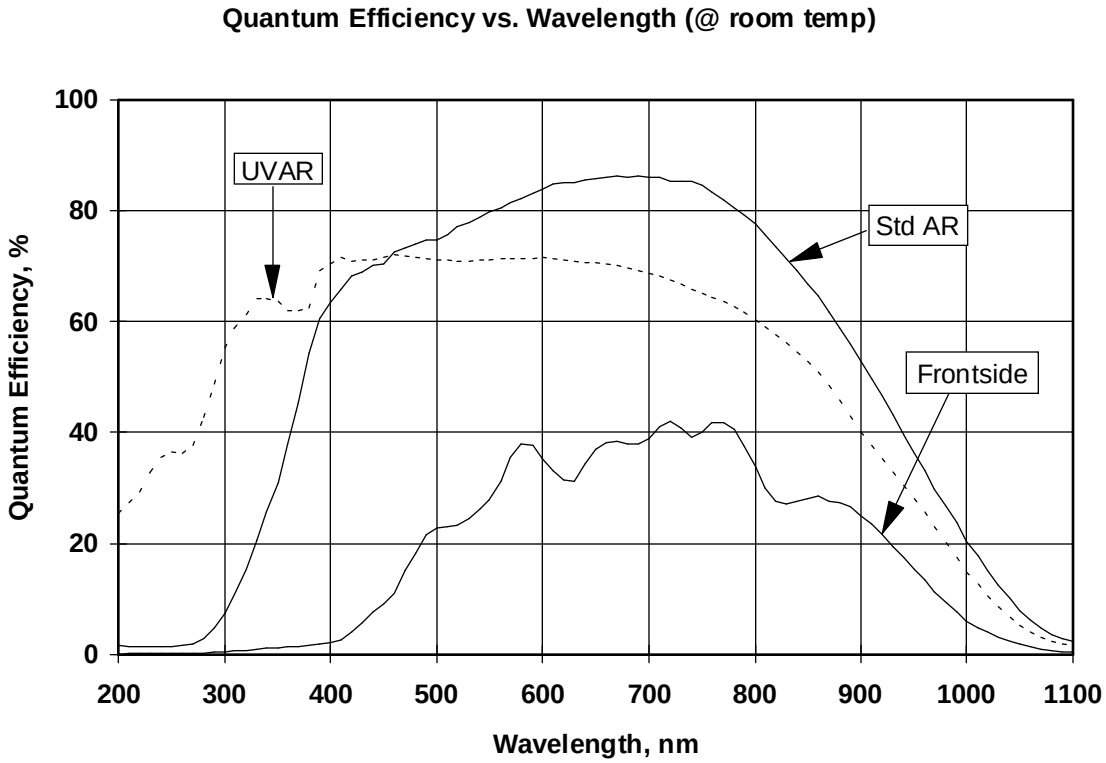

FIGURE 7 *Typical QE curves*

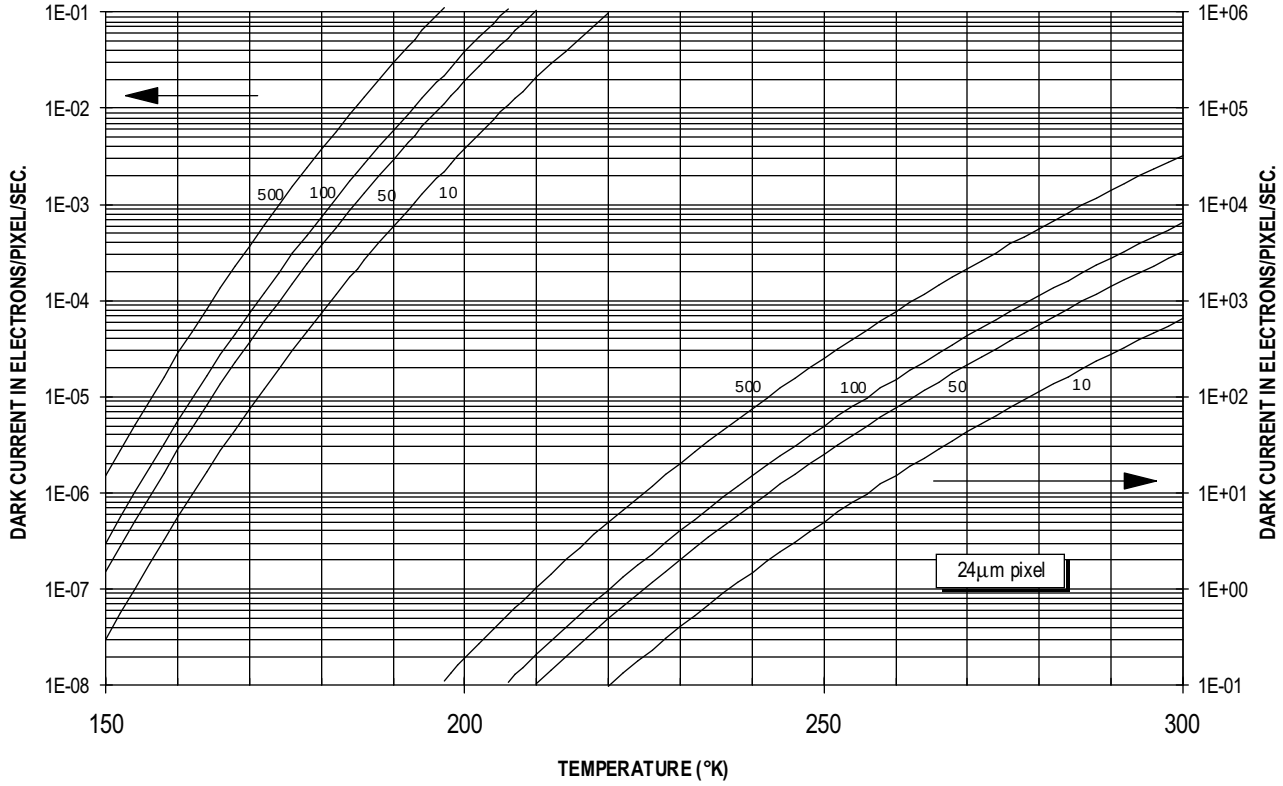

FIGURE 8 *Effect of temperature on dark current. Parameter is pAmp/cm^2 at 293K*

SCIENTIFIC IMAGING TECHNOLOGIES, INC.

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Scientific Imaging Technologies, Inc. (SITe) specializes in the research, design, and manufacture of charge-coupled devices (CCDs) and imaging subassemblies containing CCD components. SITe's scientific grade CCDs are used in applications for astronomy, aerospace, medical, military surveillance, spectroscopy, and other areas of imaging research. Commercial uses of SITe high performance CCDs include such areas as biomedical imaging, manufacturing quality control, environmental monitoring, and nondestructive testing.

With its focus on scientific-grade CCD imaging components and modules, SITe provides standard designs, user defined custom CCDs, and foundry services. SITe's engineering and manufacturing team builds custom CCD imagers for use in the most demanding applications including NASA programs, satellite platforms, and other research projects. Device formats are available as front illuminated or thinned, back illuminated CCDs.

Innovation, process development, and design experience date back to the founding of the group in 1974.

Product Precautions

Scientific Imaging Technologies, Inc. (SITe) realizes the use of charge-coupled devices (CCDs) for imaging is rapidly expanding into new applications. Awareness of the sensitivity of CCDs to electrostatic discharge (ESD) damage and the steps that can be implemented to prevent damage are very important to the end user.

With the exception of the back-illuminated SI424A, SITe imagers do not have built-in gate protection structures. Even with the protection structures, the imagers are very sensitive to ESD damage. It is imperative that proper precautions be taken whenever the imagers are handled.

The damage caused by ESD can be immediate and fatal (hard damage) resulting in a completely nonfunctional device. ESD damage can also be more subtle with no immediate device performance degradation. In this case, the result is a slow deterioration (soft damage) that may not be apparent until after extended operation.

There are three major areas where special procedures are required. We recommend that our customers use these procedures to minimize the risk of ESD damage.

1. Work areas specifically designed to minimize ESD.

2. Personnel requirements for ESD damage protection.

3. Use special ESD protected handling and shipping containers. SITe has developed a custom shipping container which grounds all the CCD pins together and allows clean and safe handling for incoming inspection and storage.

For more specific information on minimizing ESD damage, refer to SITe's technical briefing called "Recommended ESD Handling Procedures For CCD Imagers."

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