STANDARD
MICROSYSTEMS
CORPORATION

SLC88B17
ADVANCE INFORMATION

PCI-ISA Bridge Chip

FEATURES

- 5 Volt Operation
- PCI 2.1 Compliant
- Multifunction PCI to ISA bridge
  - Supports 33MHz PCI bus
  - Supports Full ISA at ¼ of PCI Frequency
  - Supports Full Subtractive Decode of PCI
  - Supports up to 5 ISA Slots
- Supports PC/PCI DMA Protocol
- Supports Serial Interrupts
- 160 Pin QFP Package

GENERAL DESCRIPTION

The SLC88B17 is a PCI device implementing a PCI-to-ISA bridge function. As a PCI-to-ISA bridge, the SLC88B17 supports full ISA protocols, including ISA master devices. It also supports PC/PCI DMA protocols for PCI based DMA applications. The interrupt logic supports serial interrupt protocol. The SLC88B17 normally is a subtractive decode bridge, it can be configured to positively decode a fixed memory range, from 0FFFF0000h to 0FFFFFFFFh.

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ARCHITECTURAL OVERVIEW

Figures 1 and 2 consist of a System Block Diagram of the SLC88B17 in desktop application and notebook application respectively.

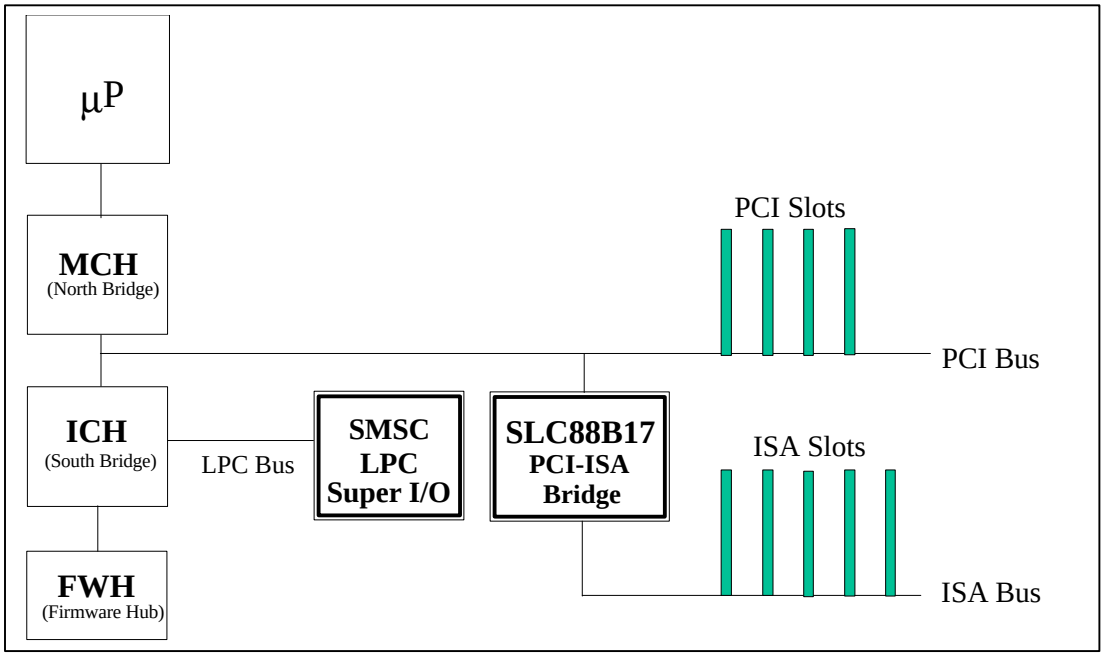


FIGURE 1 – DESKTOP APPLICATION

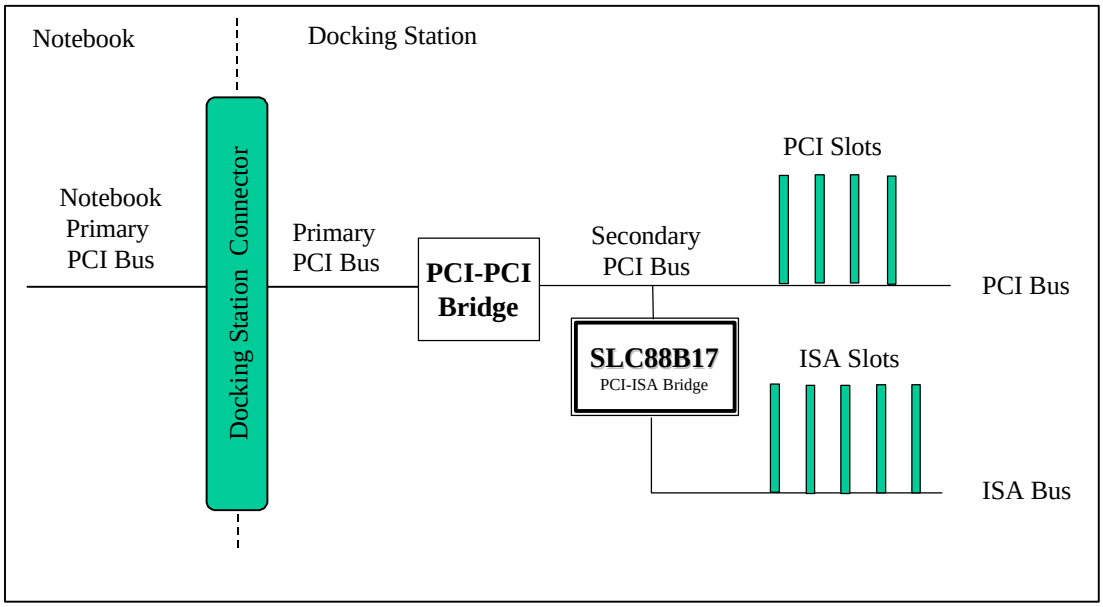


FIGURE 2 – NOTEBOOK DOCKING STATION APPLICATION

FUNCTIONAL BLOCK OVERVIEW

The SLC88B17 is a high integration chip. Below is a brief overview of the major functional blocks in the SLC88B17. Figure 3 shows the Block Diagram of the SLC88B17.

PCI-to-ISA Bridge

The SLC88B17 is compatible with the PCI 2.1 specification, as well as the ISA bus specification. The SLC88B17 operates as a PCI master for ISA masters. The SLC88B17 operates as a slave for its internal registers and for cycles that are passed to the ISA bus. The SLC88B17 positively decodes all internal registers.

The SLC88B17 can be configured for a full ISA bus. Like standard ISA Bridge chips, the SLC88B17 also provides byte-swap logic, I/O recovery support, wait-state generation, and SYSCLK generation. The SLC88B17 is designed to directly drive up to 5 ISA slots without external data or address buffering. The SLC88B17 is configured as a subtractive decode PCI to ISA Bridge but can also be configured to positively decode a fixed memory range, from 0FFFF0000h to 0FFFFFFFFh.

ISA DMA and Interrupt Logic

The DMA logic supports the PC/PCI protocol and allows PCI-based peripherals to initiate DMA cycle by encoding requests and grants through signals nISAREQ and nISAGNT.

The SLC88B17 interrupt logic transmits ISA interrupt requests through the SERIRQ signal line to the interrupt controllers for processing. The interrupt controllers normally reside on the south bridge chip.

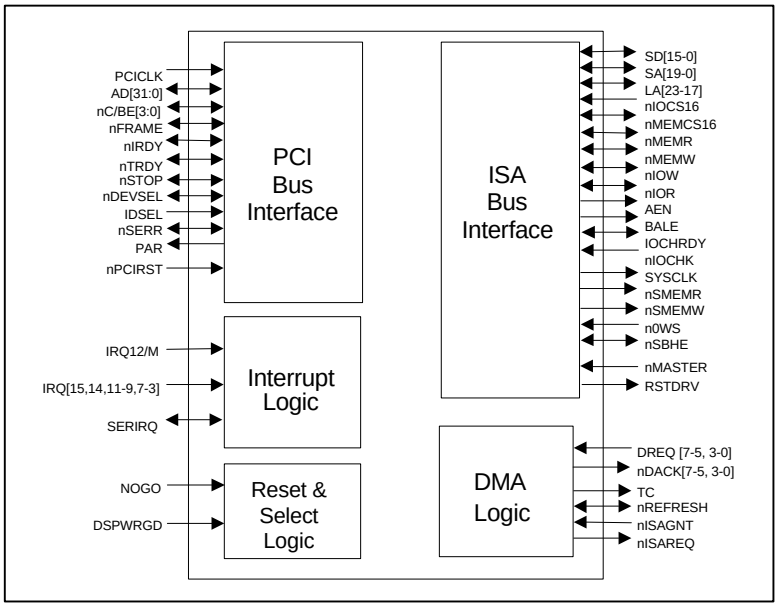
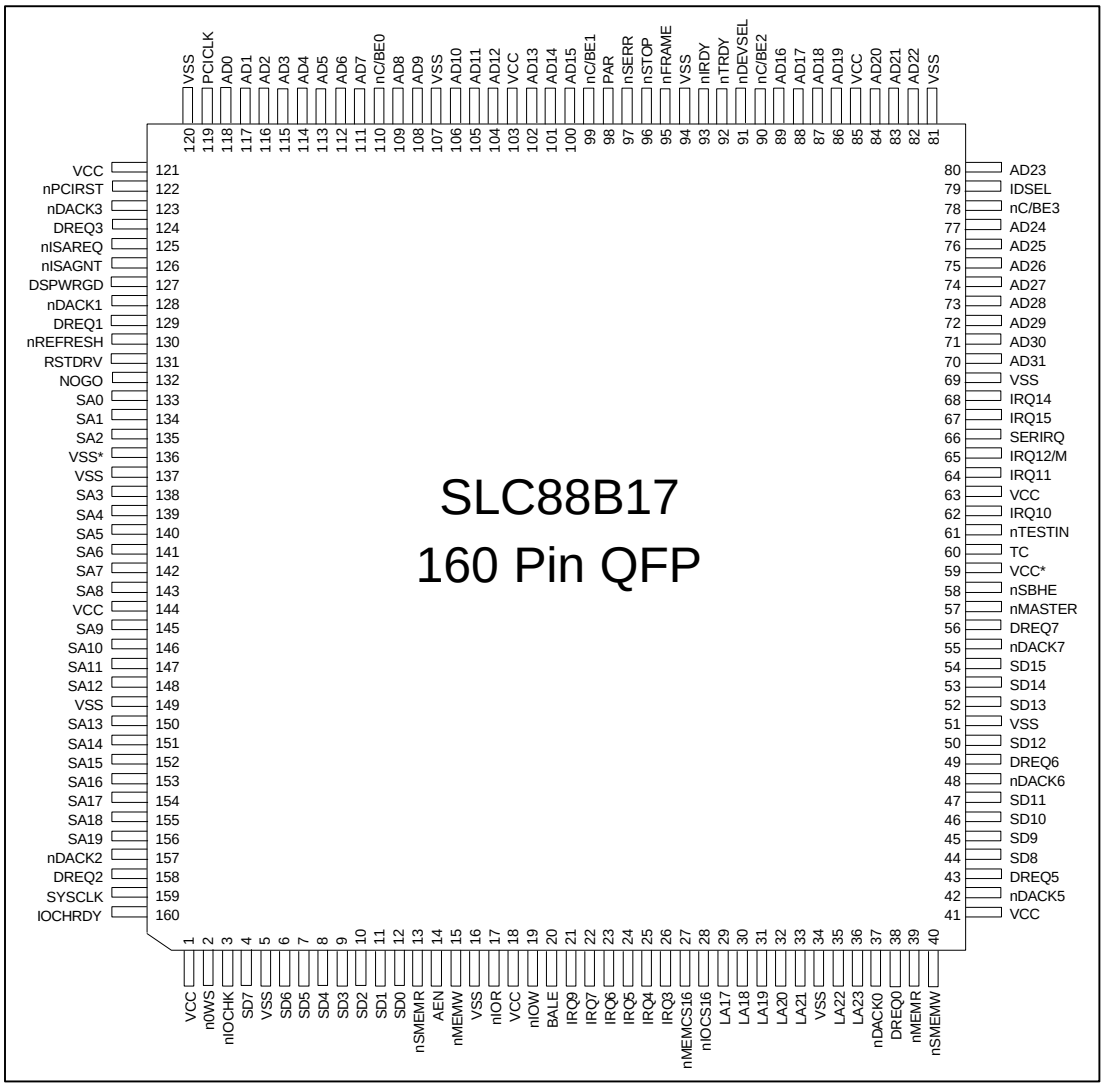


FIGURE 3 - CHIP BLOCK DIAGRAM

PIN CONFIGURATION



*=Core

SIGNAL DESCRIPTION

This section provides a detailed description of each SLC88B17 signal. The signals are arranged in functional groups according to their associated function.

The 'n' symbol at the beginning of a signal name indicates that it is an active low signal. When 'n' is not present before the signal name, it indicates an active high signal.

The terms assert or **assertion** indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The terms negate or **negation** indicates that a signal is inactive.

Certain signals have different functions, depending on the configuration programmed in the PCI configuration space. This signal whose function is being described is in bold font.

The term **High-Z** means tri-stated.
The term **Undefined** means the signal could be high, low, tri-stated, or in some in-between level.

The following notations are used to describe the signal type.

I	Input is an input-only signal.
O	Totem pole output is a standard active driver.
I/O	Input/Output is a bi-directional, tri-state input/output pin.
OD	Open drain.
I/OD	Input/Open Drain Output is a standard input buffer with an Open Drain Output.
s/t/s	Sustained tri-state is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives a s/t/s pin low must drive it high for at least one clock before letting it float. A new agent can not start driving a s/t/s signal any sooner than one clock after the previous owner tri-states it. An external pull-up resistor is required to sustain the inactive state until another agent drives it and must be provided by the central resource.
V	This is a power supply pin.

PCI Interface

NAME	TYPE	DESCRIPTION
AD[31-0]	I/O	**Address/Data.** PCI address and data lines. Address is driven with nFRAME asserted, data is driven or received in following clocks. During Reset: High-Z After Reset: High-Z
C/nBE[3-0]	I/O	**Command/Byte Enable.** The command is driven with nFRAME asserted, byte enables corresponding to supplied or requested data is driven in following clocks. C/nBE0 applies to byte 0, C/nBE1 applies to byte 1, etc. During Reset: High-Z After Reset: High-Z
nFRAME	I/O	**FRAME.** Its assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer will be followed. nFRAME remains tri-stated until driven by the SLC88B17 as an initiator. During Reset: High-Z After Reset: High-Z
nDEVSEL	I/O	**Device Select.** The SLC88B17 asserts nDEVSEL to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, the SLC88B17 asserts nDEVSEL when it samples IDSEL active in configuration cycles to SLC88B17 configuration registers. The SLC88B17 also asserts nDEVSEL when an internal SLC88B17 register is accessed or when the SLC88B17 subtractive or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, nDEVSEL indicates the response to a SLC88B17 initiated transaction and is also sampled when deciding whether to subtractive decode the cycle. nDEVSEL is asserted or sampled at medium decode time. It remains tri-stated until driven by the SLC88B17 as a target. During Reset: High-Z After Reset: High-Z
nIRDY	I/O	**Initiator Ready.** The signal is asserted when the SLC88B17 is ready for a data transfer. A data phase is completed on any clock both nIRDY and nTRDY are sampled asserted. nIRDY is an input to the SLC88B17 when the SLC88B17 is the target and an output when the SLC88B17 is an initiator. It remains tri-stated until driven by the SLC88B17 as a master. During Reset: High-Z After Reset: High-Z

NAME	TYPE	DESCRIPTION
nTRDY	I/O	**Target Ready.** The signal is asserted when the SLC88B17 is ready for a data transfer. A data phase is completed on any clock both nIRDY and nTRDY are sampled asserted. nTRDY is an input to the SLC88B17 when the SLC88B17 is the initiator and an output when the SLC88B17 is a target. It remains tri-stated until driven by the SLC88B17 as a target. During Reset: High-Z After Reset: High-Z
nSTOP	I/O	**Stop.** nSTOP indicates that the SLC88B17, as a Target, is requesting the initiator to stop the current transaction. As an initiator, nSTOP causes the SLC88B17 to stop the current transaction. nSTOP is an output when the SLC88B17 is a Target and an input when the SLC88B17 is an initiator. nSTOP is tri-stated from the leading edge of nPCIRST., and it remains tri-stated until driven by the SLC88B17 as a slave. During Reset: High-Z After Reset: High-Z
IDSEL	I	**Initialization Device Select.** IDSEL is used as a chip select during PCI configuration read and write cycles. The SLC88B17 samples IDSEL during the address phase of a transaction. The SLC88B17 responds by asserting nDEVSEL if IDSEL is sampled active during configuration cycle.
nSERR	I/O	**System Error.** nSERR can be driven active by any PCI device that detects a system error condition. Upon sampling nSERR active, the SLC88B17 can be programmed to generate a non-maskable interrupt (NMI) to the CPU. During Reset: High-Z After Reset: High-Z
PAR	O	**Parity.** PAR is “even” parity and is calculated on 36 bits (AD[31-0] and nC/BE[3-0]). PAR is calculated on 36 bits regardless of the valid byte enables. PAR is driven and tri-stated identically to the AD[31-0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase for all SLC88B17 initiated transactions. It is also an output during the data phase when the SLC88B17 is the initiator of a PCI write transaction, and when it is the target of a read transaction. During Reset: High-Z After Reset: High-Z
nPCIRST	I	**Reset.** This is a PCI reset input signal. In response to the assertion of nPCIRST, the SLC88B17 will assert ISA RSTDRV to reset ISA devices.

ISA Interface Signals

NAME	TYPE	DESCRIPTION
SA[19-0]	I/O	**System Address.** The address lines SA[19-17] that are coincident with LA[19-17] are defined to have the same values as LA[19-17] for all memory cycles. For I/O accesses, only SA[15-0] are used, and SA[19-16] are undefined. SA[19-0] are outputs when the SLC88B17 owns the ISA bus. They are inputs when an external ISA master owns the ISA bus. During Reset: High-Z After Reset: Undefined
LA[23-17]	I/O	**ISA LA[23-17].** LA[23-17] address lines allow accesses to physical memory on the ISA bus up to 16 Mbytes. They are outputs when the SLC88B17 owns the ISA bus. They become inputs whenever an ISA master owns the ISA bus. These signals are at an undefined state upon nPCIRST. During Reset: High-Z After Reset: Undefined.
SD[15-0]	I/O	**System Data.** 16-bit data path for devices residing on the ISA bus. They are undefined during refresh. During Reset: High-Z After Reset: Undefined.
nSMEMR	O	**Standard Memory Read.** The SLC88B17 asserts nSMEMR to request an ISA memory slave to drive data onto the data lines. If the memory access is below the 1Mbyte range during DMA, SLC88B17 master, or ISA master cycles, the SLC88B17 asserts nSMEMR. nSMEMR is a delayed version of nMEMR. During Reset: High-Z After Reset: High
nSMEMW	O	**Standard Memory Write.** The SLC88B17 asserts nSMEMR to request an ISA memory slave to receive data from the data lines. If the memory access is below the 1Mbyte range during DMA, SLC88B17 master, or ISA master cycles, the SLC88B17 asserts nSMEMW. nSMEMW is a delayed version of nMEMW. During Reset: High-Z After Reset: High
nMEMR	I/O	**Memory Read.** nMEMR is the command to a memory slave that it may drive data onto the ISA data bus. nMEMR is an output when the SLC88B17 owns the ISA bus or during refresh cycles. nMEMR is an input when an ISA master owns the ISA bus. For DMA cycles, the SLC88B17, as a master, asserts nMEMR. During Reset: High-Z After Reset: High.

NAME	TYPE	DESCRIPTION
nMEMW	I/O	**Memory Write.** nMEMW is the command to a memory slave that it may latch data from the ISA data bus. nMEMW is an output when the SLC88B17 owns the ISA bus. nMEMW is an input when an ISA master owns the ISA bus. For DMA cycles, the SLC88B17, as a master, asserts nMEMW. During Reset: High-Z After Reset: High
AEN	O	**Address Enable.** AEN is asserted during DMA cycles to prevent I/O slaves from claiming DMA cycles as valid I/O cycles. When de-asserted, it indicates that an I/O slave may respond to the bus command. When asserted, it informs I/O slave that a DMA transfer is occurring on the ISA bus. The signal is driven high during SLC88B17 initiated refresh cycles, it is driven low upon nPCIRST. During Reset: High-Z After Reset: Low
BALE	O	**Address Latch Enable.** BALE is asserted by the SLC88B17 to indicate that the address and nSBHE signal lines are valid. The LA[23-17] are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. During Reset: High-Z After Reset: Low
nSBHE	I/O	**System Byte High Enable.** When asserted indicates that a byte is being transferred on the SD[15-8] of the data bus. It is negated during refresh cycle. nSBHE is an output when the SLC88B17 owns the ISA bus. It becomes an input when an external ISA master owns the ISA bus. During Reset: High-Z After Rest: Undefined
nIOCHK	I	**IO Channel Check.** When asserted, the signal indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus.

NAME	TYPE	DESCRIPTION
IOCHRDY	I/O	**IO Channel Ready.** When asserted, the signal indicates that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when the SLC88B17 owns the ISA bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. It becomes an output when an external ISA master owns the ISA bus and is accessing DRAM or a SLC88B17 register. As an output, the signal is driven low from the falling edge of the ISA commands by the SLC88B17. After data is available for the ISA master to read or the SLC88B17 latches the data for a write cycle, IOCHRDY is asserted for 70ns. After that, the IOCHRDY is floated. The SLC88B17 does not drive the signal when it is not the target of a bus master cycle. During Reset: High-Z After Reset: High-Z
nIOCS16	I	**16-Bit IO Chip Select.** When asserted, it indicates that the ISA IO device supports 16-bit I/O bus cycles.
nIOR	I/O	**IO Read.** ISA I/O Read command to an ISA I/O device. The I/O device must hold the data valid until after nIOR is negated. nIOR is an input when an external ISA master owns the ISA bus. During Reset: High-Z After Reset: High
nIOW	I/O	**IO Write.** ISA I/O Write command to an ISA I/O device. The I/O device may latch data from the ISA data bus. nIOW is an input when an external ISA master owns the ISA bus. During Reset: High-Z After Reset: High
nMEMCS16	I/O	**Memory Chip Select 16.** nMEMCS16 is a decode of LA[23-17] without any qualification of the command signals. ISA devices that are 16-bit memory devices drive this signal low. The SLC88B17 ignores nMEMCS16 during I/O and refresh cycles. It is used by byte-swap logic during DMA cycles. This signal is an output when an ISA master owns the ISA bus. The SLC88B17 drives this signal low during ISA master to DRAM cycles. During Reset: High-Z After Reset: High-Z
n0WS	I	**Zero Wait States.** The signal is asserted by an ISA slave to indicate that the current cycle can be shortened after the address and command signals are decoded. 16-Bit ISA memory cycle can be reduced to 2 SYSCLKs. 8-Bit memory or I/O cycle can be reduced to 3 SYSCLKs. 16-Bit IO cycle is not affected. If IOCHRDY is de-asserted and n0WS is asserted during the same clock, then n0WS is ignored and wait states are added while IOCHRDY is de-asserted.

NAME	TYPE	DESCRIPTION
RSTDRV	O	**Reset Drive.** The SLC88B17 asserts RSTDRV to reset devices that reside on the ISA bus. The SLC88B17 asserts the signal during hard reset and power-up. During Reset: High After Reset: Low
nMASTER	I	**Master.** The signal is used with a DREQ line by an ISA master to gain control of the ISA Bus.
DSPWRGD	I	**Docking Station Power Good. The signal should be asserted active when the SLC88B17 power source is stable.**

DMA Signals

NAME	TYPE	DESCRIPTION
DREQ[0-3] DREQ[5-7]	I	**DMA Request.** These DREQ lines are used to request DMA services from the DMA controller or for a 16-bit ISA master to gain control of the ISA bus. The active level (high or low) can be programmed via the DMA command register. The request must remain active until the corresponding nDACK is asserted.
nDACK[0]	I/O	**DMA Acknowledge.** This pin is normally used to return DMA acknowledge signal for DMA channel 0 in response to its data transfer request. During reset, the SLC88B17 also senses the voltage level of the nDACK0 pin. If it is pulled down to VSS externally, the SLC88B17 will claim (i.e. positively decode) all PCI memory cycles whose address falls in the range of FFF00000h to FFFFFFFFh, and forward them to the ISA bus.
nDACK[1-3] nDACK[5-7]	O	**DMA Acknowledge.** DMA acknowledge signals for the corresponding requests. If the DREQ goes inactive before nDACK being asserted, the nDACK signal will not be asserted. During Reset: High After Reset: High
nISAREQ	O	**ISA DMA Request.** This is DMA requests for PC/PCI protocol.
nISAGNT	I	**ISA DMA Grant.** This is DMA grant for PC/PCI protocol. During Reset: High After Reset: High
TC	O	**Terminal Count.** Terminal count indicator. The SLC88B17 asserts TC after a new address has been output and the byte count expires with that transfer. TC remains asserted until AEN is negated, unless AEN is negated during an auto initialization. TC is negated before AEN is negated during an auto initialization.
nREFRESH	I/O	**Refresh Request.** As an output, nREFRESH is used to indicate when a refresh is in progress. The SA[7-0] should be applied to all banks of DRAM on the ISA bus so that when nMEMR is asserted, the entire expansion bus DRAM is refreshed. This signal is an output only when the SLC88B17 DMA controller is a master on the bus responding to the internally generated request for refresh. It is an input signal during ISA master cycles. During Reset: High-Z After Reset: High

Interrupt Signals

NAME	TYPE	DESCRIPTION
IRQ[3-7, 9-11, 14-15]	I	**Interrupt Requests.** These interrupts may be programmed for either an edge sensitive or a high level sensitive mode. Default is edge sensitive mode. If the request goes inactive before it is acknowledged, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ12/M	I	**Interrupt Request 12.** This is an interrupt request channel 12. In addition, this pin can also be programmed to provide the mouse interrupt function. When the mouse interrupt is selected, the SLC88B17 latches a low to high transition on this signal and generates an INTR to the CPU as IRQ12. An internal IRQ12 interrupt will continue to be generated until a Reset or an I/O read access to address 60h is detected.
SERIRQ	I/O	**Serial Interrupt Request.** Serial interrupt input decoder, typically used with the Distributed DMA protocol.

Clocks

NAME	TYPE	DESCRIPTION
PCICLK	I	**PCI Clock.** This is a clock signal provides timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to the edge.
SYSCLK	O	**ISA System Clock.** SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is derived by dividing PCICLK by 4. During Reset: Running After Reset: Running

Mobile PCI-PCI

NAME	TYPE	DESCRIPTION
NOGO	I	**NO GO.** This signal indicates which master initiated the current transaction and also indicates whether or not the current bus cycle is targeted for the ISA bus. This signal is point–to-point connection between the South Bridge and SLC88B17.

Power and Ground Signals

NAME	TYPE	DESCRIPTION
VCC	V	**Main Voltage Supply.** These pins are the primary voltage supply for the SLC88B17 and must be tied to 5V.
VSS	V	**Main Ground.** These pins are the primary ground for the SLC88B17.
nTESTIN	I	**Test Input. This signal should always be high.**

PCI/ISA BRIDGE REGISTER DESCRIPTION

The SLC88B17 internal registers are organized to function as an ISA Bridge with other AT compatibility logic. It has its registers divided into a set of PCI configuration registers and one or more register sets located in the system I/O space.

Some of the SLC88B17 registers contain reserved bits. Software must ensure that the value of reserved bit positions are preserved. That is, Software must first read the value of the reserved bits, merged the value with the new values for the other bits and then write back to the register.

Upon reset, the SLC88B17 sets its internal registers to predetermined default states, which represents the minimum functionality feature set required for the BIOS to bring up the system. It is the responsibility of the BIOS to properly program the configuration registers to achieve optimal system performance.

The following notation is used to describe register access attributes:

RO Read Only. Writes have no effect.
WO Write Only. Reads have no effect.
R/W Read/Write. The register can be read or written.
R/WC Read/Write Clear. A register bit with this attribute can be read and written. However, a write of a 1 clears the corresponding bit (sets to 0) and a write of a 0 has no effect.

PCI/ISA Bridge Register Mapping

PCI Configuration Register Mapping Table

PCI OFFSET ADDRESS	MNEMONIC	REGISTER NAME	ACCESS RIGHT
00-01h	VID	Vendor Identification	RO
02-03	DID	Device Identification	RO
04-05	PCICMD	PCI Command Register	R/W
06-07	PCISTS	PCI Status Register	R/W/C
08	RID	Revision ID	RO
09-0B	CLASSCODE	Class Code	RO
0C-0D		Reserved	
0E	HEDT	Header Type	RO
0F-3F		Reserved	
40	IORT	ISA I/O Recovery Timer	R/W
41		Reserved	

MISA Specific Register Mapping Table

OFFSET ADDRESS	MNEMONIC	REGISTER NAME	ACCESS RIGHT
42	MISA_STS	MISA Error Status Register	RO
43-FFh		Reserved	

PCI/ISA Bridge PCI Register Description (Function 0)

This section describes in detail the registers associated with the SLC88B17 PCI-to-ISA bridge function.

VID **Vendor Identification Register**
Offset Address: 00 - 01h
Default Value: 1055h
Access: Read Only

This is a 16 bit PCI Vendor ID assigned to SMSC.

DID **Device Identification Register**
Offset Address: 02 - 03h
Default Value: 8170h
Access: Read Only

This is the PCI device ID of the SLC88B17.

PCICMD **PCI Command Register**
Offset Address: 04 - 05h
Default Value: 0007h
Access: Read/Write

This register provides basic control over the SLC88B17's ability to respond to PCI cycles. When a 0 is written to this register, SLC88B17 is logically disconnected from the PCI bus for all accesses except configuration accesses.

BIT	FUNCTION
15-10	Reserved.
9	Fast Back-to-Back: not implemented, hardwired to 0..
8	**nSERR Enable**: 1=Enable, 0=Disable. Controls the enable for the nSERR driver on the PCI interface.
7-5	Reserved. Read as 0
4	Postable Memory Write Enable. This bit is hardwired to 0.
3	**Special Cycle Enable**: Not implemented, hardwired to 0.
2	Bus Master Enable: This bit is hardwired to a 1 (always enabled).
1	Memory Access Enable: The SLC88B17 memory Space is always enabled.. This bit is hardwired to a 1.
0	IO Access Enable: The SLC88B17 I/O space is always enabled.. This bit is hardwired to a 1.

PCISTS **PCI Status Register**
Offset Address: 06 - 07h
Default Value: 0200h
Access: Read/Write

This register status information for PCI bus related events. Reads to this register behave normally. Bits in this register can only be set by SLC88B17 events (through hardware)

BIT	FUNCTION
15	Detected Parity Error. Not implemented, hardwired to a 0.
14	**Signaled nSERR Status: When the SLC88B17 asserts** the nSERR signal (delay transaction time out), this bit is set to 1. Software can set this bit to a 0 by writing a 1 to it.
13	**Master Abort Status:** When the SLC88B17, as a master on the PCI bus, generates a master abort, this bit is set to 1. Software can set this bit 0 by writing a 1 to it.
12	**Received Target Abort Status**: This bit is set when the SLC88B17 target aborts a PCI transaction as a target. Software can set this bit 0 by writing a 1 to it.
11	**Signaled Target Abort:** This bit is set when the SLC88B17 signals a target abort for a PCI transaction. Software can set this bit 0 by writing a 1 to it.
10-9	nDEVSEL timing: Always 01 to select “medium” timing, which is two PCI clocks after the assertion of nFRAME, when the SLC88B17 asserts nDEVSEL as a PCI target. The SLC88B17 always does a medium decode for PCI configuration accesses (the only type of access that it does a positive decode for). SLC88B17 responds to all other types of accesses through subtractive decoding and the NOGO signal
8	**Parity Detected**: Always 0, does not check parity.
7	**Fast Back-to-Back**: Always 0, does not support fast back-to-back transaction.
6	**66 MHz/33MHz**: Hardwired to 0. Maximum PCI bus frequency is 33MHz.
5	**User Definable Features (UDF):** Hardwired to 0. SLC88B17 does not support any UDFs.
4-0	Reserved.

RID **Revision Identification Register**
Offset Address: 08h
Default Value: 00h
Access: Read Only

BIT	FUNCTION
7-0	Hardwired to the revision number, which is set to 00 as the initial number.

CLASSC **Class Code Register**
Offset Address: 09 - 0Bh
Default Value: 060100h
Access: Read Only

This class code register is a read-only register used to identify SLC88B17. Writes to this register have no effect.

BIT	FUNCTION
23-16	**Base Class Code**: always 06 indicating that the SLC88B17 is a bridge device.
15-8	**Sub-Class Code**: PCI-to-ISA subtractive decode bridge = 01h
7-0	**Programming Interface**: 00, no interface is defined.

HEDT **Header Type Register**
Offset Address: 0Eh
Default Value: 00h
Access: Read Only

This register is used to indicate that SLC88B17 configuration space adheres to PCI local bus specification. It also indicates that SLC88B17 is not a multifunction device.

BIT	FUNCTION
7	**Multifunction Indicator**. 00h= not a multi-function device.
6-0	**Layout Code**. Value=0 (PCI layout type 00)

IORT **ISA I/O Recovery Timer Register**
Offset Address: 40h
Default Value: 4Dh
Access: Read/Write

This register is used to add additional recovery delay between PCI initiated 16bit and 8bit I/O cycles to the ISA Bus. SLC88B17 automatically forces a minimum delay of 3.5SYSCLKs between back to back 16bit and 8bit I/O cycles to the ISA Bus. The delay is measured from the rising edge of the IO command to the falling edge to the next IO command. No additional delay is inserted for back to back I/O "sub cycles" generated as a result of byte assembly or disassembly.

BIT	FUNCTION
7	**SYSCLK Divider Select.** 1= Divide PCI clock by 3. 0 = Divide PCI clock by 4. Sets how the SYSCLK is generated form the PCI clock.
6	**8 bit IO recovery enable.** When set to a 1, enables the recovery time programmed in bits[5-3]. When set to a 0, disables programmed recovery times and uses the default timing of 3.5 SYSCLKs for 8-bit I/O recovery times.
5-3	**8 bit IO recovery times.** When bit 6 is set to 1. Programmable delays between back to back 8 bit PCI cycles to an ISA I/O slave is shown in terms of additional ISA clock recovery cycles (SYSCLK). 001: 1 010: 2 011: 3 100: 4 101: 5 110: 6 111: 7

BIT	FUNCTION
2	**16 bit IO recovery enable.** When set to a 1, enables the recovery time programmed in bits[1-0]. When set to a 0, disables programmed recovery times and uses the default timing of 3.5 SYSCLKs.
1-0	**16 bit IO recovery times (actual recovery clock counts) when bit 2 is set to 1.** 01: 1 102 11: 3 00: 4

MISCON Miscellaneous Control Register
Offset Address: 041h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7	Passive Release Enable. 0: Disable Passive Release. 1: Enable.
6	Delay Transfer Enable. 0: Disable. 1: Enable.
5-3	Reserved
2	nPERR Enable. 0: Disable. 1: Enable.
1	AT DRAM slow refresh. 0: Disable. 1: Enable. Refresh interval is extended to 60 us.
0	AT refresh option. 0: Disable 1: Enable.

MISA_STS MISA Error Status Register
Offset Address: 42h
Default Value: 00h
Access: Read Only

This register reflects the error status of the ISA interface.

BIT	FUNCTION
7-3	**Reserved.**
2	**nIOCHK Pin State.** This bit reflects the inverse state of nIOCHK pin on the ISA Bus. When this bit is set, SLC88B17 pulses nSERR (if enabled via the PCICMD register).
1	**Reserved.**
0	**Byte Lane Error (BYTERR).** This bit is set if SLC88B17 detects an illegal byte lane combination for a PCI I/O cycles. When this condition is detected, SLC88B17 signals a target abort and pulses the nSERR signal (if enabled via the PCICMD register).

TOM **Top of Memory Register**
Offset Address: 43h
Default Value: 0Eh
Access: Read/Write

This register controls the forwarding of DMA or ISA master memory cycles to the PCI bus and sets the top of main memory accessible by ISA or DMA devices. In addition, this register controls the forwarding of ISA or DMA accesses to the lower BIOS range (E0000h-EFFFFh) and the 512-640Kbyte main memory region.

BIT	FUNCTION
7-4	**Top of Memory Accessible by the ISA Master/DMA devices.** The top of memory can be assigned in 1Mbyte increments from 1-16 Mbytes. ISA or DMA accesses within this range, and not in the memory hole region, are forwarded to PCI. 0000: 1 Mbytes 0001: 2 Mbytes 0010: 3 Mbytes 0011: 4 Mbytes 0100: 5 Mbytes 0101: 6 Mbytes 0110: 7 Mbytes 0111: 8 Mbytes 1000: 9 Mbytes 1001: 10 Mbytes 1010: 11 Mbytes 1011: 12 Mbytes 1100: 13 Mbytes 1101: 14 Mbytes 1110: 15 Mbytes 1111: 16 Mbytes Note: If a 1Mbyte memory hole is created for the Host-to-PCI bridge chip between 15 and 16 Mbytes, this register should be set to 15 Mbytes.
3	**ISA/DMA E0000-EFFFFh Memory Region Forwarding (to PCI) Enable.** If this bit is a 1, ISA/DMA cycles which access lower BIOS region are forwarded to PCI. If this bit is a 0, no forwarded (always contained to ISA).
2	**ISA/DMA 640-768K, A0000-BFFFFh, Memory Region Forwarding Enable.** 1: Enable, ISA/DMA cycles which access 640-768K memory region are forwarded to PCI. 0: Disable (contained to ISA).
1	**ISA/DMA 512K-640K Memory Region Forwarding Enable.** 1: Enable, ISA/DMA cycles which access 512-640K memory region are forwarded to PCI. 0: Disable (contained to ISA).
0	**Reserved**

PCI/ISA BRIDGE FUNCTIONAL DESCRIPTION

This section describes the major functions of the SLC88B17 PCI-to-ISA bridge.

Memory Map

The SLC88B17 interfaces to two system buses: PCI and ISA buses. The SLC88B17 normally acts as a subtractive decoding agent, it also provides positive decode for certain memory space accesses on the PCI bus. ISA masters and DMA devices can access PCI memory. ISA masters and DMA devices do not have accesses to host or PCI I/O space.

ISA/DMA Memory Access

The following table shows the SLC88B17's action when ISA Master or DMA accesses to the memory space.

MEMORY ADDRESS RANGE OF A DMA/ISA MASTER CYCLE	ACTION
(Top of Memory) to 128 Mbyte	Confine to ISA
1Mbyte to (Top of Memory)	Forward to PCI. Top of Memory is declared via bits 7-4 of TOM.
(1Mbyte – 64Kbyte) to 1Mbyte	Forward to PCI
(1Mbyte - 128Kbyte) to (1Mbyte -64Kbyte)	Forward to PCI if bit3/TOM=1.
768Kbyte to (1Mbyte - 128Kbyte)	Forward to PCI
640Kbyte to 768Kbyte	Forward to PCI if bit2/TOM =1.
512Kbyte to 640Kbyte	Forward to PCI if bit1/TOM=1
0-512Kbyte	Forward to PCI

PC/PCI DMA Logic

PC/PCI DMA uses dedicated nISAREQ and nISAGNT signals to permit PCI devices to request transfers associated with specific DMA channels. Upon receiving a request and getting control of the PCI bus, the south bridge asserts the nISAGNT signal and performs a two-cycle transfer. For example, if data is to be moved from the peripheral to main memory, the south bridge will first read data from the peripheral and then write it to main memory. The read-from-peripheral cycle will then pass to ISA bus through the SLC88B17. The location in main memory is the Current Address Registers in the DMA controller.

The SLC88B17 provides support for DMA across PCI using the PC/PCI DMA Protocol through the nISAREQ and nISAGNT signal pair. The nISAREQ/nISAGNT pair follows the PC/PCI serial protocol described below.

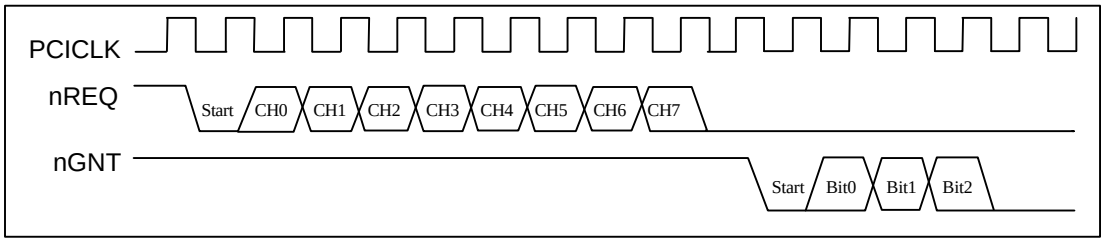


FIGURE 4 - DMA SERIAL CHANNEL PASSING

The SLC88B17 encodes the channel request information as shown above, where CH0-CH7 are one clock active high states representing DMA channel requests 0-7.

The south bridge encodes the granted channel on the nISAGNT line as shown above, where the bits have the same meaning as shown in the figure. For example, the sequence [start, bit 0, bit 1, bit 2]=[0,1,0,0] grants DMA channel 1 to the SLC88B17, and the sequence [start, bit 0, bit 1, bit 2]=[0,0,1,1,] grants DMA channel 6 to the SLC88B17.

The SLC88B17 uses the channel passing protocol described above. It works as follows:

1. If the SLC88B17 has more than one request active, it will resend the request serial protocol after one of the requests has been granted the bus and it has completed its transfer. The SLC88B17 will drive its nISAREQ inactive for two clocks and then transmit the serial channel passing protocol again, even if there are no new requests from the PCI expansion agent to the south bridge. For example: If the SLC88B17 had active requests for DMA channel 1 and Channel 5, it would pass this information to the south bridge through the expansion channel passing protocol. If after receiving nISAGNT (assume for CH5) and having the device finish its transfer (device stops driving request to the SLC88B17) it would then re-transmit the expansion channel passing protocol to inform the south bridge that DMA channel 1 was still requesting the bus, even if that was the only request the SLC88B17 had pending.
2. If the SLC88B17 has a request go inactive before the south bridge asserts nISAGNT, it will resend the expansion channel passing protocol to update the south bridge with this new request information. For example: if the SLC88B17 has DMA channel 1 and 2 requests pending it will send them serially to the south bridge using the expansion channel passing protocol. If, however, DMA channel 1 goes inactive into the SLC88B17 before the SLC88B17 receives a nISAGNT from the south bridge, the SLC88B17 will pull its nISAREQ line high for one clock and

resend the expansion channel passing information with only DMA channel 2 active. Note that the south bridge does not do anything special to catch this case because a DREQ going inactive before a nDACK is received is not allowed in the ISA DMA protocol and, therefore, does not need to work properly in this protocol either. This requirement is needed to be able to support Plug-n-Play devices that toggle nDREQ lines to determine if those lines are free in the system.

3. If the SLC88B17 has sent its serial request information and receives a new DMA request before receiving nISAGNT the SLC88B17 will resend the serial request with the new request active. For example: if the SLC88B17 has already passed requests for DMA channel 1 and 2 and sees DREQ 3 active before a nISAGNT is received, it will pull its nREQ line high for one clock and resend the expansion channel passing information with all three channels active.

The three cases above show the following functionality in the SLC88B17:

1. Drive nISAREQ inactive for one clock to signal new request information.
2. Drive nISAREQ inactive for two clocks to signal that a request that had been granted the bus has gone inactive.
3. The nISAREQ and nISAGNT state machines run independently and concurrently (i.e., a nISAGNT could be received while in the middle of sending a serial nISAREQ or nISAGNT could be active while nISAREQ is inactive).

PCI DMA Expansion Cycles

In the PC/PCI DMA mode, the DMA controller does a two-cycle transfer (a load followed by a store) as opposed to the ISA “fly-by” cycle for the SLC88B17. The memory portion of the cycle generates a PCI memory read or memory write bus cycle, its address representing the selected memory.

The I/O portion of the DMA cycle generates a PCI I/O cycle to one of the four I/O addresses (Table 1). Note that these cycles must be qualified by an active nISAGNT signal to the SLC88B17.

Table 1 - DMA Cycle vs. I/O Address

DMA Cycle Type	DMA I/O Address	TC (A2)	PCI Cycle Type
Normal	00h	0	I/O Read/Write
Normal TC	04h	1	I/O Read/Write
Verify	0C0h	0	I/O Read
Verify TC	0C4h	1	I/O Read

For PCI DMA cycles, the I/O address indicates the type of DMA cycle taking place (whether it's a normal or a verify cycle, and if this is the last transfer of the buffer). Note that the A2 address line is encoded as the terminal count signal for PCI cycles; A2 asserted during a PCI I/O cycle indicates the last transfer in the current DMA buffer. To ensure that non Mobile PC/PCI compliant PCI I/O devices do not confuse Mobile PC/PCI DMA cycles for normal I/O cycles, the addresses used by PCI DMA cycles correspond to the slave addresses of the Mobile PC/PCI DMA controller.

All PCI DMA I/O ports are DWord aligned and can be either byte or word in size. This means that any PCI DMA I/O port are always connected to the lower data lines of the PCI data bus (Table 2). The byte enables also reflect this during the I/O portion of a PCI DMA cycle. Table 3 illustrates the byte enable for any given PCI DMA cycle.

Table 2 - PCI Data Bus vs DMA I/O Port Size

PCI DMA I/O Port Size	PCI Data Bus Connection
Byte	AD[7:0]
Word	AD[15:0]

Table 3 - DMA I/O Cycle Width vs nBE[3:0]

nBE[3:0]	Description
1110b	8-bit DMA I/O Cycle
1100b	16-bit DMA I/O Cycle

Note: For verify cycles the value of the byte enables (Bes) is a "don't care"

The SLC88B17 recognizes a valid signal on its nISAGNT combined with the DMA I/O address as its command authorization to initiate a DMA access cycle. The south bridge is required to assert the DMA I/O device's nISAGNT signal until the data phase of the I/O portion of the DMA transfer.

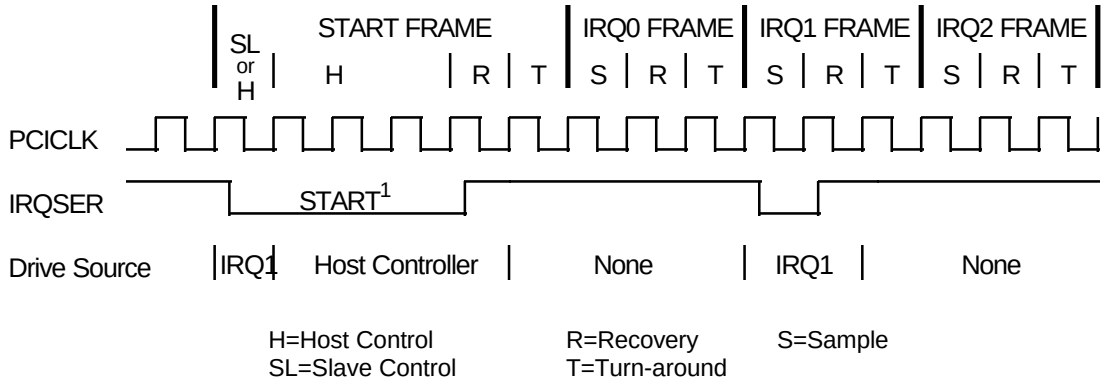
SERIAL INTERRUPTS

The SLC88B17 supports the serial interrupt to transmit interrupt requests to the host system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems, Version 6.0.

Timing Diagrams For IRQSER Cycle

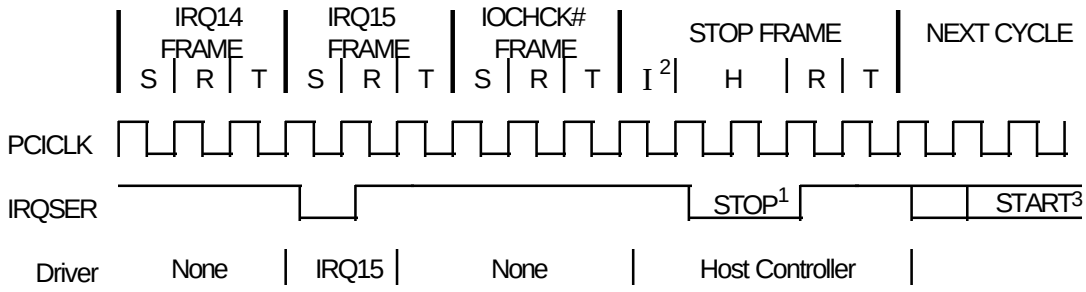
PCICLK = 33MHz_IN pin
IRQSER = SERIRQ pin

A) Start Frame timing with source sampled a low pulse on IRQ1



H=Host Control R=Recovery S=Sample
SL=Slave Control T=Turn-around

B) Stop Frame Timing with Host using 17 IRQSER sampling period



H=Host Control T=Turn-around I= Idle.
R=Recovery S=Sample

1. Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

IRQSER Cycle Control

There are two modes of operation for the IRQSER Start Frame.

1) **Quiet (Active) Mode**: Any device may initiate a Start Frame by driving the IRQSER low for one clock, while the IRQSER is Idle. After driving low for one clock the IRQSER must immediately be tri-stated without at any time driving high. A Start Frame may not be initiated while the IRQSER is Active. The IRQSER is Idle between Stop and Start Frames. The IRQSER is Active between Start and Stop Frames. This mode of operation allows the IRQSER to be Idle when there are no IRQ/Data transitions which should be most of the time.

> Once a Start Frame has been initiated the Host Controller will take over driving the IRQSER low in the next clock and will continue driving the IRQSER low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the Host Controller will drive the IRQSER back high for one clock, then tri-state.

Any IRQSER Device (i.e., The SLC88B17x) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the Host Controller unless the IRQSER is already in an IRQSER Cycle and the IRQ/Data transition can be delivered in that IRQSER Cycle.

2) **Continuous (Idle) Mode**: Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other IRQSER agents become passive and may not initiate a Start Frame. The IRQSER will be driven low for four to eight clocks by the Host Controller. This mode has two functions. It can be used to stop or idle the IRQSER or the Host Controller can operate IRQSER in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An IRQSER mode transition can only occur during the Stop Frame. **Upon reset, IRQSER bus is defaulted to Continuous mode, therefore only the Host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next IRQSER Cycle's mode.**

IRQSER Data Frame

Once a Start Frame has been initiated, the SLC88B17x will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase the SLC88B17x must drive the IRQSER (SERIRQ pin) low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, IRQSER must be left tri-stated. During the Recovery phase the SLC88B17x must drive the IRQSER high, if and only if, it had driven the IRQSER low during the previous Sample Phase. During the Turn-around Phase the SLC88B17x must tri-state the IRQSER. The SLC88B17x will drive the IRQSER low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. (e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, (6 x 3) - 1 = 17th clock after the rising edge of the Start Pulse).

IRQSER Sampling Periods

IRQSER PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	Not Used	2
2	IRQ1	5
3	Not Used	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	IOCHK	50

The IRQSER data frame does not support IRQ2/nSMI from a logical device.

Stop Cycle Control

Once all IRQ/Data Frames have completed the Host Controller will terminate IRQSER activity by initiating a Stop Frame. Only the Host Controller can initiate the Stop Frame. A Stop Frame is indicated when the IRQSER is low for two or three clocks. If the Stop Frame's low time is two clocks then the next IRQSER Cycle's sampled mode is the Quiet mode; and any IRQSER device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks then the next IRQSER Cycle's sampled mode is the Continuos mode; and only the Host Controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

Latency

Latency for IRQ/Data updates over the IRQSER bus in bridge-less systems with the minimum IRQ/Data Frames of seventeen, will range up to 96 clocks (3.84μS with a 25MHz PCI Bus or 2.88uS with a 33MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

EOI/ISR Read Latency

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the IRQSER Cycle latency in order to ensure that these events do not occur out of order.

AC/DC Specification Issue

All IRQSER agents must drive / sample IRQSER synchronously related to the rising edge of PCI bus clock. IRQSER (SERIRQ) pin uses the electrical specification of PCI bus. Electrical parameters will follow PCI spec. section 4, sustained tri-state.

Reset and Initialization

The IRQSER bus uses RSTDRV as its reset signal. The IRQSER pin is tri-stated by all agents while RSTDRV is active. With reset, IRQSER Slaves are put into the (continuous) IDLE mode. The Host Controller is responsible for starting the initial IRQSER Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent IRQSER Cycles. It is Host Controller's responsibility to provide the default values to 8259's and other system logic before the first IRQSER Cycle is performed. For IRQSER system suspend, insertion, or removal application, the Host controller should be programmed into Continuous (IDLE) mode first. This is to guarantee IRQSER bus is in IDLE state before the system configuration changes.

TESTABILITY

The SLC88B17 provides Tri-state and NAND Tree test modes. The test modes are selected from DREQ[6:5] inputs when the nTESTIN is active

Table 4 - Test Modes

TEST MODE	nTESTIN	DREQ6	DREQ5
Normal Operation	1	X	X
Tri-state	0	0	0
NAND Chain Test	0	0	1
Reserved	0	1	X

Note: Care should be taken to avoid the “reserved” input combination

Tri-state Test
This test mode tri-states all outputs including the NAND tree outputs, BALE, and RSTDRV.

NAND Tree Mode
This test mode tri-states all output and bi-directional buffers except for BALE and RSTDRV. Every output buffer, except BALE and RSTDRV, is configured as an input in NAND Tree mode and included in the NAND chain. The first input of the NAND chain is nOWS. The NAND chain is routed counter-clockwise around the chip (eg., nOWS, nIOCHK, SD7,…). BALE is an intermediate output and RSTDRV is the final output. nTESTIN, DREQ6, DREQ5, BALE and RSTDRV pins are not included in the NAND chain.

To perform a NAND Tree test, all pins included in the NAND tree should be driven to 1, beginning with nOWS and working counterclockwise around the chip. Each pin can be toggled and a resulting toggle can be observed on BALE or RSTDRV.

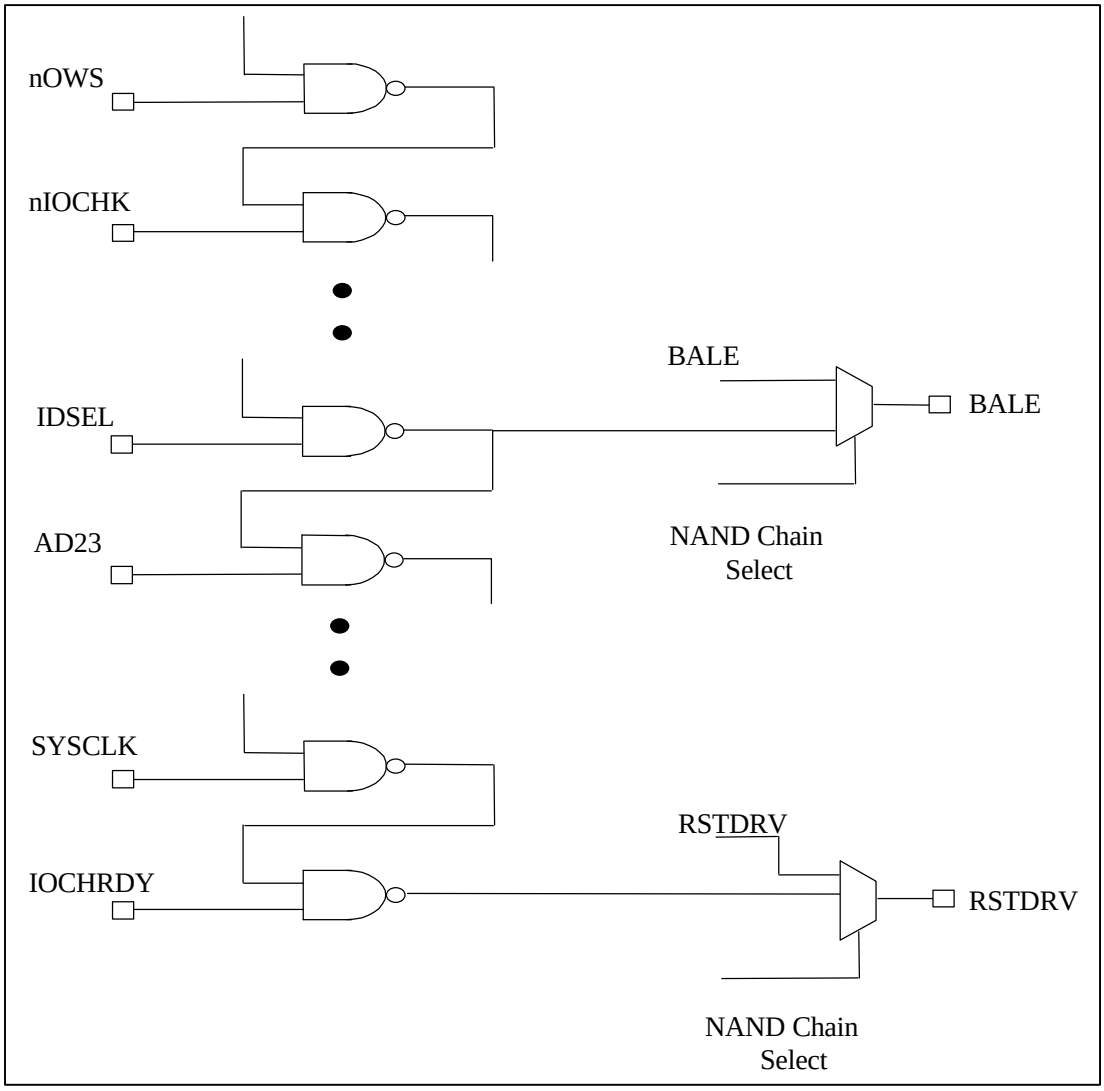


FIGURE 5 - NAND TREE DIAGAM

PACKAGE SPECIFICATION

The SLC88B17 uses a 160-pin QFP package. The mechanical dimensions and the pinout of the chip are outlined as follows.

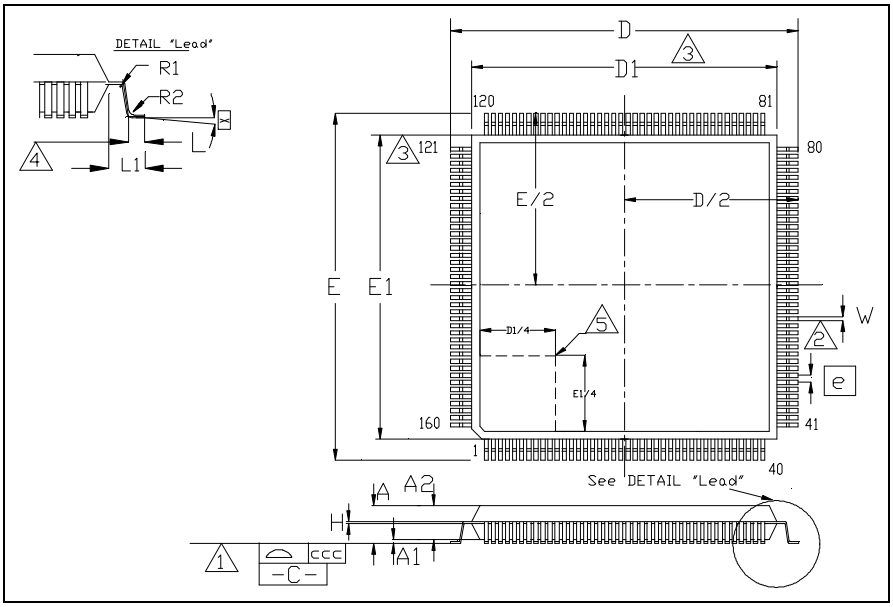


FIGURE 6 - 160 PIN QFP PACKAGE OUTLINE, 3.2MM FOOTPRINT

See Table on the following page.

	MIN	NOMINAL	MAX	REMARKS
A	~	~	4.07	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	3.1	~	3.67	Body Thickness
D	30.95	31.20	31.45	X Span
D/2	15.475	15.60	15.725	$^1/_2$ X Span Measured from Centerline
D1	27.90	28.00	28.10	X body Size
E	30.95	31.20	31.45	Y Span
E/2	15.475	15.60	15.725	$^1/_2$ Y Span Measured from Centerline
E1	27.90	28.00	28.10	Y body Size
H	0.10	~	0.20	Lead Frame Thickness
L	0.65	0.80	0.95	Lead Foot Length
L1	~	1.60	~	Lead Length
e		0.65 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.20	~	0.40	Lead Width
R1	~	0.20	~	Lead Shoulder Radius
R2	~	0.30	~	Lead Foot Radius
ccc	~	~	0.09	Coplanarity *(Assemblers)*
ccc	~	~	0.10	Coplanarity *(Test House)*

Note 1: Controlling Unit: millimeter
Note 2: Tolerance on the position of the leads is ± 0.065 mm maximum
Note 3: Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm
Note 4: Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
Note 5: Details of pin 1 identifier are optional but must be located within the zone indicated.

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