SCG2500 Synchronous Clock Generators

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

General Description

The SCG2500 is a mixed-signal phase lock loop generating CMOS outputs from an intrinsically low jitter voltage controlled crystal oscillator.

The SCG2500 can lock to one of two possible input reference frequencies at 8 kHz which is selectable using one input select pin.

Further features include an alarm output to indicate Loss of Reference, LOR, or Loss of Lock, LOL. If only one of the references is lost, the unit will disable its phase detector and will signal an alarm, but will not switch reference automatically. If both references are lost, the SCG2500 will enter a Free Run state which will guarantee a 20 ppm accurate output. Additionally, the Free Run mode may be entered manually by applying a high signal to the Free Run pin. If the unit is in Free Run mode, the Free Run status pin will be high.

The outputs may be put into the tri-state high impedance condition for external testing purposes by applying a high signal to the Reset/Tri-State pin.

The filtered 8 kHz is derived from the oscillator output. The offset between the filtered output and the reference input will change with each reference rearrangement.

The package dimensions are .775" x .8" x .35" on a six layer FR4 board with surface mount pins. Parts are assembled using high temperature solder to withstand surface mount reflow process.

Features

- Phase Locked Output Frequency Control
- Intrinsically Low Jitter Crystal Oscillator
- Two Selectable References @ 8 kHz
- Alarm Output
- Tri-Statable Oscillator and Alarm Outputs
- Force Free Run Function
- Automatic Free Run Operation upon loss of both references
- Input Duty Cycle Tolerant
- 3.3 Volt Power Supply
- Small Size: 0.775 x 0.825 inches
- Surface Mount, DIL Package

US Headquarters:
630-851-4722
European Headquarters:
+353-62-472221

Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{CC}	Power Supply Voltage	-0.5	-	+4.0	Volts	
V_I	Input Voltage	-0.5	-	+5.5	Volts	
T_S	Storage Temperature	-65.0	-	+150.0	°C	

Operating Specifications

Table 2

Parameter	Specifications	Notes
Voltage	3.3V ±5%	1.0
Current	150 mA @ 3.46V	
Oscillator Output Frequencies	1.544, 2.048, 19.44, 20.48, 44.736, 51.84, and 77.76 MHz	
Temperature Range	0 to 70°C	
Input Frequency Ref 1 and Ref 2	8 kHz	2.0
Input Jitter Tolerance	6.25 us, 10 Hz (0.05 UI @ 8000 Hz)	
Jitter Bandwidth	< 10 Hz	
Acquisition Time	Approximately 1 second	3.0
Capture/Pull-In Range	± 25 ppm Minimum	
Output Duty Cycle	40/60 % Min/Max @ 50% Level	
Output Rise and Fall Time	3 nS @ 20% to 80% output level	
Output Load	30 pF	
Alarm	LOR/LOL Status Signal Output	
Free Run Accuracy	±20 ppm	
Package	Fr4 SM 0.825” x 0.775” x 0.330”	
MTIE @ Synchronization Rearrangement	GR-253-CORE, 1999 R5-136	4.0, 4.1

Input and Output Characteristics

Table 3

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{IH}	High level input voltage	2.0	-	5.5	V	
V_{IL}	Low level input voltage	0	-	0.8	V	
T_{IO}	I/O to output valid	-	-	10	nS	
C_{OUT}	Output capacitance	-	-	10	pF	
V_{HO}	High level output voltage Ioh = -4mA	2.40	-	-	-	Vcc Min
V_{IO}	Low Level output voltage Io1 = 8mA	-	-	0.4	-	Vcc Max
T_{IR}	Input reference signal pulse width	30	-	-	nS	

Output Jitter Specifications

Table 4 — All SCG2500 Models

Frequency (MHz)	Jitter BW 10 Hz - 1 MHz pS (RMS)	m UI	Sonnet Jitter BW 12 kHz - 20 MHz pS (RMS)	m UI
1.544	TBD	TBD	TBD	TBD
2.048	TBD	TBD	TBD	TB
19.44	TBD	TBD	TBD	TBD
20.48	TBD	TBD	TBD	TBD
34.368	TBD	TBD	TBD	TBD
44.736	TBD	TBD	TBD	TBD
51.84	TBD	TBD	TBD	TBD
77.76	TBD	TBD	TBD	TBD

Input Selection / Output Response

Table 5 — All SCG2500 Models

INPUTS					OUPUTS				
Reset/ Tri-State	SEL_{AB}	REF_A	REF_B	FR	FR_{status}	Alarm	Oscillator Output	8 kHz Output	Notes
1	X	X	X	X	TS	TS	TS	TS	
0	X	X	X	1	1	1	FR	FR	
0	0	A	A	0	0	0	LRB	LRBD	
0	1	NA	A	0	0	1	U	U	5.0
0	0	NA	A	0	0	1	LRB	LRBD	
0	1	A	NA	0	0	1	U	U	5.0
0	0	A	NA	0	0	0	LRA	LRAD	
0	X	NA	NA	0	1	1	FR	FR	

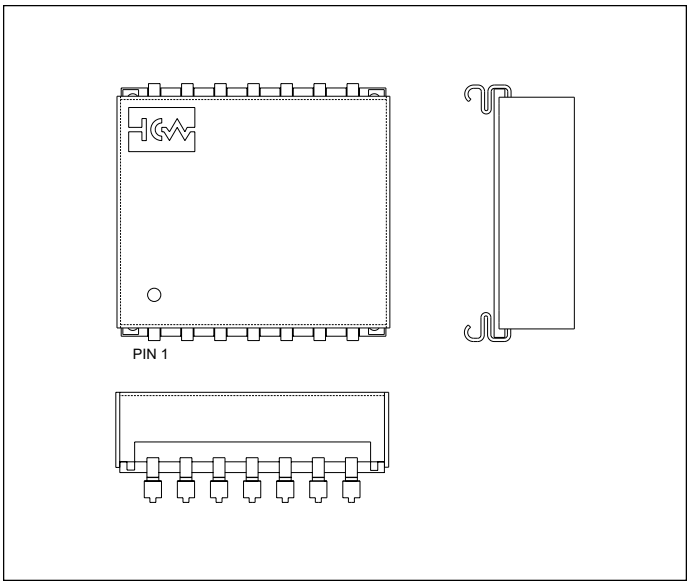
TS = Tri-State
FR = Free Run
LRA = Locked to Ref A
LRB = Locked to Reb B
U = Unstable
LRAD = Locked to Ref A and divided down
LRAB = Locked to ref B and divided down
X = Don't cart

NOTES:

1.0 Requires external regulation
2.0 Externally selectable via Input Select AB
3.0 From a 10 ppm offset in reference frequency
4.0 Entry into Free Run doesn't meet requirement for initial 2.33 seconds of self-timing
4.1 If the selected reference is removed, system response to the ALARM must be less than 10µs
5.0 On alarm assertion, switch references. If alarm is still active, force Free Run

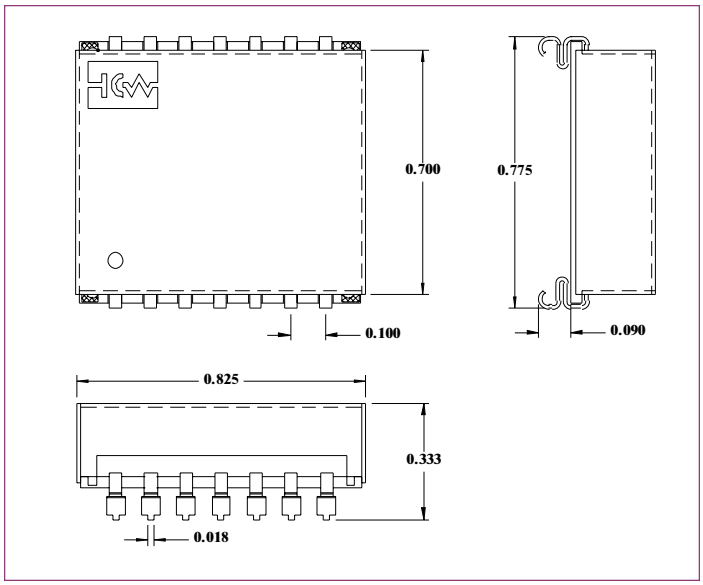
Package Outline

Figure 1



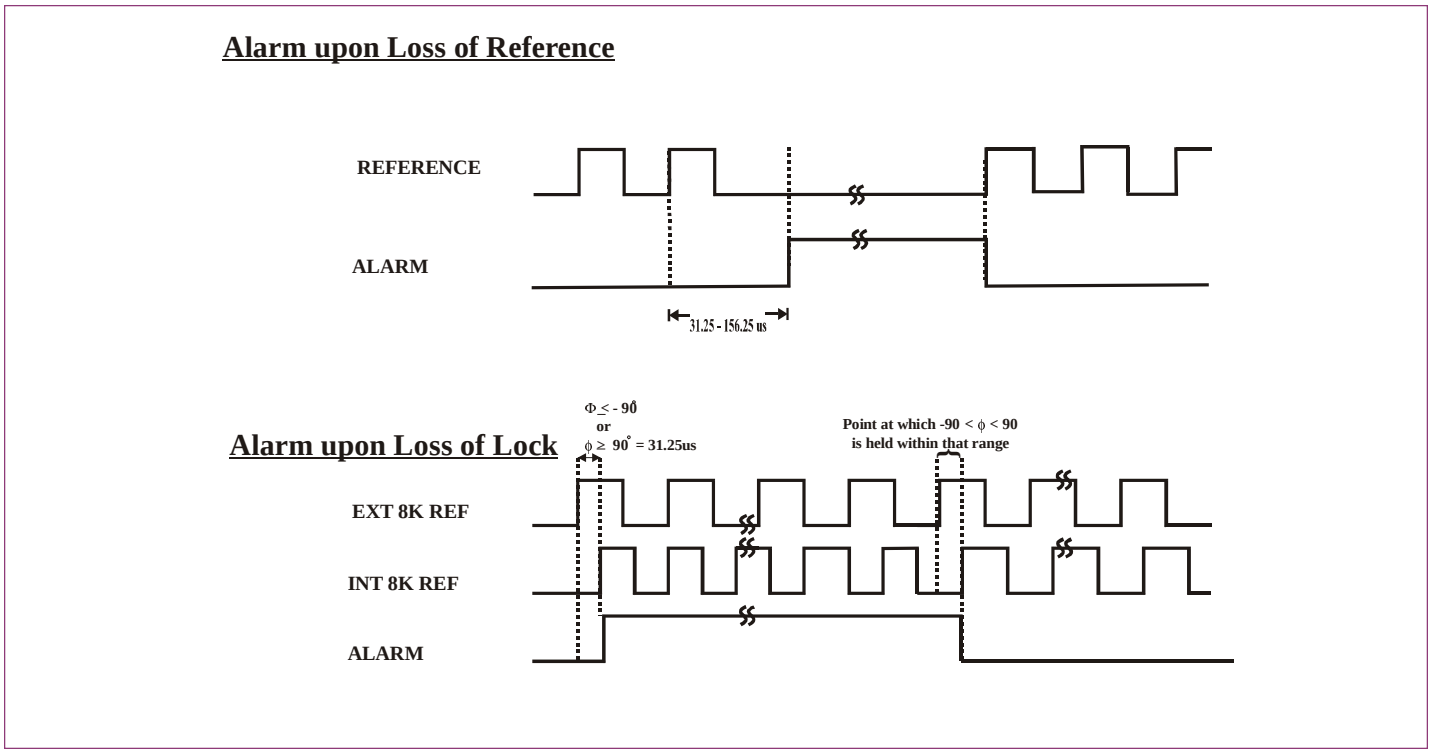
Package Dimensions

Figure 2



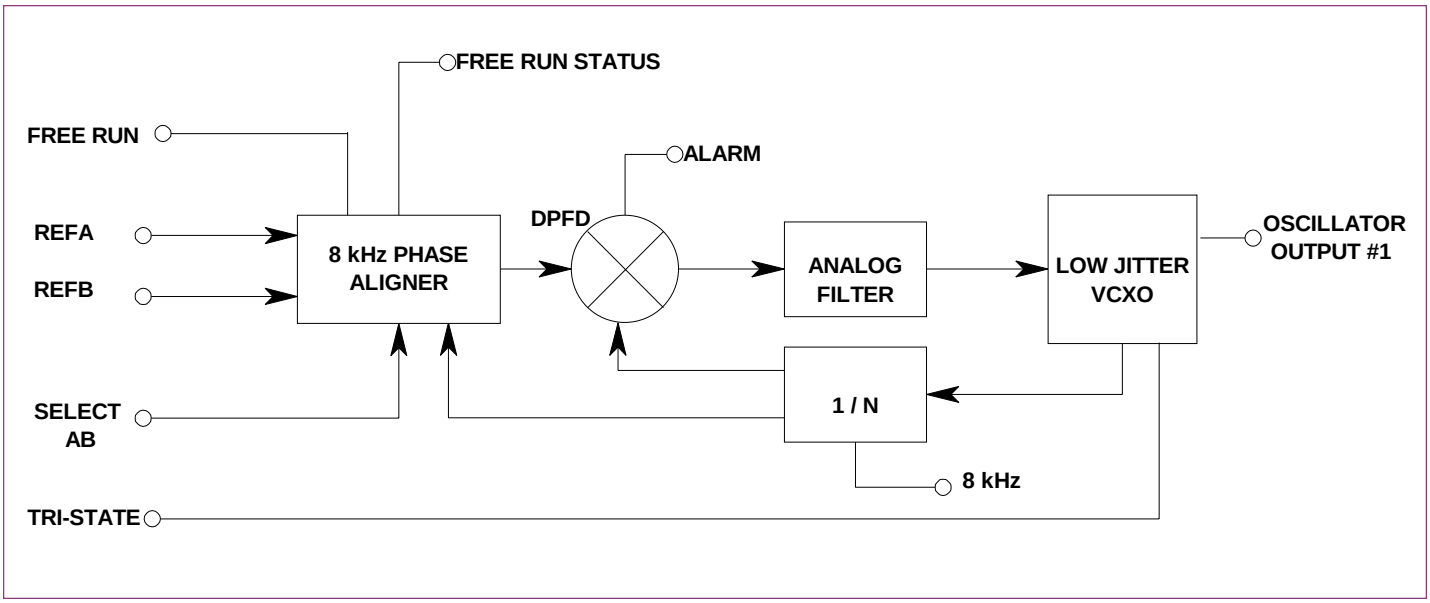
Alarm Timing

Figure 3



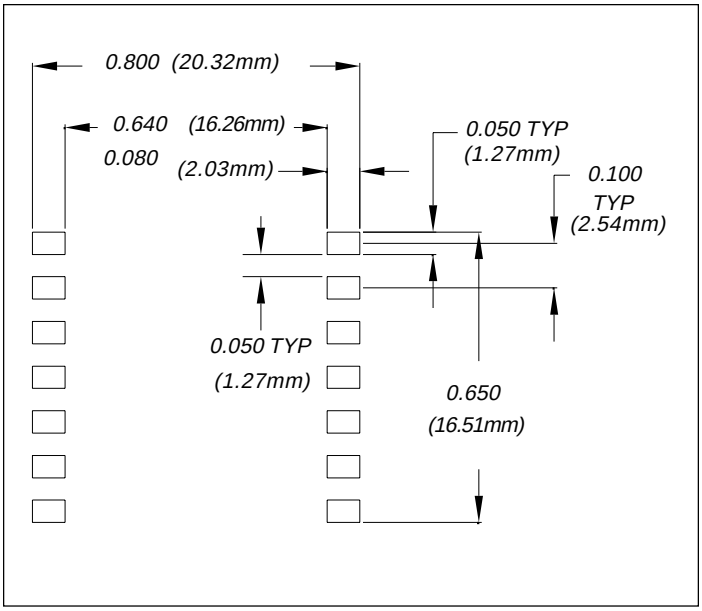
Block Diagram

Figure 4



Circuit Board Footprint

Figure 5



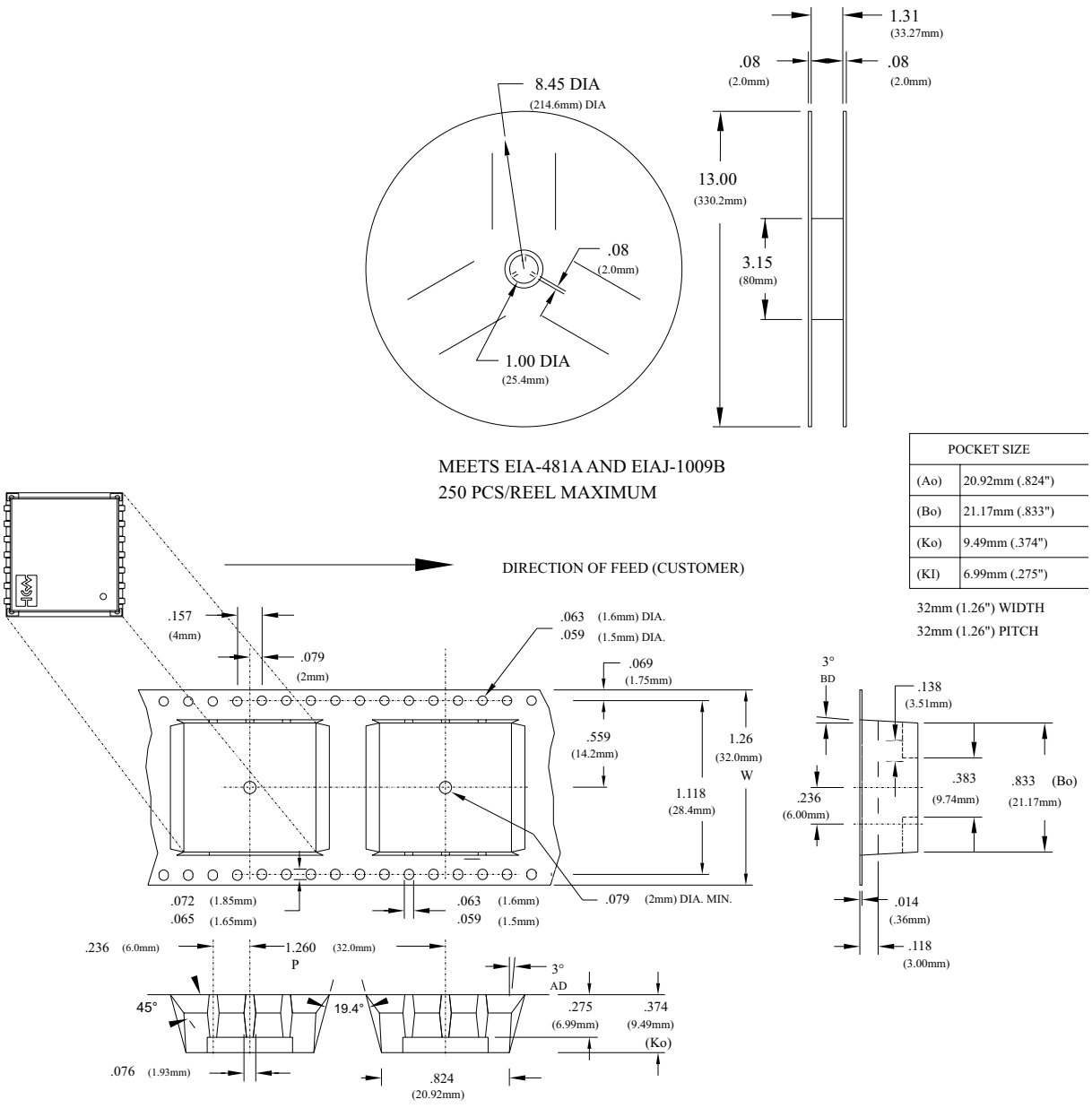
Pin Connections

Table 6

Pin	Connection
1	Filtered 8 kHz Output
2	TCK
3	TMS
4	Ground
5	Free Run / TDI (1 = Free Run)
6	Alarm Output (1 = Alarm)
7	REF B
8	REB A
9	Oscillator Output
10	Free Run Status Pin (FR = 1)
11	Vcc
12	TDO
13	Reset / Tri-State
14	Input Frequency Select AB (A = 0, B = 1)

Tape and Reel Packaging

Figure 6

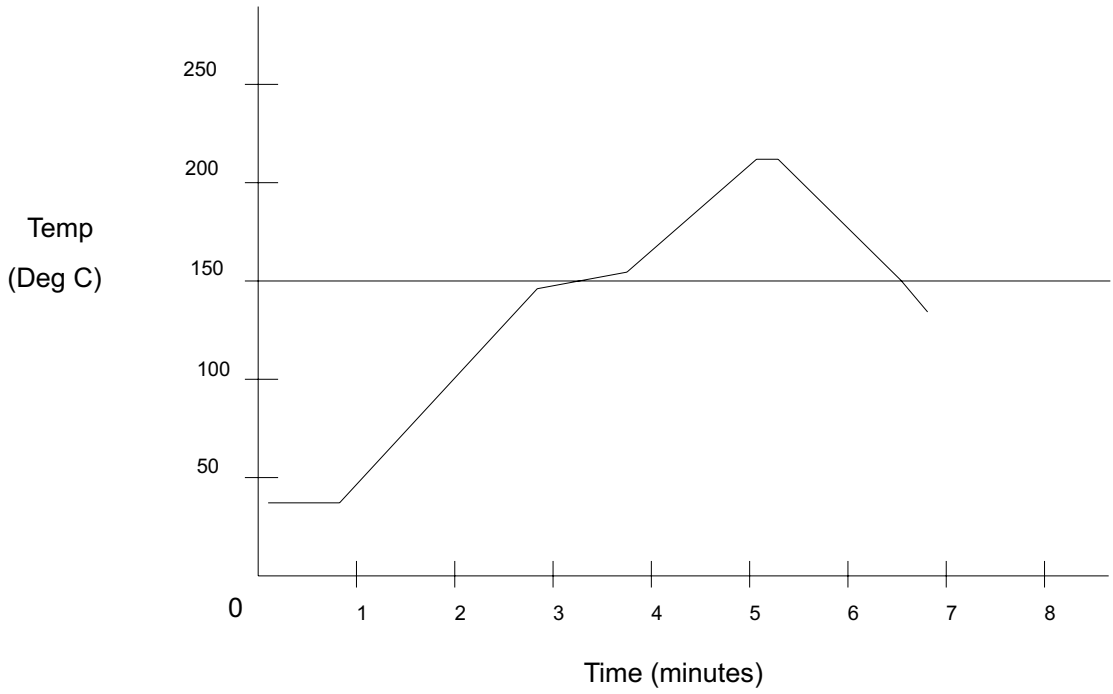


POCKET SIZE	
(Ao)	20.92mm (.824")
(Bo)	21.17mm (.833")
(Ko)	9.49mm (.374")
(KI)	6.99mm (.275")

32mm (1.26") WIDTH
32mm (1.26") PITCH

Solder Profile

Figure 7



Recommended Reflow Profile

Peak Temp:	217 Deg C
Max Rise Slope:	1.5 Deg C/Sec
Time Above 150 C:	100 Sec

Revision	Revision Date	Note
00	4/24/01	Product Release
01	7/24	Reformatted to new Style