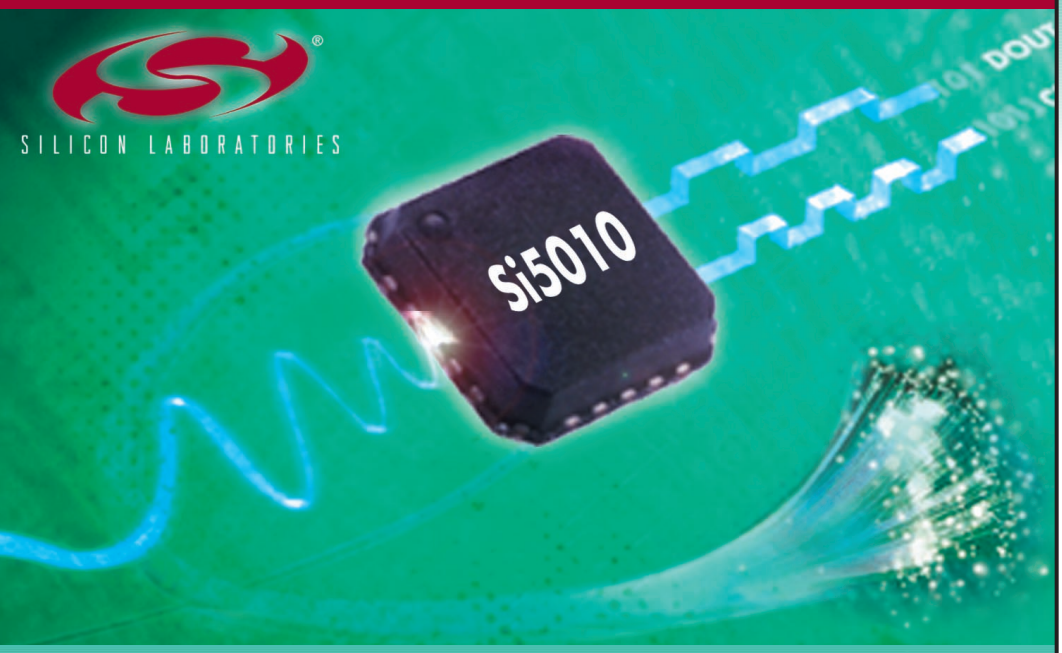
Si5010

MULTI-RATE SONET/SDH CLOCK AND DATA RECOVERY IC FOR OC-3/12, STM 1/4 APPLICATIONS



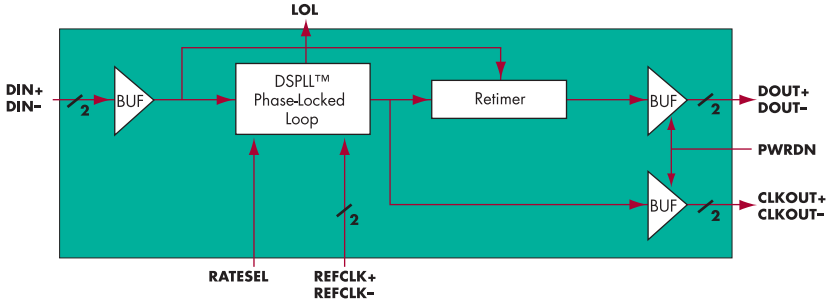
PRODUCT DESCRIPTION

The Si5010 is a fully integrated low-power clock and data recovery (CDR) IC designed for high-speed serial communication systems. It recovers timing information and data from a serial input at OC-3/12 and STM-1/4 data rates.

The Si5010 utilizes Silicon Laboratories' proprietary DSPLL™ technology to provide superior jitter performance and eliminate the external loop filter components in traditional CDR implementations. This improves jitter performance by reducing the device's sensitivity to board-level noise. In addition, the DSPLL significantly exceeds all SONET/SDH jitter requirements providing additional design margin with respect to jitter generation, tolerance, and transfer. Application is further simplified by reducing external device configuration via reference clock detection circuitry that automatically configures the device for operation with one of three common reference clock frequencies: 19 MHz, 77 MHz, and 155 MHz.

The Si5010 sets a new standard for low jitter, small size, and low power for high speed CDR devices. It consumes 293 mW (Typ OC-12) from a single 2.5V supply and comes standard in a 20-pin micro leaded package (MLP).

Si5010 BLOCK DIAGRAM



FEATURES

- Multi-rate operation: OC-3/12, STM-1/4
- Low jitter gen (<1.6mUI Typ OC-12)
- Low power: 293 mW (Typ OC-12)
- Small footprint: 20-pin MLP, 4 mm x 4 mm outside dimension
- Proprietary DSPLL™ technology eliminates external loop filter components
- Exceeds all SONET/SDH jitter specifications
- Automatic detection and configuration for 19, 77, or 155 MHz reference clocks
- Chip power down
- Loss-of-lock indication
- Single 2.5 V supply operation

APPLICATIONS

- SONET/SDH/ATM routers
- Add/drop multiplexers
- Digital cross connects
- SONET/SDH test equipment
- Optical transceiver modules
- SONET/SDH regenerators
- Board-level serial links

PRODUCTBRIEF

THE NEW STANDARD IN LOW JITTER, SMALL SIZE, LOW POWER, HIGH-SPEED, PHYSICAL LAYER DEVICES.

SILICON LABORATORIES

Si5010 OC-3/12, STM-1/4 SONET/SDH CLOCK AND DATA RECOVERY IC

SMALL SIZE, LOW JITTER, LOW POWER, INNOVATIVE PLL DESIGN

Industry's Lowest Jitter: The Si5010 exceeds all SONET jitter specifications. It has typical Jitter generation of 1.6mUI which exceeds the SONET Jitter Specifications by more than 5x.

Industry's Smallest Size: The Si5010 is the smallest OC-3/12, STM-1/4 SONET/SDH CDR available today. Because it requires no external loop-filter components, further board space savings is realized.

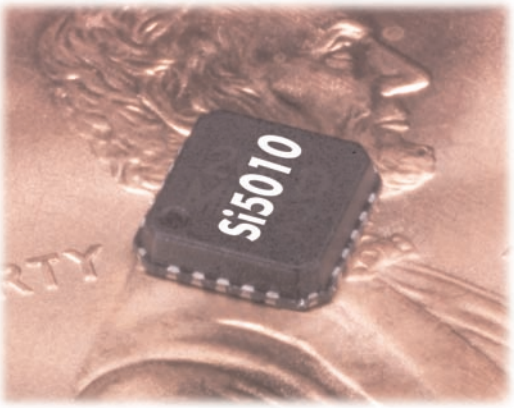
Low Power: The Si5010 is based on a single supply (2.5 V) design that only consumes 293 mW (Typ) OC-12 operation.

Proprietary DSPLL™ Technology: The phase-locked loop (PLL) within the Si5010 utilizes digital signal processing (DSP) to provide superior jitter performance and eliminate the need for external loop filter components. By keeping all PLL circuitry internal, sensitive noise entry points are eliminated. This makes the PLL less susceptible to board-level interaction, thus helping to ensure optimal jitter performance over a wide range of board designs.

DEVELOPMENT TOOLS

For quick assessment of device performance, the Si5010-EVB evaluation kit is available. This kit supports a straightforward evaluation of device performance using industry standard test measurement equipment.

Over 2x Smaller / Low Power/1.6mUI RMS jitter generation (Typ)



Si5010: 4 mm x 4 mm x 1 mm

INDUSTRY'S SMALLEST FOOTPRINT:

The Si5010 comes in a 20-pin micro leaded package (MLP) that has an outside dimension of 4 mm x 4 mm. This provides the Si5010 with a footprint that is two times smaller than comparable multi-rate CDRs.

EASY-TO-USE DESIGN

The Si5010 incorporates many features that simplify the design effort associated with high speed serial communication links.

For example, proprietary DSPLL™ technology enables robust operation over a wide range of board designs by eliminating the noise entry points introduced by the external loop filter components found in traditional CDR designs. Eliminating these discrete components saves board space and provides layout flexibility especially when the isolation these components require is considered. In addition, the Si5010 provides industry's smallest CDR footprint allowing maximum channel packing densities which is further aided by the devices low power consumption. To simplify device configuration, the Si5010 automatically detects the frequency of the supplied reference clock and self configures for operation with three common reference frequencies, 19, 77, or 155 MHz. Finally, the device significantly exceeds all SONET/SDH jitter specifications providing the design margin required to make the Si5010 a low risk solution for high speed serial links.

CONTACT INFORMATION

SILICON LABORATORIES

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PB:Si5010; REG-5,000-Dec00

ORDERING INFORMATION

Product	Description
Si5010-BM	OC-3/12, STM-1/4 SONET/SDH Clock and Data Recovery IC, -40 to 85°C
Si5010-EVB	Evaluation Board for the Si5010