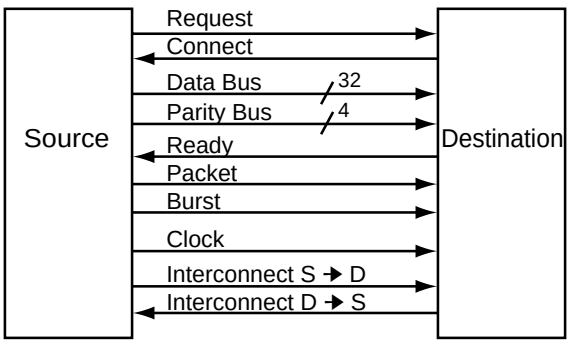
HIPPI SOURCE/DESTINATION INTERFACE CIRCUITS S2020/S2021

FEATURES

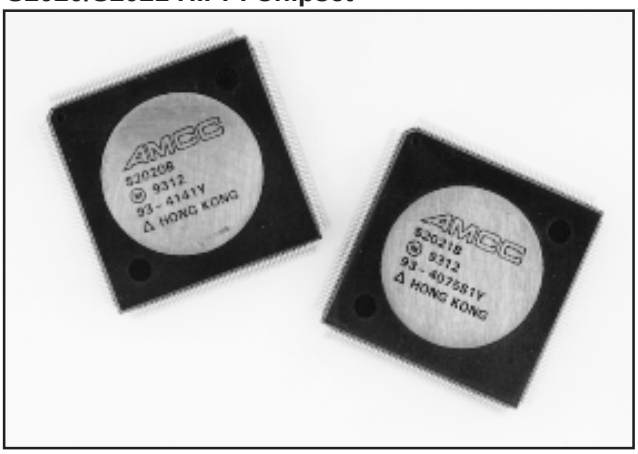
- Functionally compliant with the ANSI HIPPI standard
- 32-Bit data channel
- Equivalent single channel rate of 800 Mbits/sec
- Host-side interface single-ended TTL designed for use with external FIFO
- Channel-side interface differential ECL 10K
- Four rank data and control signal synchronization
- Byte parity checking
- Length/Longitudinal Redundancy Checkword (LLRC) generation and checking
- Automatic division of data into HIPPI bursts
- 16-Bit READY counter for flow control
- Maximum latency through both ICs Connection: 600ns, Data: 400ns
- Diagnostic modes for self test
- Standard +5V, 0V(gnd), and -5.2V power requirements
- 225-pin ceramic PGA package
- 208-pin Thermally Enhanced Plastic (TEP)

Figure 1. Interface Signal Summary



Source: ANSI X3.183–1991
High-Performance Parallel Interface.
Mechanical, Electrical, and Signalling
Protocol Specification (HIPPI-PH).

S2020/S2021 HIPPI Chipset



GENERAL DESCRIPTION

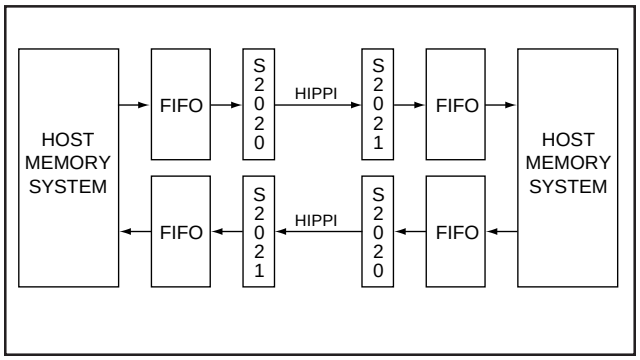
The S2020 and the S2021 are Source and Destination interface circuits, respectively, for the High-Performance Parallel Interface (HIPPI) standard. These circuits are designed to completely meet the signalling protocol of the proposed ANSI HIPPI specification: current document number X3.183–1991 They include both LLRC generation and checking as well as byte parity checking. The S2021 also incorporates a sophisticated four rank synchronization scheme to ensure that the incoming data and control signals are coupled to the local clock. Data flow control is provided by a 16-bit ready counter in both the Source and the Destination circuits. HIPPI data BURST partitioning is also provided in the Source circuit.

Architected and designed by Network Systems Corporation, the S2020 and S2021 utilize AMCC's 1.5-micron BiCMOS technology. AMCC's BiCMOS technology is especially optimized for high performance mixed mode ECL/TTL applications such as the HIPPI Source and Destination interfaces. AMCC pioneered ECL/TTL mixed mode BiCMOS capability and continues to be the leading U.S. supplier of BiCMOS VLSI circuits.

HIPPI OVERVIEW

The individual HIPPI channel is a simplex interface, meaning that data moves in one direction from the HIPPI Source (S2020) to the HIPPI Destination (S2021). Thus a fully bidirectional interface requires the use of two HIPPI channels as indicated in the System Block Diagram.

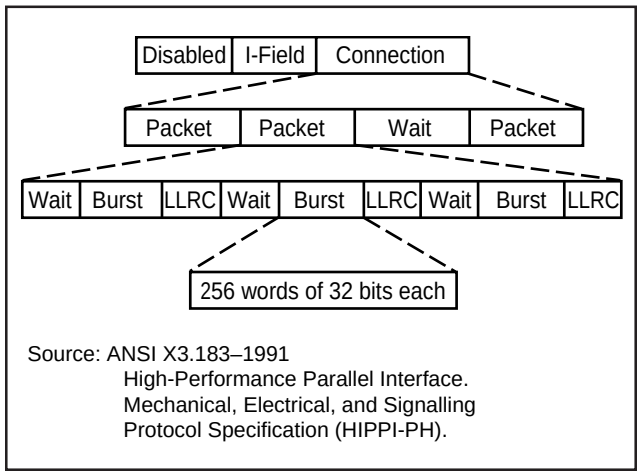
Figure 2. System Block Diagram



The transfer of data from the Source to the Destination depends on the physical connection of the two endpoints and the exchange of requesting, acknowledging, and data delimiting signals. The Source and Destination circuits both observe the state of the INTERCONNECT signals to verify a physically intact channel. If both Source and Destination are interconnected, the Source may initiate a data transfer by asserting the REQUEST signal. At the same time the Source places a 32 bit word also known as the I-Field on the data lines together with the appropriate Byte parity. The Upper Level Protocols (ULPs) controlling the Source and Destination may use this information for routing. The Destination responds to the REQUEST by asserting the CONNECT signal either for a short period while leaving the READY signal inactive to actively reject the REQUEST, or by asserting CONNECT and then asserting the READY signal to accept the REQUEST and indicate the availability of an input data buffer. The Destination can also accept the REQUEST by asserting CONNECT for a longer period without sending a READY, thus indicating a temporary delay in the availability of an input data buffer. The Source may remove the I-Field data after detecting the CONNECT signal.

Once the connection is established, data transfer can proceed according to the Physical Framing Hierarchy (see Figure 3). The basic data block is the Burst consisting of from 1 to 256 words of 32 data bits and 4 bits of odd byte parity. Each Burst is delimited by the assertion and deassertion of the BURST signal by the data Source. Every burst is followed immediately by Length/Longitudinal Redundancy Checkword (LLRC) which is the even parity for each bit for the entire length of the Burst together with the modulo 256 count of the number of words in the Burst. The count is included in the parity calculation for the least significant 8 bits of the LLRC word. For the normal full burst of 256 words, the count is all zeros (256 base 2 truncated to 8 bits).

Figure 3. Physical Framing Hierarchy



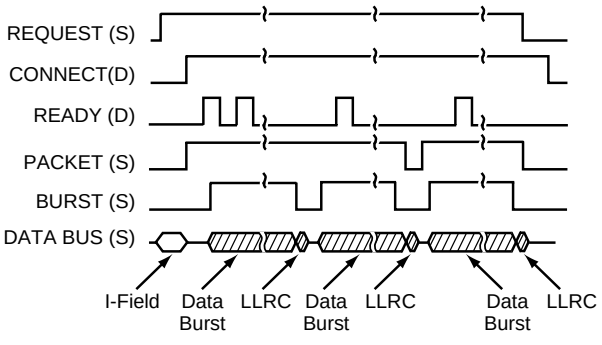
Source: ANSI X3.183–1991
High-Performance Parallel Interface.
Mechanical, Electrical, and Signalling
Protocol Specification (HIPPI-PH).

One or more Bursts are grouped as a Packet delimited by the assertion and deassertion of the PACKET signal by the Source. Wait periods are placed between Bursts and between Packets to allow synchronization adjustments between the Source and Destination circuits. A connection may contain one or more Packets. The details of the data transfer handshake are shown in Figure 4.

S2020 AND S2021 DESCRIPTION

The S2020 Source and the S2021 Destination circuits generate all of the required control and handshaking signals described above in the correct timing relationships, as well as providing Burst and Packet control, READY to BURST coordination, and LLRC generation and checking.

Figure 4. Typical HIPPI-PH Waveforms



Source: ANSI X3.183–1991
High-Performance Parallel Interface.
Mechanical, Electrical, and Signalling
Protocol Specification (HIPPI-PH).

The Host systems are the actual originator and the ultimate destination of the data sent over the HIPPI channel. The purpose of the S2020 and S2021 is to decouple the Host hardware and software from the timing and formatting details of the interface. Each circuit can be considered as having a “Host-side” and a “HIPPI-side.” The Host-side of the Source circuit accepts data from the Host FIFO and passes it to the HIPPI-side. The HIPPI-side controls the forward signals (REQUEST, PACKET, BURST and CLOCK) and receives the reverse signals (CONNECT and READY) of the HIPPI channel. The HIPPI-side of the Destination circuit receives the forward signals and controls the reverse signals of the HIPPI channel. The Host-side of the Destination delivers the received data to the Host FIFO.

The Host-side of both circuits can be thought of as consisting of four sections:

- Connect Control (for connecting/disconnecting to/from the HIPPI channel)
- Data/FIFO Control (for moving data to/from the Host logic)
- Data + Parity (for presenting data to/from the Host logic
- Status/Control (for general control of the circuit and to obtain status from the circuit)

The purpose of these circuits is to reduce the complexity of the circuitry required to mate a Host memory system to the HIPPI channel. The Host-side is primarily single-ended TTL while the HIPPI-side is primarily differential ECL. Beside meeting the signalling protocol requirements of the HIPPI standard, the circuits provide a reduction of the signal lines to the host interface.

The circuits provide diagnostic modes for testing the devices themselves plus the circuitry that interfaces to the device. In the self-test modes, the INTERCONNECT signal can be deasserted. This effectively “unplugs” the device undergoing self-test from the HIPPI channel making it unavailable for connection and thus unable to generate spurious data or control information while in the diagnostic mode.

S2020 HIPPI SOURCE DEVICE

This device meets the signalling protocol requirements for a HIPPI-Source; i.e., it controls the forward signals and receives and acts on the reverse signals.

The Host-side consists of 45 single-ended TTL inputs used for data, control and the 50 MHz clock as well as 9 single-ended TTL outputs used for control of the external FIFO and to obtain device status.

The HIPPI-side consists of 40 differential ECL outputs (forward signals), 2 differential ECL inputs (reverse signals), 1 single-ended TTL output (Source-to-Destination INTERCONNECT signal) and 1 single-ended ECL input (Destination-to-Source INTERCONNECT signal).

ELECTRICAL REQUIREMENTS

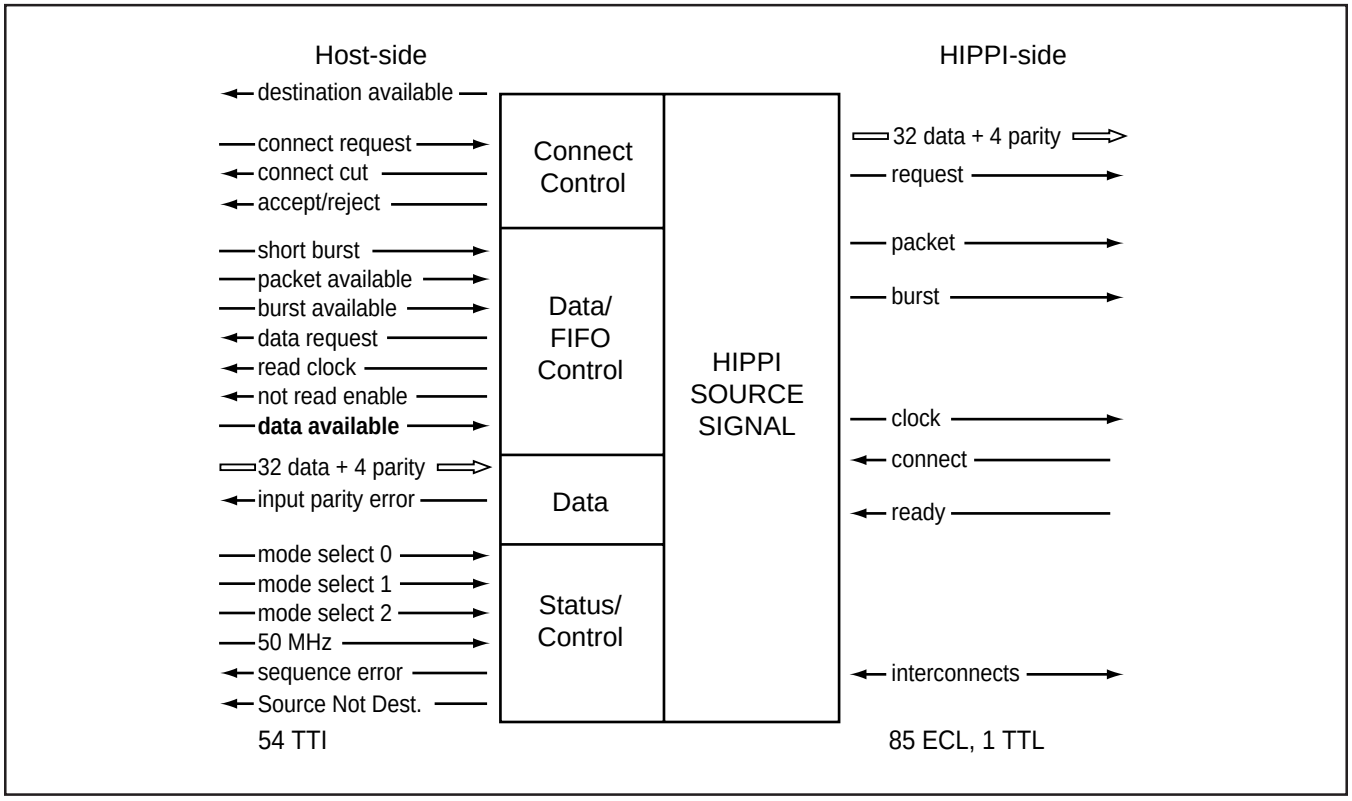
The differential ECL outputs require eighty 330 Ohm 2% resistors, one per pin. The differential ECL inputs require two 110 Ohm 2% resistors, one per input pair.

The two INTERCONNECT signals require external transmit and receive networks to reliably implement the signal swing required by the HIPPI Specification. For the Source-to-Destination INTERCONNECT (output signal), the required network is shown in Figure 10.

It should be noted that this network is only required if switching control of the INTERCONNECT signal by the Source device is desired. The network may be omitted and a simple pull-down of the Source-to-Destination INTERCONNECT via a 220 Ohm resistor to Vee may be used as indicated in the ANSI standard. For the Destination-to-Source INTER-CONNECT (input signal), the required network is shown in Figure 11.

The network is strongly recommended for use on the received INTERCONNECT signal to avoid risk of saturation when operated with a switchable INTER-CONNECT Destination device such as the S2021. It is also recommended for use in the non-switched passive pull-down applications to avoid damage to the ECL input due to transients caused by mechanical connection/disconnection cycles of the allowed cabling while Source and Destination are under power.

Figure 5. HIPPI Source Block Diagram



CONNECTION LATENCY

The Connection latency through the Source device consists of two parts: 1) The delay from the rising edge of the TTL input CONNECT_REQUEST to the assertion of the REQUEST signal in parallel with the placement of the I-Field data on the Host data bus and its availability on the HIPPI channel data bus (4 clock cycles), and 2) the delay from the detection of the CONNECT signal for the 17th clock cycle and the assertion of the TTL outputs CONNECT_OUT and ACCEPT/REJECT to the Host (3 to 4 clock cycles). The total connection latency in the Source device ranges from 7 to 8 clock cycles. This does not include cable delay or Destination processing.

DATA LATENCY

The data latency through the Source device is defined as the delay from the rising edge of the BURST_AVAILABLE signal and the assertion of the BURST signal on the HIPPI channel. The data latency is 4 clock cycles. This does not include cable delay or Destination processing.

SOURCE CONNECT CONTROL

Connection control is provided by four control signals and two error flags on the Host-side of the Source device. Using the signals the Host can “request” a connection to a Destination and monitor the results (whether the Destination has accepted or rejected the connection request). Timeout mechanisms, if required, must be provided by the Host hardware or software.

DESTINATION_AVAILABLE (output) [DSTAV]*

A high level on this signal indicates an active Destination-to-Source INTERCONNECT signal. Low indicates inactive INTERCONNECT.

CONNECT_REQUEST (input) [CNREQ]

This signal when high directs the Source device to read the I-Field from the Host System (see HIPPI Data Control, page). When a valid I-Field is read, it is placed on the HIPPI channel and the HIPPI REQUEST signal is asserted. The information in the I-Field can be used by intermediate HIPPI nodes (nodes that are not end-points) to control the routing of the associated connection. The Host would then monitor the CONNECT_OUT and ACCEPT/REJECT signals to determine the state of the connection.

*Bracketed signal name refers to pin matrix on pages 20–23 (all signals).

CONNECT_OUT (output) [CNOUT]

This signal, along with the CONNECT_REQUEST and ACCEPT/REJECT signals defines the current state of the HIPPI connection. A high level indicates active acceptance or rejection of a requested connection.

ACCEPT/REJECT (output) [ACREJ]

This signal along with the CONNECT_REQUEST and CONNECT_OUT signals defines the current state of the HIPPI connection. A high level indicates active acceptance of a requested connection.

SEQUENCE_ERROR (output) [SQERR]

This signal when high indicates the presence of either a Source error state (PACKET_AVAILABLE dropped before the first word of Burst transmitted or CONNECT_REQUEST is reasserted before Destination has deasserted CONNECT) or Destination error state (CONNECT is detected before REQUEST has been asserted).

SOURCE_NOT_DESTINATION (output) [SRNDS]

This signal is used to distinguish between a Source error (logic 1 state) and a Destination error (logic 0 state).

DATA/FIFO CONTROL

This interface provides control to the Source Host system, of the flow and organization of the data to be transferred over the HIPPI channel. It is intended for this interface to attach to an external synchronous FIFO, which is in turn attached to the Source Host memory system. Recommended FIFO's capable of buffering 4 or more Bursts are:

IDT P/N 72225LB20 1K x 18 bits

IDT P/N 72235LB20 2K x 18 bits

IDT P/N 72245LB20 4K x 18 bits

The signals of this interface can be divided into three groups; Source FLOW control, Source FIFO control, and HIPPI data control.

SOURCE FLOW CONTROL

After a HIPPI connection is established, data transfer from the Source Host to the Destination Host is enabled by the presence of data from the Source Host and the current ability of the Destination Host to accept data. The presence of data from the Source Host is indicated to the Source device on the Source FLOW control lines. The ability of the Destination Host to receive data is determined by the Source device's FLOW control circuit.

The Source device FLOW control circuit consists of a set of 16-bit counters that automatically maintain the number of READYs received from the HIPPI Destination and the number of BURSTs sent to the HIPPI Destination. In the Source device, these counters are reset when the HIPPI channel is disconnected, and then enabled when the HIPPI channel is reconnected. When the BURST counter and the READY counter are equal, data transfer will be disabled and both counters are enabled. When the BURST counter and the READY counter are not equal and their difference is not 65535 [(2exp16)-1], data transfer will be enabled and both counters are enabled. When the difference between the BURST counter and the READY counter is 65535, data transfer is enabled and the READY counter is disabled. Disabling the READY counter results in a limit of 65535 pending READYs for the HIPPI connection.

The Source FLOW control signals are:

BURST_AVAILABLE (input) [BSTAV]

This signal when held high enables the initiation of a data transfer from the FIFO, through the Source device, to the HIPPI channel. When held low this signal prevents the initiation of a data transfer. A transition from high to low after a data transfer has been initiated has no effect on that transfer (i.e., the current Burst will terminate normally).

DATA_AVAILABLE (input) [DATAV]

This signal when high indicates the current presence of at least one more word from the Source Host FIFO and enables the synchronous load of the data bus into the Source device. When low this signal disables the data loading. It is intended that this signal be driven by the Not Empty flag of the FIFO. In this configuration any interruption of the data flow due to the FIFO not being refilled by the host will result in a Short Burst with normal LLRC and Burst termination. This signal must be reasserted and the BURST_AVAILABLE signal reasserted to start a subsequent Burst.

DATA_REQUEST (output) [DTREQ]

This signal indicates the current ability of the HIPPI Destination to accept data. When high the signal indicates a current connection on the HIPPI channel and the inequality of the BURST and READY counters in the Source device FLOW control circuit. When low, (and during a HIPPI channel connection) the signal indicates the equality of the BURST and READY counters in the Source device FLOW control circuit, i.e., the Source has sent one BURST to the HIPPI Destination for each READY received from that Destination.

SOURCE FIFO CONTROL

When a data transfer is enabled, the Source device will initiate read operations of the Source Host FIFO by activating the Source FIFO control lines.

The Source FIFO control signals are:

READ_CLOCK (output) [RDCLK]

This signal is a continuous 25 MHz clock synchronous with the internal clocks of the Source device and the HIPPI channel differential ECL CLOCK signal. The signal is intended to be used together with NREN to control the read function of the FIFO and as a reference for timing critical Host-side control signals such as SHORT_BURST and PACKET_AVAILABLE. This signal is intended to drive the 'read clock' input of the Source Host FIFO system.

NOT_READ_ENABLE (output) [NRDEN]

This signal when held low, is used to strobe data from the FIFO to the Source device. This signal is used as a gate of the 25 MHz TTL RDCLK for the synchronous operation of the FIFO. This signal is intended to drive the 'read enable' input of the Source Host FIFO system.

HIPPI DATA CONTROL

PACKET_AVAILABLE (input) [PKTAV]

This signal when high causes the Source device to start a Packet if Bursts are available. When brought low, this signal will end the Packet.

SHORT_BURST (input) [SHBST]

This signal when high while PACKET_AVAILABLE is low indicates presence of I-Field data at the Source device input data lines. During a Burst, a high level indicates that the current data word is the last word of a Short Burst.

Each read operation performed by the Source device reads a Data/Parity word, and an associated HIPPI data control field consisting of the PACKET_AVAILABLE and SHORT_BURST signals. Because the HIPPI data control field is to be read in parallel with the associated DATA and PARITY, these (two) bits can be written by the Source Host into the Source Host FIFO as the DATA and PARITY are transferred into it. As the Source device reads each word from the Source Host FIFO, the HIPPI data control field specifies what type of HIPPI data operation is to be performed.

The three basic types of HIPPI data operations are: I-Field, HIPPI PACKET control, and HIPPI BURST control. The HIPPI data control signals defining these data types are shown on the HIPPI Data Control Table.

HIPPI DATA CONTROL SIGNALS		
	SHORT_BURST (input) [SHBST]	PACKET_AVAILABLE (input) [PKTAV]
IDLE. No PACKET or BURST onto HIPPI channel	0	0
Assert PACKET onto the HIPPI channel*	0	1
Associated data is a HIPPI I-Field	1	0
Associated data is last word of HIPPI Burst	1	1

When the Source Host initiates a HIPPI CONNECT_REQUEST, the Source device performs read operations until a HIPPI I-Field is read. The Source device recognizes a HIPPI I-Field by decoding the HIPPI data control lines. Once a HIPPI I-Field is presented to the Source device, the REQUEST line will be asserted on the HIPPI channel and the I-Field will be put on the HIPPI channel data bus. By identifying the HIPPI I-Field in this way, the Source Host can effectively queue several connections in the FIFO and also enter primary and secondary I-Fields for single connections to support alternate paths for connect reject retries.

When data transfers are enabled, as described above, the HIPPI data control field specifies what partitioning operations are to be performed by the Source device on the associated data word. The main partitioning operations are: begin HIPPI Packet, maintain HIPPI Packet, terminate HIPPI Packet, auto-burst termination, and explicit (short) burst termination.

The three HIPPI Packet functions control the organization of data into HIPPI Packets. The auto-burst termination allows the Source device to automatically delimit the unbounded data from the Source Host FIFO into HIPPI Bursts of 256 (max) words each. The Short Burst termination allows the Source Host to specify BURST boundaries for HIPPI data bursts. In addition to the explicit Short Burst and auto-burst terminations, the Source device will terminate a HIPPI Burst if the HIPPI Packet is terminated at a non-256 word boundary or if the Source Host supply of data expires on a non-256 word boundary.

*The Source device will not assert Packet onto the HIPPI channel until the first data Burst of the Packet is sent. This prevents the possible generation of a zero-Burst Packet (illegal) onto the HIPPI channel.

The sequence of control signals and data presented to the HIPPI channel by the Source device meet all the requirements of the HIPPI specification. There is no need for the Source Host to insert wait intervals (dummy words) in the FIFO stream to provide the required wait intervals between PACKET and BURST (the FIFO can be 100% utilized for HIPPI I-Field and data). The Source device will automatically generate LLRC and append it to the end of each terminated HIPPI Burst regardless of how the Burst was terminated. It is the responsibility of the Source Host to prevent multiple Short Bursts in one Packet.

The Source device automatically formats the transferred data into packets and bursts with LLRC. The Source device counts the number of data words received from the FIFO and uses this number as the "seed" for the LLRC calculation.

DATA AND PARITY

The Source Host presents the HIPPI I-Field and Data to the HIPPI Source device on the TTL DATA AND PARITY interface.

32_DATA_+_4_PARITY (inputs) [DATxx,PARxx]

These lines are used for the I-Field during the connection sequence and for data during Burst transfers.

INPUT_PARITY_ERROR (output) [INPRR]

Parity is checked just before the data leaves the Source device (i.e. at the inputs to the differential drivers of the HIPPI channel). Parity errors are reported on a word by word basis. Upon detecting a parity error for a given word, this signal is set high for the duration of the next word's clock cycle (approximately 40 nsec).

Note: All parity errors are indicated but no recovery action is taken by the Source device. If there is a parity error detected, then the data and the bad parity are passed through the Source.

CHIP STATUS/CONTROL

Overall control of the HIPPI Source device is provided to the Source Host by the STATUS/CONTROL interface, which allows the Source Host to control the device clock frequency and phase (if necessary), and to select the operating mode of the Source device.

50_MHZ (input) [50MHZ]

This 50 MHz TTL clock is divided by 2 to generate a 50% duty cycle 25 MHz clock for all internal timing functions of the Source device and as the generated and transmitted HIPPI channel CLOCK signal. This input also latches the MODE_SELECT inputs on its rising edge. The phase of the resulting 25 MHz clock is controllable by the phase of the asserted RESET mode described below.

SOURCE DEVICE OPERATING MODES

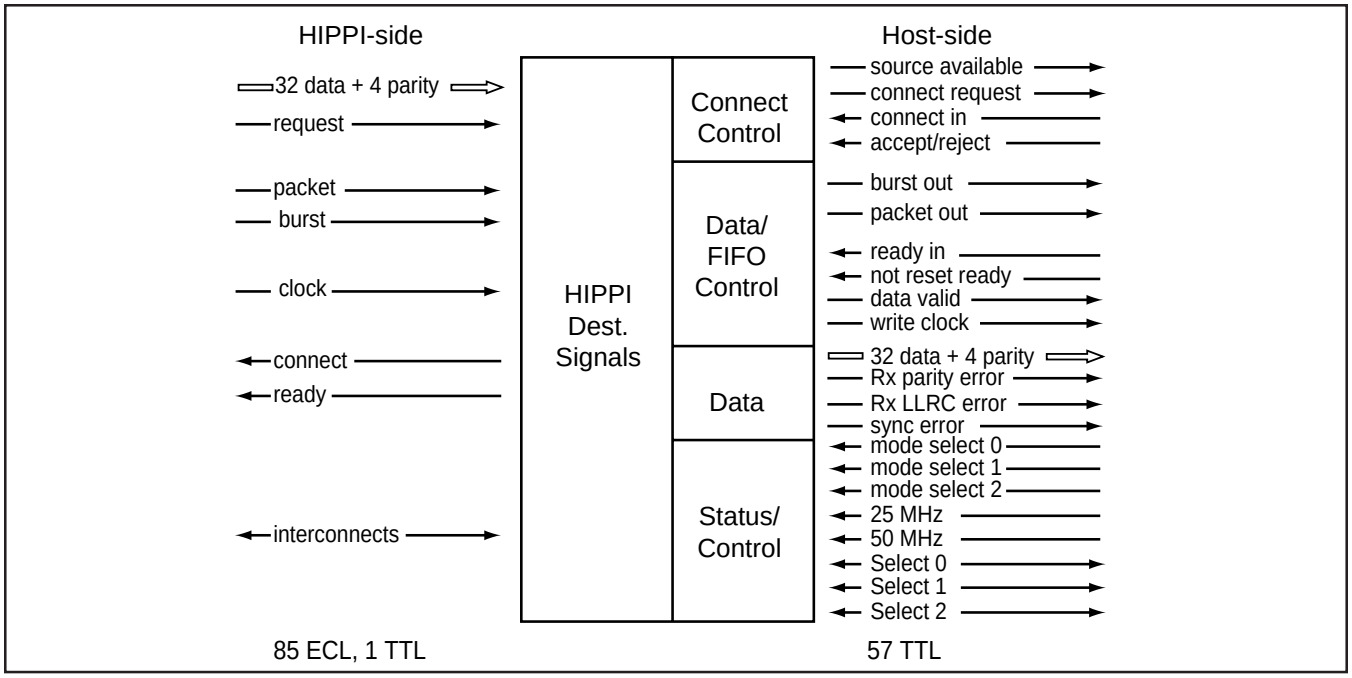
The Source device has several operating modes, which require external selection by the Source Host. Also provided is a 'board test' mode that may be used by the Source Host as a part of a system diagnostic routine. The Source Host selects the operating mode with the two lines, MODE_SELECT_0 and MODE_SELECT_1 [MSELx]. For numerical reference, MODE_SELECT_1 is the most significant bit. MODE_SELECT_2 should be held at a TTL logic zero (ground) for in-board operation of the Source device.*

Mode 0 (00 on mode select bus) is device reset. In the reset mode, all internal registers are initialized, and all device outputs are forced inactive including the HIPPI Source-to-Destination INTERCONNECT [SDIC] output. The ability to control the phase of the 25MHz clock (and the READ_CLOCK output) which is generated by dividing the 50_MHZ input by 2 is also provided by this mode.

Mode 1 (01) is the board test mode. In this mode, the Source device provides a means to verify connection and operation of the interface between the Source Host and the Source device completely independent of the HIPPI channel. In this mode, the Source-to-Destination INTERCONNECT [SDIC] signal is forced inactive. When the Source Host initiates a Connection Request by asserting CONNECT_REQUEST, the Source device advances the FIFO to the first I-Field, reads the I-Field, and then simulates a Connect Accept on the HIPPI channel, asserting the CONNECT_OUT and ACCEPT/ REJECT signals to the Source Host. The Source Host will then provide 'test' data bursts to the Source device through the FIFO, as it would for a functional data transfer, and the Source device will pass the 'test' data through the LLRC and parity check functions. The data will also appear at the HIPPI-side data outputs, but since the Source device is not in the functional or wait Modes the Source-to-Destination INTERCONNECT signal is inactive. The only difference to the Source Host between a functional transfer and a 'test' transfer is that the first data word of each 'test' burst must be the expected LLRC of the previous 'test' burst. By providing the expected LLRC, the Source device can compare its generated LLRC with the Host's expected LLRC,

*The active state of MODE_SELECT_2 is used for manufacturing test of the Source device.

Figure 6. HIPPI Destination Block Diagram



and thus verify the integrity of the DATA, PARITY, and DATA/FIFO CONTROL busses. This test routine continues until the Mode is changed or until a mis-compare is detected between the Host's expected LLRC and the device's generated LLRC. When a mis-compare is detected, the simulated connection is terminated and CONNECT_OUT is deactivated. Mode 0 (reset) clears the board test mode.

Mode 2 (10) is the WAIT mode. This mode provides an interlock device between the Source Host and the HIPPI channel that requires the Source Host to acknowledge an inactive Destination-to-Source INTERCONNECT [DSIC] before an active DSIC signal is processed. In this mode the Source-to-Destination INTERCONNECT [SDIC] is active. The requirement upon the Source Host is that if DESTINATION_AVAILABLE is inactive and the Source Host is waiting for it to become active, the Source device must be put into Mode 2. Once DESTINATION_AVAILABLE is active, the Source device must be put into Mode 3 to initiate further operations.

Mode 3 (11) is the operational mode. This mode activates the Source-to-Destination INTERCONNECT signal and enables the functional operation of all the Source device interfaces.

NOTE: The only time DESTINATION_AVAILABLE will go from inactive to active is if Destination-to-Source INTERCONNECT is active while the Source device is brought from Mode 0 (reset) to Mode 3 (operational) or if the Source device is in Mode 2 (wait).

S2021 HIPPI DESTINATION DEVICE

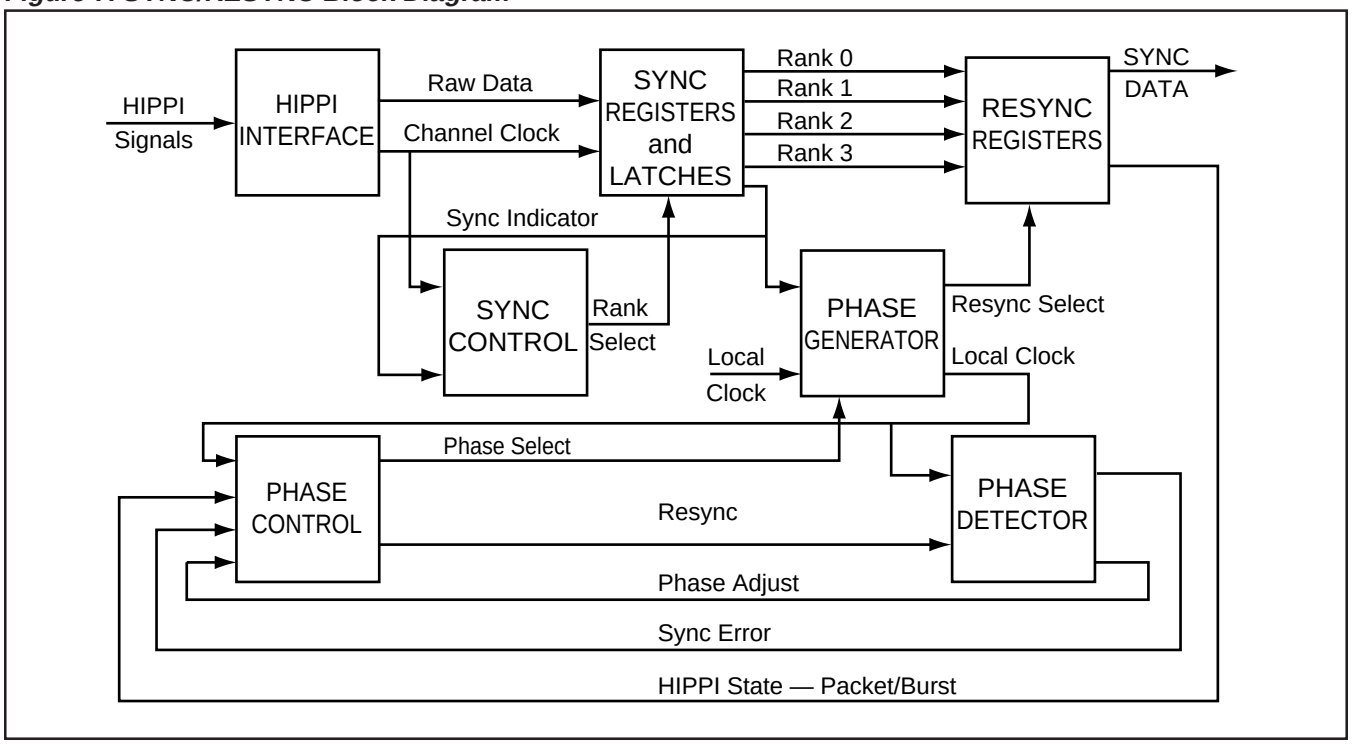
This chip meets the signalling protocol requirements for a HIPPI-Destination, i.e., it controls the reverse signals and receives the forward signals.

The HIPPI-side consists of 40 differential ECL inputs (forward going signals), 2 differential ECL outputs (reverse signals), 1 single-ended ECL input (Source-to-Destination INTERCONNECT signal), and 1 single-ended TTL output (Destination-to-Source INTERCONNECT signal).

The Host side consists of 45 single-ended TTL outputs used for data, FIFO control and status, 9 single-ended TTL inputs used for chip control, a 25 MHz clock and a 50 MHz clock and 3 TTL Bidirectional I/O.

In addition to the signal translation and control handshake functions, the Destination device provides a four stage "elastic store" for the buffering of the data, parity, and control information received from the HIPPI channel. This internal FIFO (not to be confused with the external multi-Burst size FIFO) together with a digital phase locked loop structure allow the HIPPI channel clocked information to be synchronized to the local (Host-side) 25 MHz clock. The use of the combined 50 MHz and 25 MHz clocks allow tracking of the synchronizer through more than 1200 degrees of phase "slip" or error between received HIPPI clock and the local clock. In a normally operating HIPPI channel, the accumulated

Figure 7. SYNC/RESYNC Block Diagram



phase error is re-zeroed during the inter-burst/packet Wait period by resynchronization. Since multiple nodes could be in the channel between the originating Source and the final Destination, the inter-burst Wait states may have been “consumed” before the data is received. The large phase tolerance of the synch/resynch circuitry (shown in Figure 7) in the Destination device allows 48 consecutive Bursts with missing Wait states to be received before synchronization is lost. A maximum rate transfer through a chain of 30 nodes, all with worst-case jitter, operating at progressively worse frequency margins, and all requiring a ‘dropped’ cycle at the same time would be required between the originating Source and the final Destination to produce 48 consecutive missing Wait cycles.

ELECTRICAL REQUIREMENTS

The resistors needed to complete the electrical requirements of the HIPPI-Destination interface are four 330 Ohm 2% resistors, one per pin of differential ECL outputs, and forty 110 Ohm 2% resistors, one per pair of differential ECL inputs

The two INTERCONNECT signals require external transmit and receive networks to reliably implement the signal swing required by the ANSI standard. For the Destination-to-Source INTERCONNECT (output signal), the required network is shown in Figure 10.

This network is only required if switching control of the INTERCONNECT signal by the Destination device is desired. The network may be omitted and a simple pull-down of the Destination-to-Source INTERCONNECT via a 220 Ohm resistor to Vee may be used as indicated in the ANSI standard. For the Source-to-Destination INTERCONNECT (input signal), the required network is shown in Figure 11.

CONNECTION LATENCY

The connection latency through the Destination device consists of two parts:

1) the time between the arrival of the REQUEST signal on the HIPPI channel from the Source device, to the presentation by the Destination device of the I-field to the TTL data lines and assertion of CONNECT_REQUEST ranges from 4 to 5 clock cycles;

2) the time between assertion of CONNECT_IN signal by the host (to accept the connection request), to the assertion of the CONNECT signal by the Destination device on the HIPPI channel is 2 clock cycles.

The Destination device connection latency therefore ranges from 6 to 7 clock cycles. This does not include local host connection processing (the time it takes the host to decide whether or not to accept a particular connection request).

DATA LATENCY

The data latency through the Destination device is defined as the time between detection of the BURST signal by the Destination device from the HIPPI, to the presentation of the data to the FIFO on the TTL data lines and the assertion of the DATA_VALID line. The data latency ranges from 2 to 6 clock cycles. There is no response by the Destination device on the HIPPI channel to data reception.

CONNECT CONTROL

Connection control is provided via the four signals in the "Connect Control" area on the Host-side of the Destination device. With this interface, the Host can monitor when a Connect Request or Disconnect Request comes in from the HIPPI Source, and then initiate the appropriate action in response to the request.

SOURCE_AVAILABLE (output) [SRCAV]

High indicates an active Source-to-Destination INTERCONNECT signal while the Destination device is in the on-line mode. Low indicates an inactive Source-to-Destination INTERCONNECT signal or the Destination device commanded to the off-line or disabled mode.

CONNECT_REQUEST (output) [CONRQ]

This signal indicates the state of the REQUEST signal on the HIPPI channel. High indicates a Connect Request function from the HIPPI channel, resulting from an asserted REQUEST signal while the Destination device is in a functional operating mode with Connect Requests enabled. Low indicates either a false REQUEST signal on the HIPPI channel, a disabled Connect Request at this device, or that the Destination device is in a non-functional mode.

CONNECT_IN (input) [CONIN]

This signal controls the Connect Request and Response functions of the Destination device on the HIPPI channel. A low on this input will hold the CONNECT signal on the HIPPI channel inactive, and will enable the REQUEST signal from the HIPPI channel to control the CONNECT_REQUEST output of this Destination device.

During a Connect Request, asserting this input initiates one of two responses to the Request; Accept or Reject the Request. The desired response is selected with the ACCEPT_REJECT input, described next. If a Connect Request is accepted, holding this input high will maintain an asserted CONNECT signal on the HIPPI channel, while dropping this input will deassert the CONNECT signal (Disconnect Function). If a Connect Request is rejected, holding this input high will maintain a deasserted CONNECT signal on the HIPPI channel (after the four cycle reject sequence) and disable further Connect Requests, while dropping this input will also maintain a deasserted CONNECT signal but will enable further Connect Requests.

ACCEPT_REJECT (input) [ACCRJ]

This input specifies the response to generate when CONNECT_IN is asserted during a Connect Request. A high on this input when CONNECT_IN is asserted will generate an Accept response, i.e., the CONNECT signal on the HIPPI channel will be asserted and will remain asserted until a Disconnect Function is initiated (CONNECT_IN is deasserted). A low on this input when CONNECT_IN is asserted will generate a Reject response, i.e., the CONNECT signal on the HIPPI channel will be asserted for four cycles then fall and remain deasserted until the response for the next Connect Request is initiated. The ACCEPT_REJECT signal needs to be valid only for the first cycle of the asserted CONNECT_IN input.

Note: The host can have the Destination device automatically respond to connection requests by tying the CONNECT_REQUEST output to the CONNECT_IN input. In this case, the ACCEPT/REJECT signal would be used as an "available/busy" signal. While ACCEPT/REJECT was held low all connection requests would be rejected.

DATA/FIFO CONTROL

This interface provides control to the Destination Host system over the flow of data transfers on the HIPPI channel, and provides control of data transfer from the Destination device into the Destination Host system. It is intended for this interface to attach to an external synchronous FIFO or DMA mechanism which, in turn, attaches to the Destination Host memory system. Recommended FIFO's capable of buffering 4 or more full Bursts are:

IDT P/N 72225LB20 1K x 18 bits
IDT P/N 72235LB20 2K x 18 bits
IDT P/N 72245LB20 4K x 18 bits

The signals of this interface can be divided into three groups: Destination FLOW control, Destination FIFO control, and HIPPI data control.

DESTINATION FLOW CONTROL

After a HIPPI connection is established, data transfer from the Source Host to the Destination Host is enabled by the presence of data from the Source Host and the current ability of the Destination Host to accept that data. Although this function is performed at the HIPPI Source, the HIPPI Destination signals its current buffer capacity to the Source via the READY signal on the HIPPI channel.

The Destination FLOW control circuit consists of a set of modulo 64K counters that maintains the current Buffer capacity, the number of READYs sent to the HIPPI Source, and the number of Bursts received from the HIPPI Source. At initialization (Destination device reset) all of these counters are reset. When the Source-to-Destination INTERCONNECT [SDIC] signal is true and the Destination device is in a functional mode, the Destination Host may initialize the Buffer counter to the number of HIPPI Bursts that it can accept. When a Connect Request is accepted, the Destination device will automatically generate legal READY pulses and increment the READY counter for each pulse until the READY counter equals the Buffer counter. If the Buffer counter was not initialized before the Connect Request, then no READY pulses will be generated. If the Buffer counter is incremented after the Connection is made, then READY pulses will automatically be generated until the READY and Buffer counters are equal. The Buffer counter will be disabled when it equals Burst count -1, thereby putting a limit of 64K on the number of pending READY pulses.

If the Burst counter is not equal to the READY counter as a data Burst is received, then the Burst counter is incremented and the data is automatically transferred to the Destination Host. If the Burst counter is equal to the READY counter as a data Burst is received, then the data is not transferred to the Destination Host and an Overflow error is reported.

When the HIPPI connection is terminated, one of two operations may be performed by the Destination Host: the Destination FLOW control counters may be reset (and initialized), or the current buffer capacity may be automatically saved for the next HIPPI connection. To reset and initialize, the Destination Host must maintain a set of buffer counters, or empty the buffers before the next connection. To automatically save the current buffer capacity, the Destination device will initialize the READY counter to the Burst counter: at the end of a HIPPI connection, the number of remaining available buffers at the Destination Host is the difference between the Burst counter and the Buffer counter. Therefore, initializing the READY counter to the Burst counter contents will result in that same difference between the READY and Buffer counters. When a subsequent HIPPI connection is accepted, the Destination FLOW control circuit will automatically send the correct number (equal to the number of currently available buffers in the Destination Host) of READY pulses.

The Destination FLOW control signals are:

READY_IN (input) [RDYIN]

This input controls the Destination FLOW control circuit's Buffer and READY counters. A rising edge on this input will increment the Buffer counter and, if a Connect Request has been accepted, generate a READY pulse on the HIPPI channel as well as increment the READY counter by one. This input can be driven by a free-running 12.5 MHz clock for maximum throughput on the HIPPI channel (representing infinite Host buffer capacity), or it can be controlled by the Host memory system. If controlled by the Destination Host system, after initialization with one edge for each available buffer, the Host may generate one rising edge on this input after it processes and releases each used 256 word buffer.

NOT_RESET_READY (input) [NRRDY]

This signal is an active low TTL input that erases the stored count of available Host system buffers by resetting the Buffer, Ready and Burst counters to their initial states.

DESTINATION FIFO CONTROL

When a data Burst is received over the HIPPI channel, the Destination FIFO Control provides the signals necessary to transfer the received data from the Destination device to the Destination Host FIFO system. In addition to transferring received data Bursts, the Destination device will also transfer the HIPPI I-Field, and the channel and device status words as specified in the FIFO Control Signal Table. To provide flexibility at this interface, the Destination device identifies each type of information presented to the Destination Host, so that each implementation may customize its use of the information.

The Destination FIFO Control signals are:

WRITE_CLOCK (output) [WRCLK]

This signal is a buffered 25 MHz TTL clock synchronized to the internal local clock. It is intended for use with the VALID signal to transfer data to the write port of the FIFO and to serve as the timing reference for critical input and output control signals of the Host-side of the Destination device.

SELECT_0, 1, 2 (bi-directional) [SELBx]

These signals are used in conjunction with the MODE_SELECT inputs during manufacturing testing to confirm the function of the internal counters and state machines. In the functional mode [Mode value 5 (101)] the value of the SELECT (SELECT_2 is MSB) bus indicates the type of data available on the DOUT_0,31 signals. Select value 0 (000) indicates burst data on the outputs. Select value 1 (001) indicates I-Field data on the outputs. Select value 2 (010) indicates the LLRC word, and Select value 3 (011) indicates internal status data during inter-BURST wait states. When there is no connection on the HIPPI channel, the select value will sequence and repeat 5,6,7 (101, 110, 111) until connection is requested. Select value 4 is reserved to indicate sequence error status for advanced link diagnostics. For most applications these latter values can be ignored.

DATA_VALID (output) [DTVAL]

This signal is intended to be used together with the SELECT_0,1,2 outputs to gate the clocking of received data into the FIFO or register set selected by the select lines. All received data will be presented to the data outputs of the Destination device and will be accompanied by a DATA_VALID signal.

HIPPI DATA CONTROL

The data and control signals, received on the HIPPI channel, are resynchronized to the 25_MHz local clock, converted to TTL, and then presented to the data and control interface used by the host.

The HIPPI data control signals are:

BURST_OUT (output) [BROUT]

This signal indicates the state of the BURST line on the HIPPI channel. High indicates an active BURST and is presented with each word of the received burst. Low indicates an inactive BURST and is presented when there is no received data.

PACKET_OUT (output) [PKOUT]

This signal indicates the state of the PACKET line on the HIPPI channel. High indicates an active PACKET and is presented as long as PACKET is active on the HIPPI channel. Low indicates an inactive PACKET and is presented as long as PACKET is inactive on the HIPPI channel.

Note: The BURST_OUT and PACKET_OUT signals are provided to delimit the data into the FIFO the same way it is delimited on the HIPPI channel. These signals may not be needed by the Host.

FIFO Control Signal Table

SELB(2:0)	HOST data	DATA_VALID	Comment
000	HIPPI Burst	1 (high)	for duration of data received Burst
001	HIPPI I-Field	1 (high)	for duration of HIPPI Connect Request
010	HIPPI LLRC	1 (high)	one word, after last word of each Burst
011	gen. op. status	1 (high)	one word, beginning each Packet received on channel (accomp. start of PACKET_OUT)
		1 (high)	one word, end of each Burst, after LLRC*
		1 (high)	one word, end of each Packet (accompanies deactivation of PACKET_OUT)*
011	gen. op. status	0 (low)	multiple words, while connection is estab. across channel, but channel has no data
100	SEQUENCE ERROR	1 (high)	one word, when a HIPPI sequence error is detected, or when an illegal signal sequence disrupts the devices's state machines
101	idle/disab. status	1 (high)	one word, in sequence with FLOW status words (below), continuously while channel is disconnected
110	FLOW status word 1	1 (high)	one word, in sequence with FLOW status word 2 and idle/disab. status, continuously while channel is disconnected
111	FLOW status word 2	1 (high)	one word, in sequence with FLOW status word 1 and idle/disab. status, continuously while channel is disconnected

*Only one general operational status word (Select code 011) will be presented if the BURST and PACKET terminations coincide, i.e., BURST deasserted, followed by PACKET deasserted.

DATA AND PARITY

32_DATA_+_4_PARITY (outputs) [DTOxx, PAROx]

These signals reflect what was received on the data and parity lines of the HIPPI channel, resynchronized to local clock. During a connection request (CONNECT_REQUEST going high and remaining high) the I-field is presented on these signals. The LLRC is also presented to this interface after the last word of each burst.

Note: All parity errors are indicated but no recovery action is taken by the Destination device. If there is a parity error detected, then the data and bad parity are passed through the Destination device.

RX_PARITY_ERROR (output) [RPERR]

High indicates a detected parity error on a data word received over the HIPPI channel. This is valid for each word received; however, there may be a time skew between this indication and the presentation of data. See Figure 9 for details. The bad parity bit(s) is presented with its associated data word.

During a connection request the data lines contain the I-field. RX_PARITY_ERROR indication presented to the host logic when a connection has not been established tells the host that an I- field parity error has been detected. The RX_PARITY_ERROR signal is valid for every clock that I-field is presented. Bad parity on the I-field will result in the chip raising RX_PARITY_ERROR until one of the following things happen:

- The I-field changes (stabilizes) so that the parity is good
- The host logic accepts or rejects the connection request based on I-field content and the state of RX_PARITY_ERROR
- The HIPPI channel source drops REQUEST

RX_LLRC_ERROR (output) [RLLER]

This signal high means that an LLRC error was detected on a received burst. This signal is presented to the host along with the LLRC following the last word of the burst.

The Destination device counts the number of data words it receives from the HIPPI channel and uses this number as the “seed” for the LLRC it computes and checks against the received LLRC word.

SYNC_ERROR (output) [SYNER]

This signal high indicates the loss of synchronization with the HIPPI channel (overrun or underrun).

CHIP STATUS/CONTROL

MODE_SELECT_0, 1, and 2 (inputs) [MSELx]

There are several operating modes in which the Destination device can be placed. Operational and diagnostic modes are controlled by the data placed on the MODE_SELECT bus. MODE_SELECT_2 is the MSB and MODE_SELECT_0 is the LSB of this bus. Mode value 0 (000) is to be used as the master reset mode for all internal counters and state machines and should be used for power-up initialization. Mode value 4 (100) is the board test or diagnostic mode. In this mode an internal “walking zero” pattern generator will exercise all Host-side TTL outputs and the parity error circuitry. The SELECT_0, 1, 2 outputs will count through all eight states allowing exercise of any external I-Field or status registers driven by the Destination device. Mode value 5 (101) is the normal functional mode for the Destination device.

25_MHz (INPUT) [25MHZ]

This signal provides the Destination device with a 25MHz TTL clock (also called local clock) and is used to resynchronize the HIPPI channel clock and data.

50_MHz (INPUT) [50MHZ]

This signal provides the Destination device with a 50 MHz TTL clock and is used for internal state machine control, and for resynchronization. The phase requirements between this clock and 25_MHz are shown in Figure 9.

Absolute Maximum Ratings

ECL Supply Voltage V_{EE} (V_{CC} = 0)	–8.0VDC
ECL Input Voltage (V_{CC} = 0)	GND to VEE
ECL Output Source Current (continuous)	–50mA DC
TTL Supply Voltage V_{CC} (V_{EE} = 0)	7.0V
TTL Input Voltage (V_{EE} = 0)	5.5V
Operating Temperature	0°C to 70°C Ambient
Operating Junction Temperature T_J	+130°C
Storage Temperature	–65° to +150°C

ECL 10K Input/Output DC Characteristics VEE = –5.2V1

	$T_{ambient}$			
	0°C	25°C	75°C	UNIT
V_{OHmax}	–770	–730	–650	mV
V_{IHmax}	–720	–680	–600	mV
V_{OHmin}	–1000	–980	–920	mV
V_{IHmin}	–1145	–1105	–1045	mV
V_{ILmax}	–1490	–1475	–1450	mV
V_{OLmax}	–1625	–1620	–1585	mV
V_{OLmin}	–1980	–1980	–1980	mV
V_{ILmin}	–2000	–2000	–2000	mV
I_{inHmax}	–0	30	30	µA
I_{inLmax}	–.5	–.5	–.5	µA

Recommended Operating Conditions

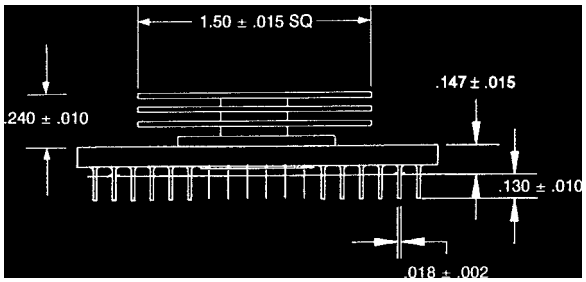
PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE})	–4.94	–5.2	–5.46	V
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Ambient Temperature	0		70	°C
Junction Temperature			<130	°C
S2020 — I_{CC} — I_{EE} — P_{OEF}		65 421 1530	91 589	mA mA mW
S2021 — I_{CC} — I_{EE} — P_{OEF}		125 307 90	174 429	mA mA mW

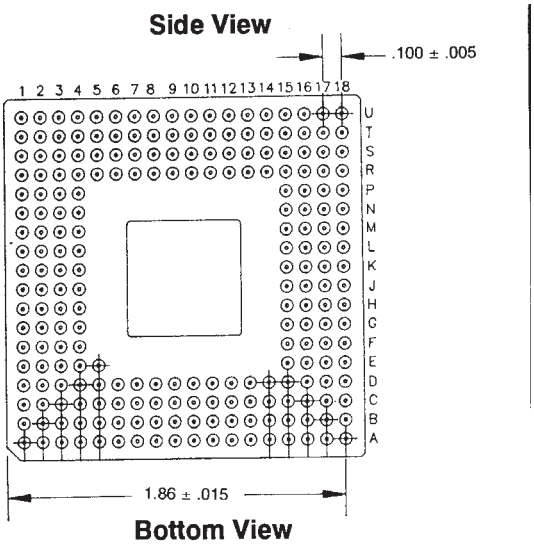
TTL Input/Output DC Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL 0°/+70°C MIN	TYP[2]	MAX	UNIT
V_{IH}[3]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[3]	Input LOW voltage	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = –18mA			–.8	–1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –1mA		2.7	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = Min	I_{OL} = 8mA			0.5	V
			I_{OI} = 20mA			0.5	V
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V				110	µA
I_I	Input HIGH current at Max.	V_{CC} = Max, V_{IN} = 5.25V				1	mA
I_{IL}	Input LOW current	V_{CC} = Max, V_{IN} = 0.5V				110	µA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{IN} = 0.5V		–25		–100	mA

1. Data measured with V_{EE} = –5.2 ± .1V assuming a +50°C rise between ambient (t_a) and junction temperature (T_J) for 0°C, +25°C, and +70°C. Specification will vary based upon T_J. These conditions will be met with an ambient 70°C airflow of 200 LFM.
2. Typical limits are at 25°C, VCC = 5.0V.
3. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

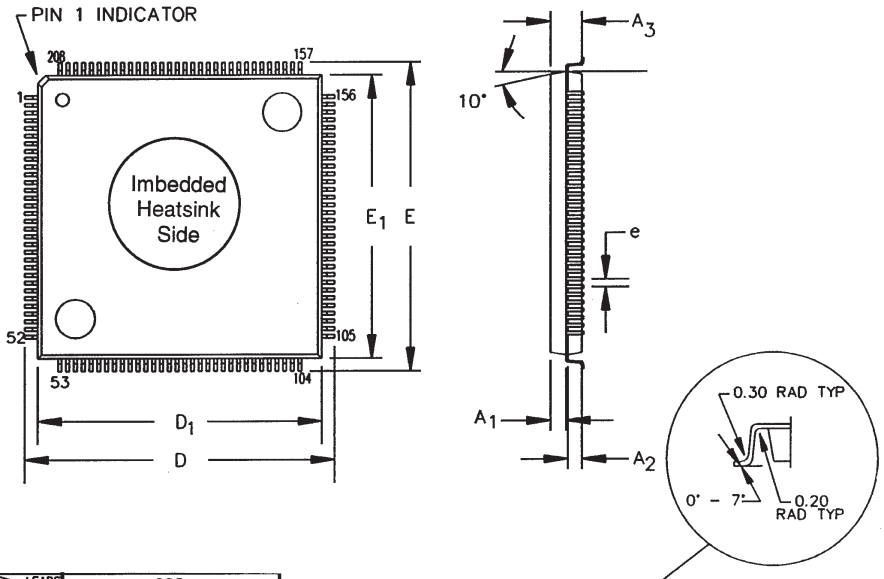
225 PGA





All dimensions nominal in inches

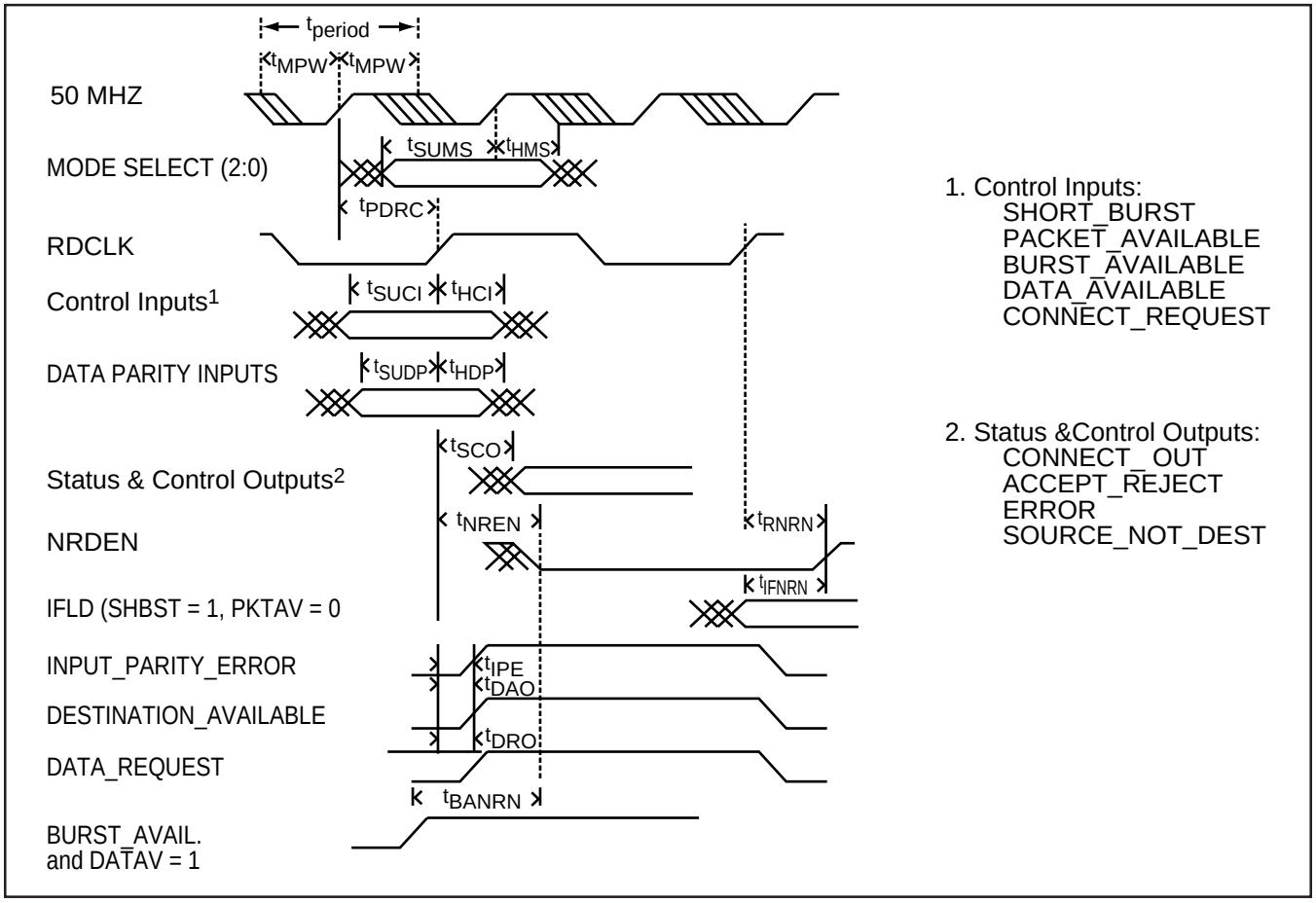
208 Thermally Enhanced Plastic (TEP)



DIM LTR	LEADS TOL	208
e	BASIC	.50
B	BASIC	.25
A	MAX	4.07
A_1	±.10	1.67
A_2	±.10	1.67
A_3	±.25	3.49
D	±.25	31.20
D_1	±.10	28.00
E	±.25	31.20
E_1	±.10	28.00
L	±.15	.80

All dimensions nominal in mm.

Figure 8. S2020 Source Device Timing

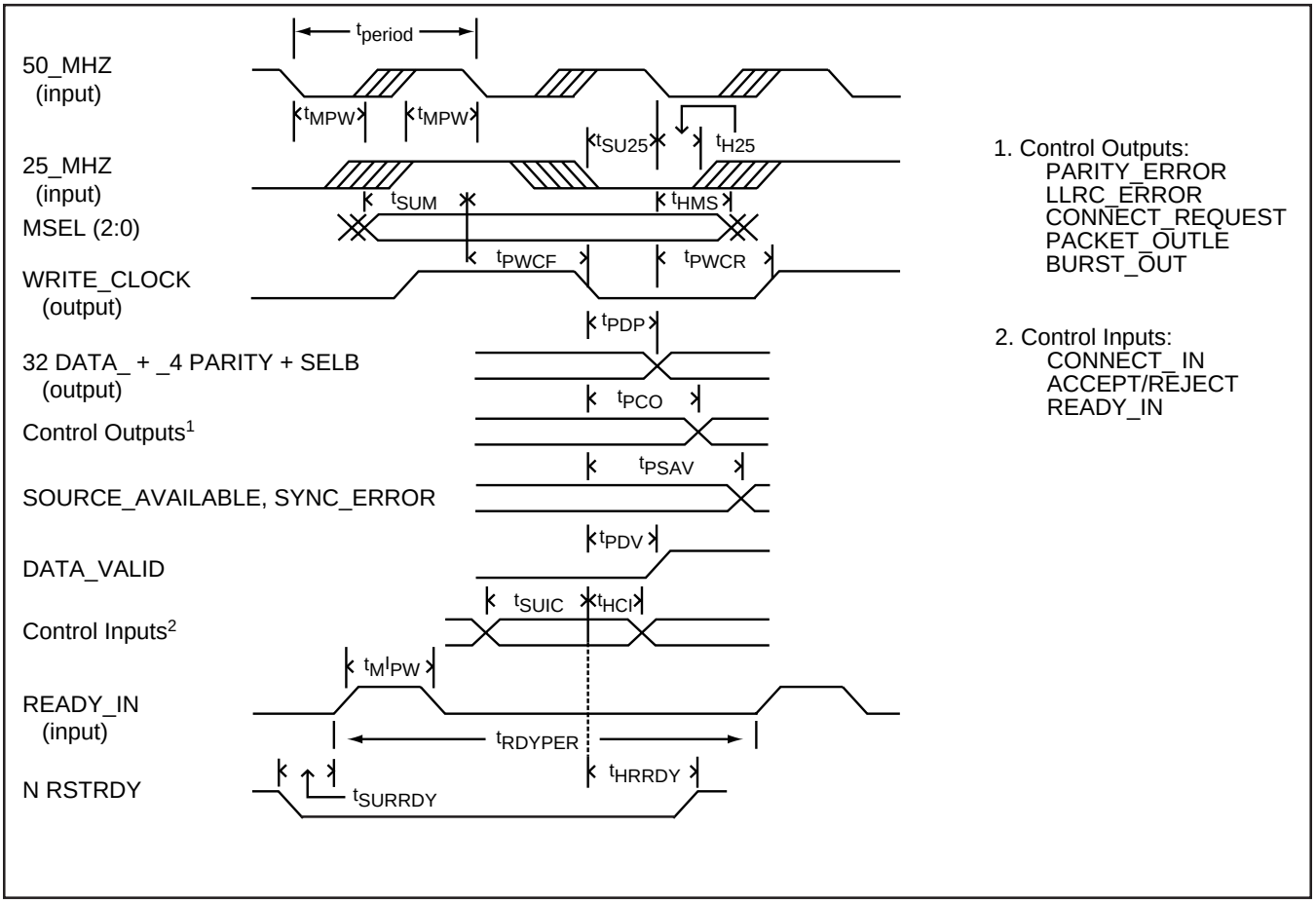


S2020 Source Timing Table

	Min nsec	Typ nsec	Max nsec	Notes
t_{PERIOD} [3]	—	20	—	
t_{MPW} [3]	5.55	—	—	
t_{SUMS}	7	—	—	Relative to 50MHz INPUT
t_{HMS}	0	—	—	
t_{PDRC}	5	11	17	For Reference Only
t_{SUCI}	21	—	—	Relative to RDCLK Rising Edge
t_{HCI}	0	—	—	
t_{SUDP}	14	—	—	
t_{HDP}	0	—	—	
t_{SCO}	—	—	17	
t_{NREN} [4]	—	—	14	
t_{IPE} [4]	—	—	10	
t_{DAO} [4]	—	—	17	
t_{DRO} [4]	—	—	10	
t_{IFNRN} [4]	—	—	19	
t_{RNRN} [4]	—	—	19	
t_{BANRN} [4]	—	—	17	

3. Guaranteed but not tested

Figure 9. S2021 Destination Device Timing



S2021 Destination Timing Table

	Min nsec	Typ nsec	Max nsec	Notes
t_{PERIOD}[3]	—	20	—	
t_{MPW}[3]	5.55	—	—	
t_{PWCF}[4]	5	—	14	Relative to 50MHz Falling Edge
t_{PWCR}[4]	5	—	15	
t_{SU25}	2	—	—	
t_{H25}	2.5	—	—	
t_{PDP}[4]	—	—	13	Relative to WRCLK Falling Edge
t_{PCO}[4]	—	—	13	
t_{PSAV}[4]	—	—	18	
t_{PDV}[4]	—	—	16	
t_{SUCI}	9	—	—	
t_{HCI}	0	—	—	
t_{RDYPER}[3]	40	—	—	
t_{SURRDY}[3]	8	—	—	Relative to WRCLK falling edge or RDYIN rising edge
t_{HRRDY}[3]	8	—	—	
t_{SUM}	5	—	—	
t_{HMS}	5	—	—	

3. Guaranteed but not tested
4. Assumes 5pf load for ECL and 15pf for TTL

SOURCE

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
NC	ND27	D28	D29	ND31	NP0	P1	P2	P3	TPWR	TGND	PAR02	DAT31	DAT28	DAT25	DAT22	DAT19	NC	U
D26	NC	ND28	ND29	D30	EGND	P0	NP2	NP3	TSTO*	PAR03	PAR00	DAT30	DAT27	DAT24	DAT21	NC	DAT18	T
ND25	D25	NC	D27	EGND	ND30	D31	NP1	–5.2V	–5.2V	PAR01	DAT29	DAT26	DAT23	DAT20	NC	DAT16	DAT15	S
ND24	D24	ND26	+5V	+5V	GND	GND	GND	–5.2V	–5.2V	GND	GND	GND	+5V	+5V	DAT17	DAT13	DAT12	R
D22	ND23	EGND	+5V											+5V	DAT14	DAT10	DAT09	P
ND21	D21	D23	GND											GND	DAT11	DTREQ	NRDEN	N
EGND	D20	ND22	GND					BOTTOM VIEW						GND	DATO0	RDCLK	DSTAV	M
ND19	D19	ND20	GND											GND	INPRR	CNOUT	ACREJ	L
ND18	D18	–5.2V	–5.2V											–5.2V	–5.2V	SDIC	SRNDS	K
D17	ND17	–5.2V	–5.2V											–5.2V	–5.2V	TGND	SQERR	J
D16	ND16	ND15	GND											GND	DAT04	DAT06	DAT07	H
D15	D14	D13	GND											GND	DAT00	DAT03	DAT05	G
ND14	GTRO*	ND12	GND											GND	SHBST	DAT01	DAT02	F
ND13	D12	EGND	+5V	NC										+5V	MSEL2	BSTAV	PKTAV	E
D11	ND11	D09	+5V	+5V	GND	GND	GND	–5.2V	-5.2V	GND	GND	GND	+5V	+5V	EGND	CNREQ	DATAV	D
D10	ND10	NC	ND08	EGND	D05	ND04	ND02	–5.2V	–5.2V	NPKT	THDI*	VBB	RDY	CON	NC	MSEL0	MSEL1	C
ND09	NC	D07	D06	ND05	D03	D02	D01	D00	NCLK	REQ	PKT	BRST	EGND	EGND	EGND	NC	50MHZ	B
NC	D08	ND07	ND06	D04	ND03	EGND	ND01	ND00	CLK	NREQ	EGND	NBRST	THDO*	DSIC	NRDY	NCON	NC	A

*Indicates signal used for component testing—make no connection

HIPPI INTERCONNECT PAIR

DSIC = Destination to Source Interconnect
SDIC = Source to Destination Interconnect

EGND = TGND = GND = 0V

TPWR = +5V

DESTINATION

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
NC	CON	NREQ	BRST	CLK	NP3	P2	P1	P0	ACCRJ	D31	D30	ND28	D27	ND25	ND24	D23	NC	U
NRDY	NC	THDI*	NBRST	PKT	CONIN	P3	NP1	NP0	ND31	ND30	D29	D28	ND26	D25	D24	NC	NRRDY	T
TGND	THDO*	NC	NCON	REQ	NPKT	NCLK	NP2	–5.2V	–5.2V	ND29	ND27	D26	RDYIN	ND23	NC	D22	ND21	S
SELB1	SELB0	RDY	+5V	+5V	GND	GND	GND	–5.2V	–5.2V	GND	GND	GND	+5V	+5V	ND22	ND20	D20	R
25MHZ	50MHZ	TPWR	+5V											+5V	D21	D19	ND18	P
DTO00	DSIC	SELB2	GND											GND	ND19	MSEL2	ND17	N
DTO03	DTO01	DTVAL	GND					BOTTOM VIEW						GND	D18	D17	D16	M
DTO05	DTO04	DTO02	GND											GND	ND16	ND15	D15	L
DTO07	DTO06	–5.2V	–5.2V											–5.2V	–5.2V	ND14	D14	K
DTO08	DTO09	–5.2V	–5.2V											–5.2V	–5.2V	ND13	MSEL1	J
TPWR	TGND	DTO11	GND											GND	ND11	ND12	D13	H
DTO10	DTO12	DTO15	GND											GND	ND09	D11	D12	G
DTO13	DTO14	DTO18	GND											GND	D08	D10	ND10	F
DTO16	DTO17	DTO21	+5V	NC										+5V	MSEL0	ND08	D09	E
DTO19	DTO20	DTO22	+5V	+5V	GND	GND	GND	–5.2V	–5.2V	GND	GND	GND	+5V	+5V	ND05	D07	ND07	D
TPWR	TGND	NC	DTO25	DTO28	TGND	PARO0	RPERR	–5.2V	–5.2V	SSO1*	D00	ND01	SDIC	D04	NC	D06	ND06	C
DTO23	NC	DTO26	DTO29	DTO30	PARO1	PARO3	SRCAV	CONRQ	PKOUT	TGND	SSO2*	VBB	D01	ND02	ND03	NC	D05	B
NC	DTO24	DTO27	TPWR	DTO31	PARO2	SYNER	BROUT	WRCLK	RLLER	TPWR	SSO0*	SSEN*	ND00	D02	D03	ND04	NC	A

*Indicates signal used for component testing only

— Connect SSEN to GROUND (0V)

— Make no connection to other pins mark with asterisk (*)

HIPPI INTERCONNECT PAIR

DSIC = Destination to Source Interconnect
SDIC = Source to Destination Interconnect

EGND = TGND = GND = 0V

TPWR = +5V

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	GND	53	GND	105	GND	157	GND
2	GND	54	+5V	106	GND	158	+5V
3	DAT18	55	NCON	107	ND09	159	ND27
4	DAT17	56	CON	108	D09	160	D27
5	DAT16	57	EGND	109	ND10	161	ND28
6	DAT15	58	NRDY	110	D10	162	D28
7	DAT14	59	RDY	111	EGND	163	EGND
8	DAT13	60	EGND	112	ND11	164	ND29
9	DAT12	61	DSIC	113	D11	165	D29
10	DAT11	62	VBB	114	ND12	166	ND30
11	DAT10	63	EGND	115	D12	167	D30
12	DAT09	64	–5.2V	116	ND13	168	ND31
13	DAT08	65	–5.2V	117	D13	169	D31
14	–5.2V	66	GND	118	–5.2V	170	–5.2V
15	–5.2V	67	GND	119	–5.2V	171	–5.2V
16	GND	68	BRST	120	GND	172	GND
17	GND	69	NBRST	121	GND	173	GND
18	DTREQ	70	PKT	122	ND14	174	NP0
19	NRDEN	71	NPKT	123	D14	175	P0
20	RDCLK	72	EGND	124	ND15	176	NP1
21	INPRR	73	REQ	125	D15	177	P1
22	DSTAV	74	NREQ	126	ND16	178	NP2
23	CNOUT	75	NCLK	127	D16	179	P2
24	ACREJ	76	CLK	128	ND17	180	NP3
25	SDIC	77	GND	129	D17	181	P3
26	SRNDS	78	GND	130	GND	182	GND
27	GND	79	+5V	131	GND	183	GND
28	GND	80	ND00	132	+5V	184	+5V
29	+5V	81	D00	133	ND18	185	TST0
30	SQERR	82	ND01	134	D18	186	TGND
31	DAT07	83	D01	135	ND19	187	PAR03
32	DAT06	84	GND	136	D19	188	PAR02
33	DAT05	85	ND02	137	EGND	189	PAR01
34	DAT04	86	D02	138	ND20	190	PAR00
35	DAT03	87	ND03	139	D20	191	DAT31
36	DAT02	88	D03	140	ND21	192	DAT30
37	DAT01	89	GND	141	D21	193	GND
38	–5.2V	90	GND	142	–5.2V	194	GND
39	–5.2V	91	–5.2V	143	–5.2V	195	–5.2V
40	GND	92	–5.2V	144	GND	196	–5.2V
41	GND	93	ND04	145	GND	197	DAT29
42	DAT00	94	D04	146	ND22	198	DAT28
43	PKTAV	95	ND05	147	D22	199	DAT27
44	BSTAV	96	D05	148	ND23	200	DAT26
45	SHBST	97	ND06	149	D23	201	DAT25
46	DATAV	98	D06	150	ND24	202	DAT24
47	CNREQ	99	EGND	151	D24	203	DAT23
48	MSEL2	100	ND07	152	ND25	204	DAT22
49	MSEL1	101	D07	153	D25	205	DAT21
50	MSEL0	102	ND08	154	ND26	206	DAT20
51	50MHZ	103	D08	155	D26	207	DAT19
52	GND	104	+5V	156	GND	208	+5V

EGND = TGND = GND = 0V;
TPWR = +5V

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	NRRDY	53	GND	105	GND	157	NCON
2	ND22	54	+5V	106	DTO23	158	NREQ
3	D22	55	ND04	107	DTO22	159	REQ
4	ND21	56	D04	108	DTO21	160	NBRST
5	D21	57	ND03	109	DTO20	161	BRST
6	ND20	58	D03	110	DTO19	162	NPKT
7	D20	59	SDIC	111	DTO18	163	PKT
8	ND19	60	ND02	112	DTO17	164	CLK
9	D19	61	D02	113	DTO16	165	NCLK
10	ND18	62	ND01	114	DTO15	166	–5.2V
11	D18	63	D01	115	–5.2V	167	–5.2V
12	–5.2V	64	ND00	116	–5.2V	168	GND
13	–5.2V	65	D00	117	GND	169	GND
14	GND	66	–5.2V	118	GND	170	CONIN
15	GND	67	–5.2V	119	DTO14	171	NP3
16	MSEL2	68	GND	120	DTO13	172	P3
17	ND17	69	GND	121	DTO12	173	NP2
18	D17	70	VBB	122	DTO11	174	P2
19	ND16	71	SSEN	123	DTO10	175	NP1
20	D16	72	SSO2	124	TGND	176	P1
21	ND15	73	SSO1	125	DTO09	177	NP0
22	D15	74	SSO0	126	DTO08	178	P0
23	ND14	75	PKOUT	127	GND	179	GND
24	D14	76	RLLER	128	GND	180	GND
25	GND	77	GND	129	+5V	181	+5V
26	GND	78	GND	130	DTO07	182	ACCRJ
27	+5V	79	+5V	131	DTO06	183	ND31
28	MSEL1	80	WRCLK	132	DTO05	184	D31
29	ND13	81	CONRQ	133	DTO04	185	ND30
30	D13	82	BROUT	134	DTO03	186	D30
31	ND12	83	SRCAV	135	DTO02	187	ND29
32	D12	84	SYNER	136	DTO01	188	D29
33	ND11	85	RPERR	137	DTO00	189	ND28
34	D11	86	PARO3	138	DSIC	190	D28
35	ND10	87	PARO2	139	–5.2V	191	GND
36	D10	88	PARO1	140	–5.2V	192	GND
37	–5.2V	89	GND	141	GND	193	–5.2V
38	–5.2V	90	GND	142	GND	194	–5.2V
39	GND	91	–5.2V	143	DTVAL	195	ND27
40	GND	92	–5.2V	144	25MHZ	196	D27
41	ND09	93	PARO0	145	50MHZ	197	ND26
42	D09	94	DTO31	146	SELB2	198	D26
43	ND08	95	DTO30	147	SELB1	199	ND25
44	D08	96	TGND	148	SELB0	200	D25
45	ND07	97	DTO29	149	TPWR	201	RDYIN
46	D07	98	DTO28	150	TGND	202	ND24
47	MSEL0	99	DTO27	151	RDY	203	D24
48	ND06	100	DTO26	152	NRDY	204	ND23
49	D06	101	DTO25	153	GND	205	D23
50	ND05	102	DTO24	154	GND	206	+5V
51	D05	103	+5V	155	+5V	207	GND
52	GND	104	GND	156	CON	208	GND

EGND = TGND = GND = 0V;
TPWR = +5V

Figure 10. Interconnect (output) Network

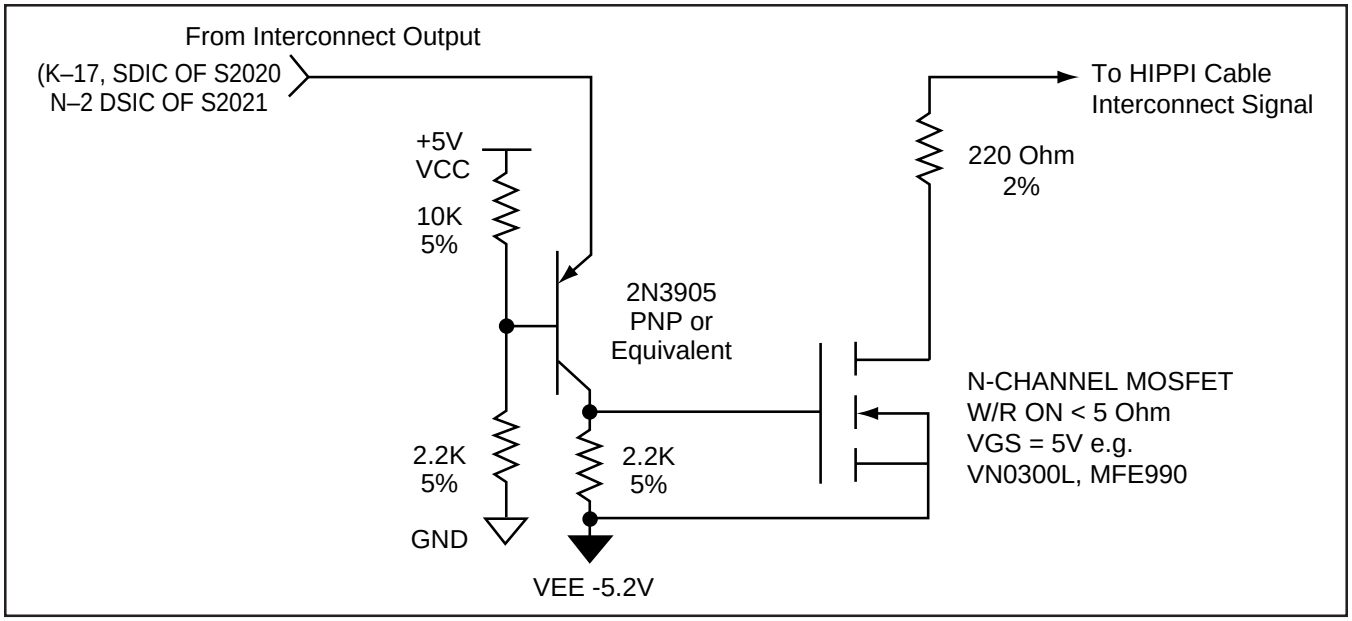
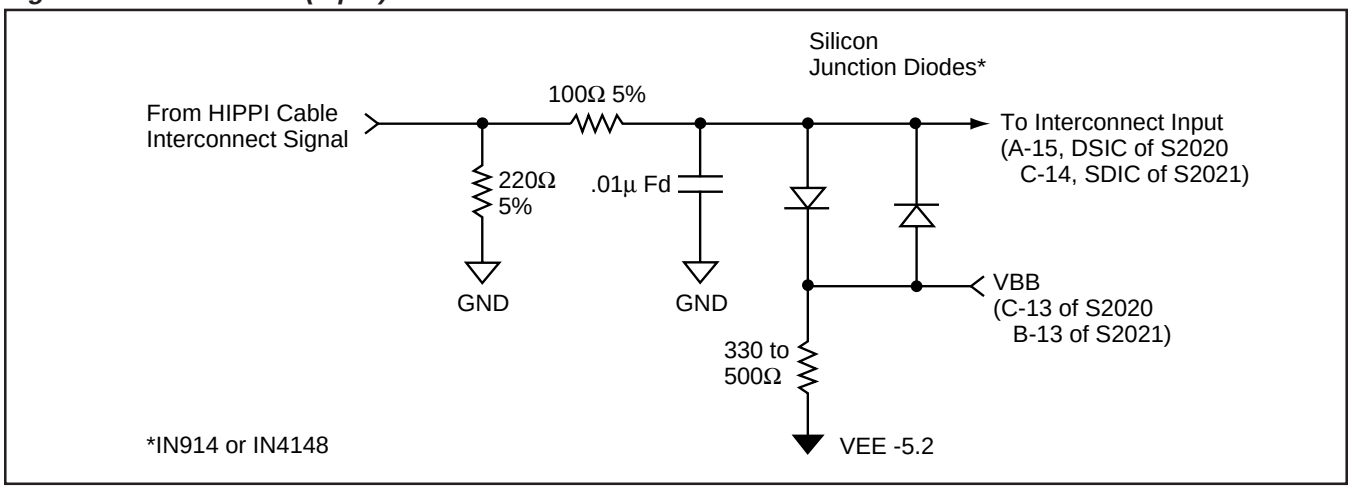


Figure 11. Interconnect (input) Network



ORDERING INFORMATION		
GRADE	FUNCTION	PACKAGE
S-Commercial	2020 — Hippi Source 2021 — Hippi Destination 2022 — Hippi Evaluation Kit (contains 2 source and 2 destination parts)	A = 225 PGA B = 208 TEP

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