P-Channel 1.25-W, 1.8-V (G-S) MOSFET

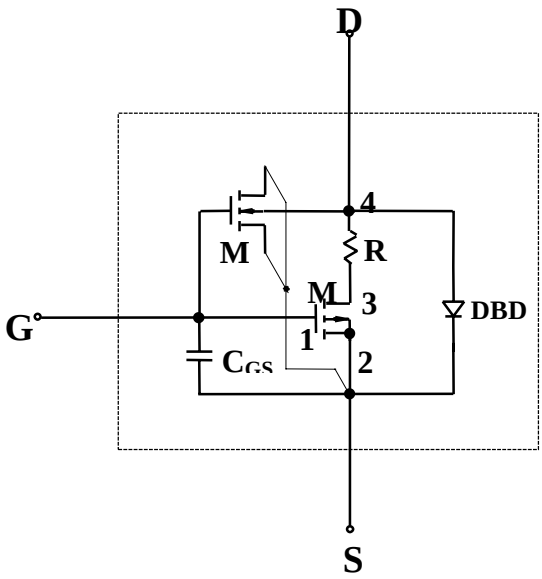
Characteristics

- P-channel Vertical DMOS
- Macro-Model (Subcircuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to –4.5 volt gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measured electrical data and are not intended as an exact physical description of a device.

Model Subcircuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

Model Evaluation

P-Channel Device (T_J=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typ	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250µA	**0.79**	V
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ **-5**V, V_{GS} = **-4.5**V	**55.7**	A
		V_{DS} ≤ **-5**V, V_{GS} = **-2.5**V	**15.1**	
Drain-Source On-Resistance[b]	$r_{DS(on)}$	V_{GS} = **-4.5**V, I_D = **-3.5**A	**0.042**	Ω
		V_{GS} = **-2.5**V, I_D = **-3.0**A	**0.065**	
		V_{GS} = **-1.8**V, I_D = **-2.0**A	**0.103**	
Forward Transconductance[b]	g_{fs}	V_{DS} = **-5**V, I_D = **-3.5**A	**9.2**	S
Diode Forward Voltage[b]	V_{SD}	I_S = **-1.6**A, V_{GS} = 0V	**0.80**	V
Dynamic[a]				
Total Gate Charge	Q_g	V_{DS} = **-6**V, V_{GS} = **-4.5**V, I_D = **-3.5**A	**8.7**	nC
Gate-Source Charge	Q_{gs}		**1.9**	
Gate-Drain Charge	Q_{gd}		**1.5**	
Input Capacitance	C_{iss}	V_{DS} = **-6**V, V_{GS} = 0V, f = 1 MHz	**1228**	pF
Output Capacitance	C_{oss}		**250**	
Reverse Transfer Capacitance	C_{rss}		**116**	
Switching[c]				
Turn-On Time	$t_{d(on)}$	V_{DD} = **-6**V, R_L = **6**Ω, I_D ≅ **-1**A, V_{GEN} = **-4.5**V, R_G = 6Ω	**25**	ns
	t_r		**12**	
Turn-Off Time	$t_{d(off)}$		**61**	
	t_f		**9.8**	

Notes:
a) For design aid only, not subject to production testing
b) Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%
c) Switching time is essentially independent of operating temperature

Comparison of Model with Measured Data
(T_J=25°C Unless Otherwise Noted)