16M SDR Synchronous Graphics RAM
185 / 167 / 143 / 125 MHz

Features

- Single 3.3 V ± 0.3 power supply
- 185 / 167 / 143 / 125 MHz maximum clock frequency
- Dual bank operation
- Programmable burst type, burst length and $\overline{CAS}$ latency
  - Burst type: Sequential & Interleave
  - Burst length: 1, 2, 4, 8 & full page
  - $\overline{CAS}$ latency: 2 & 3
- 8-column Block Write and Write-Per-Bit Modes
- LVTTL inputs and outputs
- Byte control by DQM0 ~ DQM3
- Auto Precharge and Auto Refresh Modes
- 2K Refresh cycles / 32ms
- Self Refresh
- 100-pin LQFP (0.65mm lead pitch)

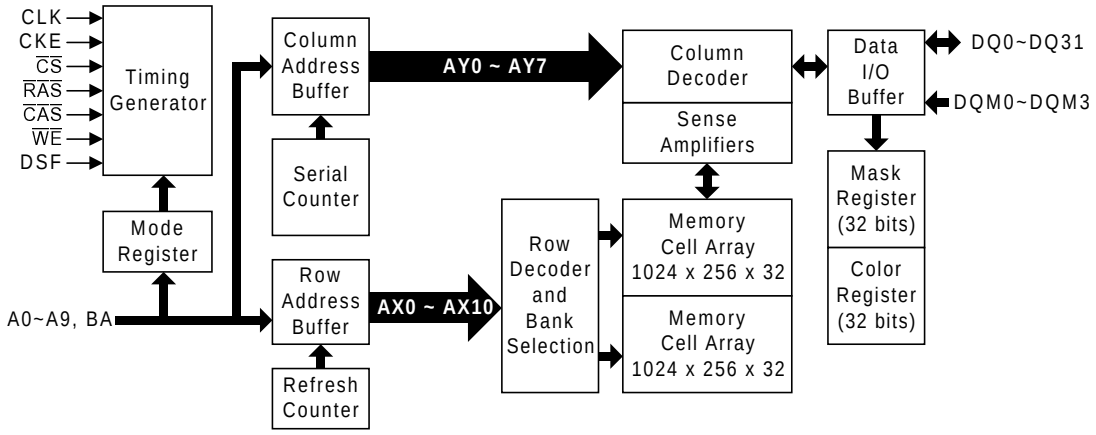
Description

The SM84L512K32B is a high-speed single-data-rate Synchronous Graphics DRAM organized in a 262,144-word by 32-bit by 2-bank configuration. Commands and data are synchronized to the rising edge of the system clock to enable precise control and predictability. A programmable mode register enables the device to be customized for maximum system performance with burst type, burst length and $\overline{CAS}$ latency. This product is ideal for high bandwidth applications.

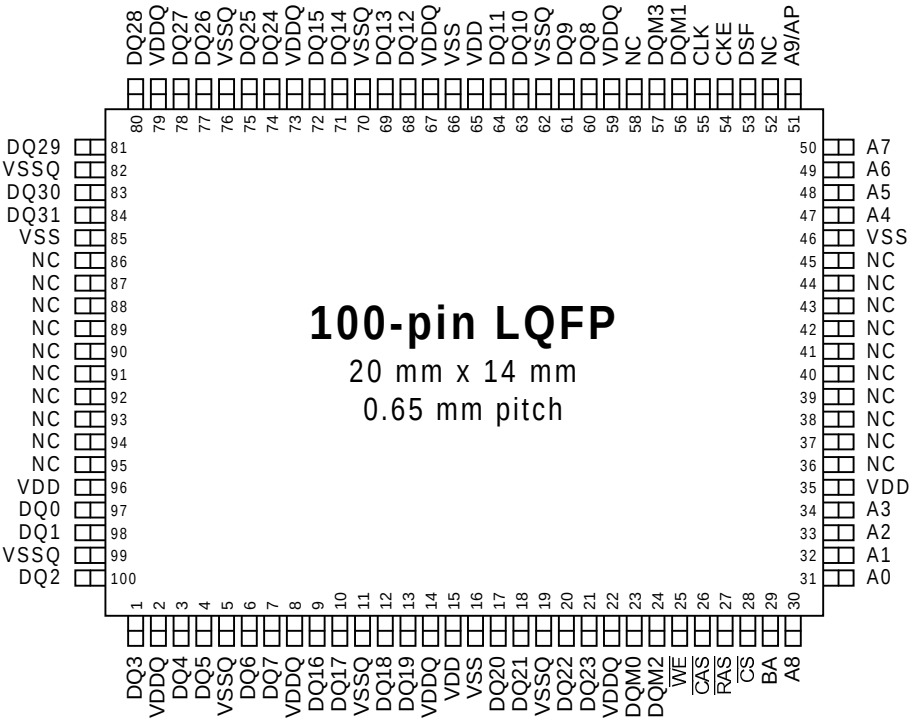
Key Timing Parameters

	-5.4	-6	-7	-8
Clock Frequency (MHz)	185	167	143	125
Access Time, t_{AC} (ns) CL=3	4.4	5.0	5.5	7
Input Setup Time, t_{IS} (ns)	1.5	1.5	1.5	2.0
Input Hold Time, t_{IH} (ns)	1.5	1.5	1.5	1.5

Functional Block Diagram



Pin Assignment (Top View)



Pin Descriptions

Pin Name	Description
CLK	System Clock input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A9	Address
BA	Bank Select
DQ0 ~ DQ31	Data Input / Output
DQM0 ~ DQM3	Data Input / Output Mask
DSF	Special Function Enable
V_{DD} / V_{SS}	Power Supply / Ground
V_{DDQ} / V_{SSQ}	DQ Power / Ground
NC	No Connection

Ordering Information

Order Number	Pkg	Speed
SM84L512K32BL-5R4	100LQFP	185 MHz
SM84L512K32BL-6	100LQFP	167 MHz
SM84L512K32BL-7	100LQFP	143 MHz
SM84L512K32BL-8	100LQFP	125 MHz

Electrical Characteristics

*Absolute Maximum Ratings **

Storage Temperature .....-50 °C to 125 °C
Voltage Relative to Vss .....-1.0 V to +4.6 V
Data Output Current .....50 mA
Power Dissipation.....1 W

* Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

DC Operating Conditions

(T_A = 0 °C to 70 °C)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Power Supply	V_{DD}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3	0	0.8	V	
Output High Voltage	V_{OH}	2.4	-	-	V	I_{OUT} = -2ma
Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OUT} = 2ma
Input Leakage Current	I_{LI}	-5	-	5	µA	0V ≤ V_{IN} ≤ V_{DD} + 0.3V All other pins not under test = 0 V
Output Leakage Current	I_{LO}	-5	-	5	µA	0V ≤ V_{OUT} ≤ V_{DD} Output Disabled

*Capacitance ***

(T_A = 25 °C, V_{DD} = 3.3V, f = 1 MHz)

Parameter	Symbol	Maximum	Unit
Input Capacitance	C_{IN}	4	pF
Input/Output Capacitance	C_{IO}	5	pF

** Note: Capacitance is sampled and not 100% tested.

DC Characteristics

(V_{DD} = 3.3V ± 0.3V, T_A = 0°C to 70°C)

Parameter	Symbol	Condition	Maximum -5R4	Maximum -6	Maximum -7	Maximum -8	Unit	Note
Operating Current	I_{CC1}	$t_{RC} \geq t_{RC(min.)}$, $t_{CK} \geq t_{CK\ (min.)}$ I_{LO} = 0 mA, burst length=1	240	230	210	180	mA	1
Precharge Standby Current (Non power-down mode)	I_{CC2N}	$\overline{CS} \geq V_{IH(min.)}$, CKE $\geq V_{IH(min.)}$, $t_{CK} = t_{CK\ (min.)}$	60				mA	1
	I_{CC2NS}	$\overline{CS} \geq V_{IH\ (min.)}$, CKE $\geq V_{IH\ (min.)}$, CLK $\leq V_{IL\ (max.)}$ Input signals stable.	25					
Precharge Standby Current (Power-down mode)	I_{CC2P}	$\overline{CS} \geq V_{IH\ (min.)}$, CKE $\leq V_{IL\ (max.)}$, $t_{CK} = t_{CK\ (min.)}$	5				mA	1
	I_{CC2PS}	$\overline{CS} \geq V_{IH\ (min.)}$, CKE $\leq V_{IL\ (max.)}$, CLK $\leq V_{IL\ (max.)}$	5					
Active Standby Current (Non power-down mode)	I_{CC3N}	$\overline{CS} \geq V_{IH\ (min.)}$, CKE $\geq V_{IH\ (min.)}$, $t_{CK} = t_{CK\ (min.)}$	65				mA	1
	I_{CC3NS}	$\overline{CS} \geq V_{IH\ (min.)}$, CKE $\geq V_{IH\ (min.)}$, CLK $\leq V_{IL\ (max.)}$ Input signals stable.	40					
Active Standby Current (Power-down mode)	I_{CC3P}	$\overline{CS} \geq V_{IH\ (min.)}$, CKE $\leq V_{IL\ (max.)}$, $t_{CK} = t_{CK\ (min.)}$	40				mA	1
	I_{CC3PS}	$\overline{CS} \geq V_{IH\ (min.)}$, CKE $\leq V_{IL\ (max.)}$, CLK $\leq V_{IL\ (max.)}$	40					
Operating Current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (min.)}$, $\overline{CAS}$ latency = 3	335	320	290	260	mA	1
		I_{LO} = 0mA, $\overline{CAS}$ latency = 2	275	260	230	210		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC\ (min.)}$	225	215	195	165	mA	2
Self Refresh Current	I_{CC6}	CKE $\leq$ 0.2V	6				mA	
Operating Current (Block write mode)	I_{CC7}	$t_{CK} \geq t_{CK\ (min.)}$, I_{LO} = 0mA	280	270	250	220	mA	

Note:

1. These parameters depend on output loading and cycle rate. Measurements obtained with outputs open.
   Input signals are changed once during $t_{CK\ (min.)}$.
2. Input signals are changed once during $t_{CK\ (min.)}$.

AC Characteristics

(V_{DD} = 3.3V ± 0.3V, T_A = 0°C to 70°C)

Parameter		Symbol	-5R4 (185 MHz)		-6 (167 MHz)		-7 (143 MHz)		-8 (125 MHz)		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Clock cycle time	CL = 3	t_{CK}	5.4		6		7		8		ns
	CL = 2		7.4		8		10		12		
Access time from CLK	CL = 3	t_{AC}		4.4		5		5.5		7	ns
	CL = 2			5.4		6		7		10	
CLK to output in Hi-Z	CL = 3	t_{HZ}		4.4		5		5.5		7	ns
	CL = 2			5.4		6		7		10	
CLK to output in Low-Z		t_{LZ}	1		1		1		1		ns
CLK high pulse width		t_{CH}	2.2		2.5		2.5		3		ns
CLK low pulse width		t_{CL}	2.2		2.5		2.5		3		ns
Output data hold time		t_{OH}	2.2		2.5		2.5		3		ns
Input setup time		t_{IS}	1.5		1.5		1.5		2.0		ns
Input hold time		t_{IH}	1.5		1.5		1.5		1.5		ns
Row cycle time		t_{RC}	48.6		54		63		80		ns
Row active time		t_{RAS}	32.4	100K	36	100K	42	100K	48	100K	ns
Row precharge time		t_{RP}	16.2		18		21		24		ns
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}	16.2		18		21		24		ns
Row active to row active delay		t_{RRD}	10.8		12		14		16		ns
Last data-in to row precharge		t_{RDL}	1		1		1		1		CLK
Last data-in to new column address delay		t_{CDL}	1		1		1		1		CLK
Last data-in to burst stop		t_{BDL}	1		1		1		1		CLK
Block write cycle time		t_{BWC}	1		1		1		1		CLK
Block write data-in to precharge command		t_{BPL}	1		1		1		1		CLK
Refresh time		t_{REF}		32		32		32		32	ms

AC Test Conditions

(V_{DD} = 3.3V ± 10%, T_A = 0°C to 70°C)

Parameter	Condition
Input signal level	V_{IH} / V_{IL} = 2.4V / 0.4V
Input timing reference level	1.4 V
Input transition time (rise/fall)	1.0 ns
Output timing reference level	1.4 V
Output load condition	See Figure B.

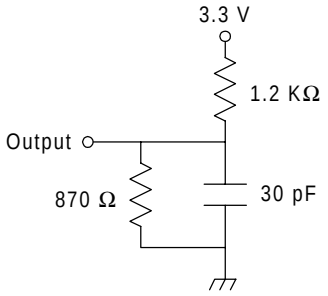


Figure A. DC output load.

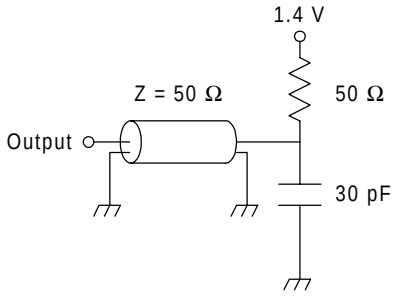


Figure B. AC output load.

Command Truth Table

Command		CKEn-1	CKEn	DQM	BA	A9	A0-8	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Note
Mode register set		H	X	X	Opcode			L	L	L	L	L	1
Special mode register set		H	X	X	Opcode			L	L	L	L	H	1, 2, 3
Bank active with write-per-bit disabled		H	X	X	V	V	V	L	L	H	H	L	4, 6
Bank active with write-per-bit enabled		H	X	X	V	V	V	L	L	H	H	H	4, 6
Read		H	X	X	V	L	V	L	H	L	H	L	4
Read with auto precharge		H	X	X	V	H	V	L	H	L	H	L	4, 5
Write		H	X	X	V	L	V	L	H	L	L	L	4, 6
Write with auto precharge		H	X	X	V	H	V	L	H	L	L	L	4, 5, 6
Masked block write		H	X	X	V	L	V	L	H	L	L	H	4, 6
Masked block write with auto precharge		H	X	X	V	H	V	L	H	L	L	H	4, 5, 6
Precharge selected bank		H	X	X	V	L	X	L	L	H	L	L	
Precharge both banks		H	X	X	X	H	X	L	L	H	L	L	
Auto refresh		H	H	X	X	X	X	L	L	L	H	L	1
Self refresh	Entry	H	L	X	X	X	X	L	L	L	H	L	1
	Exit	L	H	X	X	X	X	H	X	X	X	X	1
		L	H	X	X	X	X	L	H	H	H	X	1
Burst stop		H	X	X	X	X	X	L	H	H	L	L	3
Clock suspend mode	Entry	H	L	X	X	X	X	L	H	H	H	X	
or		H	L	X	X	X	X	H	X	X	X	X	
Active power down	Exit	L	H	X	X	X	X	X	X	X	X	X	
Precharge	Entry	H	L	X	X	X	X	L	H	H	H	X	7
Power down mode		H	L	X	X	X	X	H	X	X	X	X	7
	Exit	L	H	X	X	X	X	L	V	V	V	V	
		L	H	X	X	X	X	H	X	X	X	X	
Data write		H	X	L	X	X	X	X	X	X	X	L	8
Output enable		H	X	L	X	X	X	X	X	X	X	X	8
Data mask / output disable		H	X	H	X	X	X	X	X	X	X	X	
Device deselect		H	X	X	X	X	X	H	X	X	X	X	
No operation		H	X	X	X	X	X	L	H	H	H	X	

(L = low, H = high, V = valid, X = don't care)

Notes:

1. Command can be issued only when both banks have been precharged.
2. SMRS can only be issued if the DQs are idle.
3. The burst stop command is valid only at the full page burst length
4. Bank is selected by BA. BA = low selects bank A. BA = high selects bank B.
5. A new read/write command cannot be isssued during a burst read/write with auto precharge. The new command can be issued t_{RP} after the end of the burst.
6. The write-per-bit function is enabled/disabled at the row active cycle.
7. If the command is asserted during a burst cycle, the device will enter the clock suspend mode.
8. The read latency is two cycles from DQM and zero cycles for the write latency.

Mode Register Field Table

Mode Register Set Command

BA	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0 [1]	Write Mode	MRS		$\overline{CAS}$ Latency			Burst Type	Burst Length		

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	-
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	
1	1	0	
1	1	1	

			Burst Length	
A2	A1	A0	Sequential	Interleave
0	0	0	1	Reserved
0	0	1	2	
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

A9	Write Mode
0	Burst Write
1	Single-Bit Write

A8	A7	MRS
0	0	Mode Register Set
0	1	Reserved
1	0	for
1	1	Vendor Use

A3	Burst Type
0	Sequential
1	Interleave

Note:

1. Maintain BA = low during Mode Register Set.

Special Mode Register Field Table

Special Mode Register Set Command

BA	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X				LC	LM	X				

A6	Load Color Register
0	Disable
1	Enable

A5	Load Mask Register
0	Disable
1	Enable

Note:

1. A5 and A6 cannot simultaneously be set “high” (1) during Special Mode Register Set. This may set the input mask and color registers at an unknown state.

Burst Length and Sequence

Burst Sequence (Burst length = 2)

Initial Column Address	Sequential	Interleave
A0		
0	0, 1	0, 1
1	1, 0	1, 0

Burst Sequence (Burst length = 4)

Initial Column Address		Sequential	Interleave
A1	A0		
0	0	0, 1, 2, 3	0, 1, 2, 3
0	1	1, 2, 3, 0	1, 0, 3, 2
1	0	2, 3, 0, 1	2, 3, 0, 1
1	1	3, 0, 1, 2	3, 2, 1, 0

Burst Sequence (Burst length = 8)

Initial Column Address			Sequential	Interleave
A2	A1	A0		
0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full-Page Burst

Full-page sequential burst is analagous to the tables above. The full-page column burst length is 256 locations.

Pin and Functional Description

Clock (CLK)

All operations are synchronized to the positive rising edge of this clock signal. When the clock enable is active (CKE=high), all valid input signals must be in their valid high or low states at the positive rising edge of the clock and meet specified set-up and hold requirements.

Clock Enable (CKE)

CKE activates or suspends the internal clock. If CKE is asserted high, the next CLK rising edge is valid. If CKE is low, the next rising edge of CLK is not valid and the internal clock is suspended from this point forward as long as CKE remains low. When the internal clock is suspended, the state of the output and burst address is frozen and all other input signals are ignored. If CKE goes low when both banks are in the idle state, the device will enter the power down mode from the next clock cycle. The device will remain in the power down mode and all inputs will be ignored for the duration that CKE remains low. Input signals will be recognized and the device will become active when CKE is asserted high at least t_{IS} + t_{CK} before the rising edge of CLK.

Bank Select (BA)

The device is organized internally with a two-bank memory cell array. The BA input pin determines which bank will be used for operation. When BA is low, bank A is selected. When BA is high, bank B is selected. BA is latched during bank activate, read, write, mode register set and precharge operations.

Address Input (A0 ~ A9)

18 address bits are required to decode the 262,144 x 32 x 2 cell locations. Ten address inputs (A0~A9) are latched at the row activate command for row selection. Eight address inputs (A0~A7) are latched at the read or write command cycle for column selection. A0~A9 are also used to select functions in the Mode Register Set cycle and Special Mode Register Set cycle.

Chip Select ($\overline{CS}$)

$\overline{CS}$ selects the device and enables/disables the latching of commands on the rising edge of CLK. When $\overline{CS}$ is low, command inputs are latched. When $\overline{CS}$ is high, command inputs are not latched and are ignored.

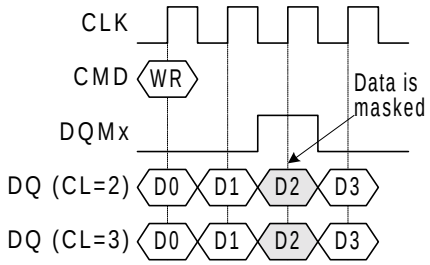
Write Enable ($\overline{WE}$)

The $\overline{WE}$ input, when latched at the rising edge of CLK with $\overline{RAS}$ and $\overline{CAS}$, determines whether the write function will be enabled or disabled. The $\overline{WE}$ input is also used to select the bank activate, read, write or precharge commands. See the truth table for detail.

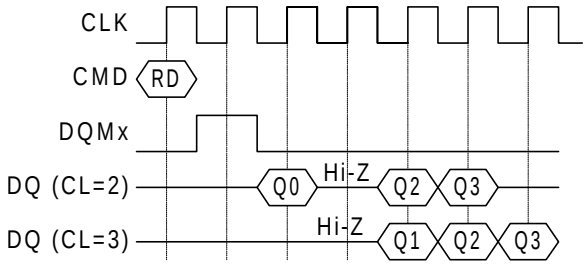
Data Input/Output Mask (DQM0 ~ DQM3)

DQM0~DQM3 enables the output buffers during a Read cycle or can mask data during a Write cycle. When DQM is asserted high during a Read cycle at the rising edge of CLK, the output data buffer is disabled after two clock cycles. If DQM is low, the output data buffer is enabled. When DQM is asserted high during a Write cycle at the rising edge of CLK, the data at the same clock cycle is masked and not written to memory. If DQM is low, the data is not masked and is written to memory. DQM0~DQM3 corresponds to the output data in the following manner: DQM0 = DQ0 to DQ7, DQM1 = DQ8 to DQ15, DQM2 = DQ16 to DQ23, DQM3 = DQ24 to DQ31.

Write (BL = 4)



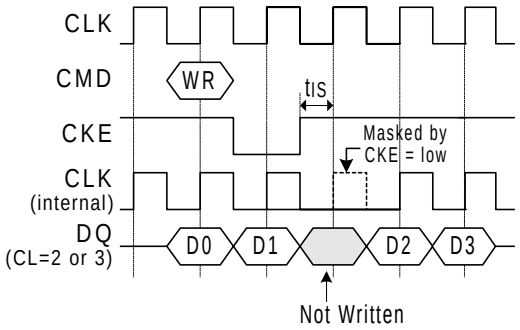
Read (BL = 4)



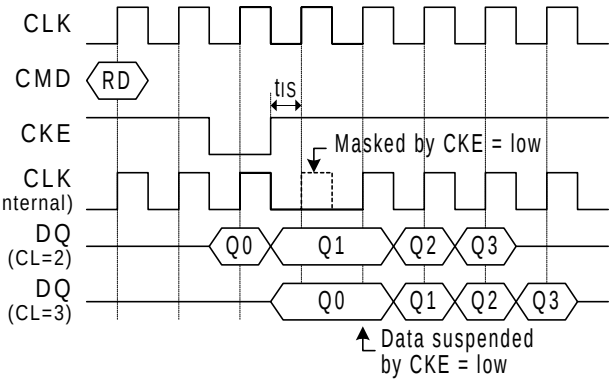
Clock Suspend Mode

The internal clock may be suspended by asserting CKE to the low state in the active bank. The state of the bank will not change while the clock is suspended. If CKE=low is asserted while both banks are in the idle state, power down mode will be initiated. Asserting CKE=high will resume the internal clock operation. If the device is in the power-down mode when CKE is asserted high, internal clock operation will resume. The device will then exit power-down and all disabled buffers are placed into the active state.

Clock Suspended During Write



Clock Suspended During Read



Define Special Function (DSF)

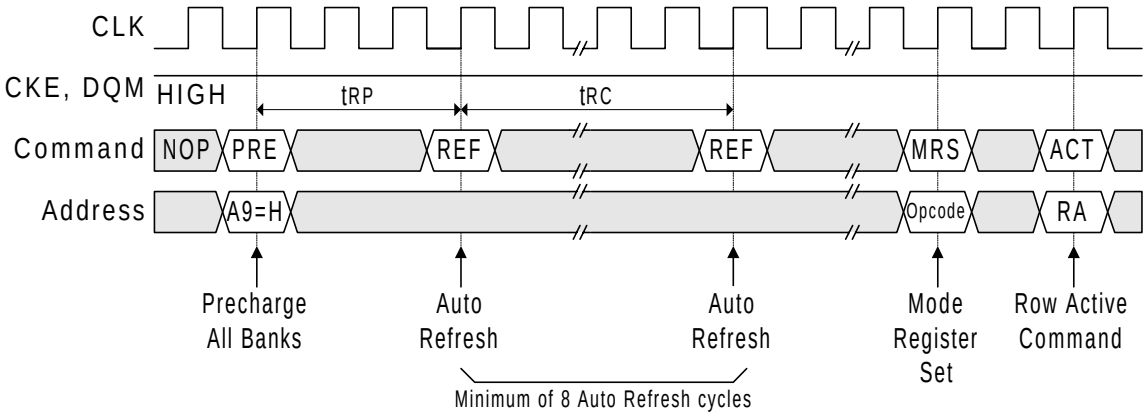
When used in conjunction with $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ at the rising edge of CLK, the DSF input controls the device's graphic functions; write-per-bit, block write and special mode register set command. When DSF=high, the graphics functions are enabled. When DSF=low, the graphics functions are disabled and the SGRAM functions like a standard x32 SDRAM.

NOP and Device Deselection

No operation (NOP) occurs when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high. A NOP is used to produce a "wait state" since it does not initiate a new device operation. $\overline{CS}$ asserted to a high state is considered a NOP and $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF and all address inputs are ignored.

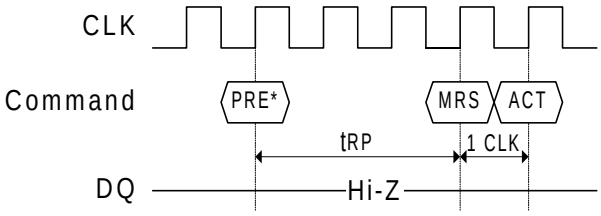
Power-Up Sequence

1. Apply power and start clock. Maintain CKE=high, DQM=high. All other input pins should be in the NOP condition.
2. Maintain power, clock, CKE=DQM=high and NOP input conditions for a minimum of 200 µs.
3. Precharge all banks.
4. Perform a minimum of two auto refresh cycles.
5. Perform the mode register set command to initialize the mode register. (The MRS command may be performed before or after the two minimum auto refresh cycles).
6. Device is ready for normal operation.



Mode Register Set (MRS)

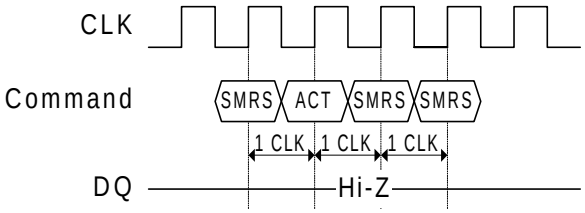
The Mode Register Set command sets the values in the mode register which determines burst length, burst type and $\overline{CAS}$ latency. The default values in the mode register after power-up are undefined. Therefore, this command must be issued after power-up to ensure proper operation. The mode register can be set only when both banks are in the idle state. Refer to the table and timing diagrams for the codes associated with the various operational mode settings.



Note*:
Precharge if necessary. MRS can be issued only when both banks are in the precharged state.

Special Mode Register Set (SMRS)

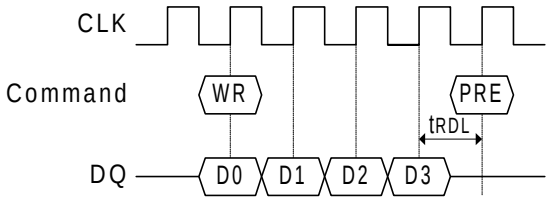
The special mode register set command loads the “color register” and “mask register” which are used in the block write and write-per-bit graphics functions of the device. The 32-bit write mask register provides the I/O mask data which is used during the write-per-bit and masked block write functions. The 32-bit color register is used in the block write function. When A5 is high, the write mask data present on the input data pins is latched into the mask register. When A6 is high, the color data present on the input data pins is latched into the color register. If both A5 and A6 are high simultaneously, the data written in the mask and color register is unknown. The SMRS command can be issued when the device is in the active state with idle I/O. Data written in the mask and color registers will remain valid until it is re-written or the power to the device has been interrupted.



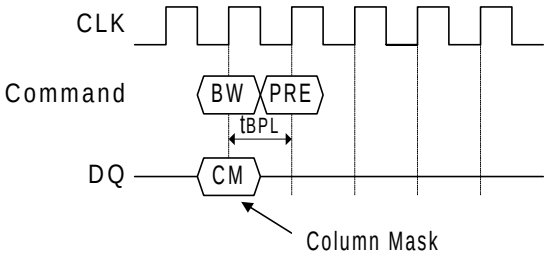
Single-Bank Precharge

The precharge command precharges the bank designated by the bank select pin BA. The precharge command can be issued after $t_{RAS(min.)}$ from the bank activate command of the selected bank. A time of t_{RP} is required to precharge the selected bank. The selected bank will switch from the active state to the idle state after being precharged.

Normal Write (BL = 4)

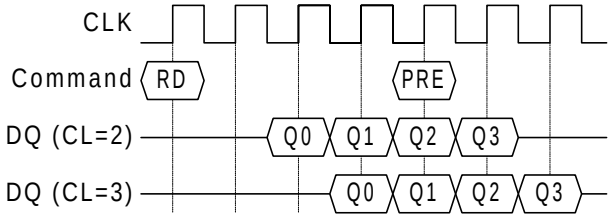


Block Write



Read (BL = 4)

Note:
A maximum of one data is valid after the precharge command for CL = 2; two valid data for CL = 3.



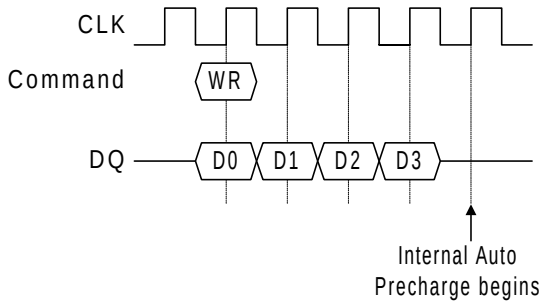
Precharge Both Banks

This command precharges both banks simultaneously. The command is initiated in a similar manner as the bank precharge command except BA=don’t care and A9=high. Both banks will be switched to the idle state upon completion of the precharge operation.

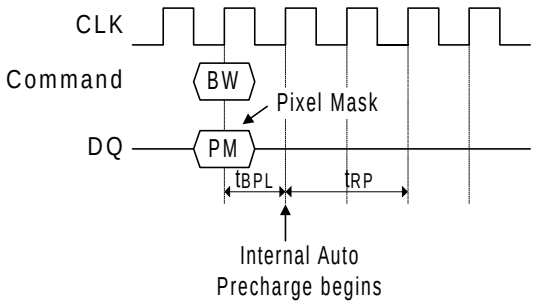
Auto Precharge

Auto precharge is used in conjunction with Read, Write and Block Write. A precharge operation is automatically performed after the completion of these operations. The Read, Write and Block Write with auto precharge cannot be interrupted by any other command. A delay of t_{RP} is required from the start point of the internal auto refresh operation before a new row activate command can be issued to the selected precharged bank.

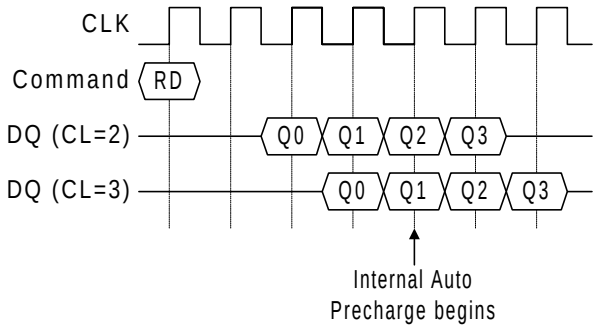
Normal Write (BL = 4) with Auto Precharge



Block Write with Auto Precharge

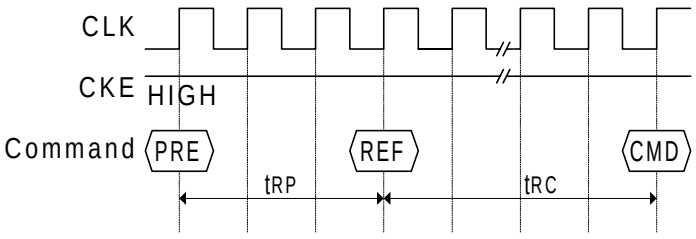


Read (BL = 4) with Auto Precharge



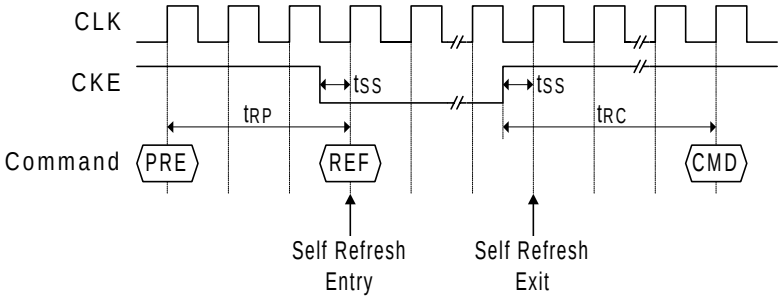
Auto Refresh

The Auto Refresh command is used to refresh the dynamic memory cells in the device by using row addresses provided by an internal refresh address counter. The two internal memory banks are refreshed alternately and the refresh address counter is incremented automatically. The auto refresh command can only be asserted when both banks are in the idle state and the device must not be in the power down mode. A time period of t_{RC} is required to complete the auto refresh operation. The auto refresh command must be followed by NOPs until the refresh operation is complete. The auto refresh must be performed to each memory cell within 32ms to maintain data integrity. The auto refresh is commonly performed once every 15.6µs or a burst of 2048 auto refresh cycles in 32ms may be performed. Both banks will be in the idle state at the end of the auto refresh operation.



Self Refresh

The self refresh command refreshes the dynamic memory cells in the device by utilizing both an internal timer and refresh address counter. When the device is in the self refresh mode, the internal clock and all input and output buffers, except the CKE buffer, are disabled. Self refresh is a common mode used for data retention and low power operation. Entry into the self refresh mode is executed when both banks are idle and $\overline{WE}$=high and $\overline{CS}$=$\overline{RAS}$=$\overline{CAS}$=CKE=low. After the device has entered self refresh mode, CKE must remain low to keep the device in the self refresh mode. All other inputs including CLK are ignored. Exiting from self refresh mode is accomplished by restarting and stabilizing the external CLK prior to placing CKE=high. Once CKE=high, NOP commands must be issued for $t_{RC(min.)}$ before resuming normal operation.



Bank Activate

The bank activate command selects a random row from an idle bank specified by BA. A read or write command may be issued after t_{RCD} from the bank activate command to access the activated bank and row. The selected bank must remain active for $t_{RAS(min.)}$. This is the minimum time required for the device to activate and complete the sense/restoration of the selected row/bank of memory cells. The maximum time that a bank can be in the active state is $t_{RAS(max.)}$. A delay of $t_{RRD(min.)}$ must occur between the activation of different banks to allow time for internal stabilization.

Burst Read

The burst read command accesses consecutive data locations from an active row of an active bank. The $\overline{CAS}$ latency, burst length and burst type are specified in the Mode Register Set command. The bank must be active for a minimum of t_{RCD} before issuing the burst read command. The first data output will appear at the I/O after the predetermined $\overline{CAS}$ latency clock cycles from the burst read command. The remaining data burst will follow on the consecutive rising edges of CLK. The burst read can be initiated on any column address of the active row. The output will go into the high impedance state at the end of the burst unless a new burst read command was initiated to produce a gapless stream of output data. The burst read can be terminated by: (1) issuing another burst read or write to the same bank, (2) issue a precharge command to the same bank, (3) issue a burst read or write to the other active bank. The burst stop command is valid only for the full page burst length.

Burst Write

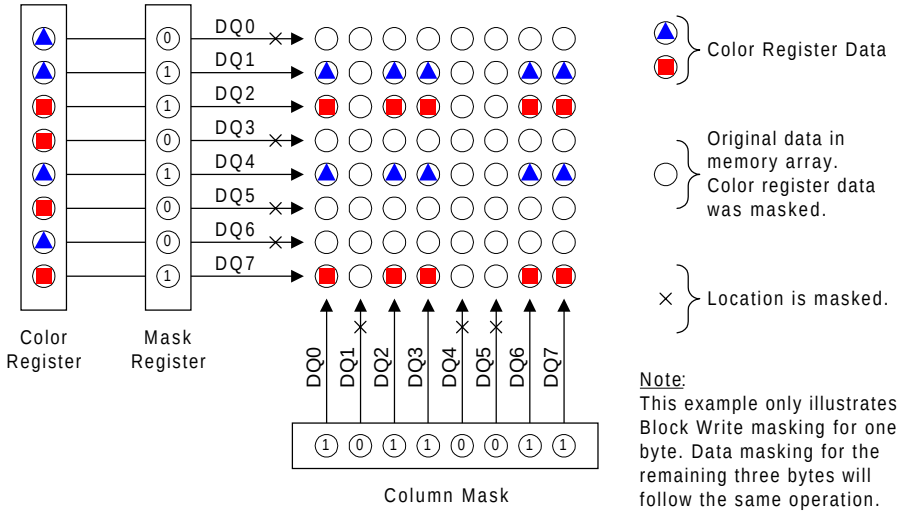
The burst write command writes data into the device on consecutive clock cycles into consecutive column addresses. The burst length and burst type are specified in the mode register set command. The initial column address is provided along with the input data in the same clock cycle as the burst write command. The burst write command can be terminated by: (1) issue burst write to the same bank, (2) issue a burst write to the other active bank, (3) issue a burst read with DQM to mask the data inputs, (4) precharge the bank after a delay of t_{RDL} from the last data input to the active row (use DQM to mask input data). The DSF input signal must be low during a burst write operation to ensure that the I/O write data is written into the memory array. See timing diagram for detail.

Write-Per-Bit

Data written into the device may be masked on a bit basis by invoking the write-per-bit function. The DSF bit is set high in the bank activate command which is executed t_{RCD} before the burst write command. The mask which is used on the input data was previously specified in the Special Mode Register Set Command and is stored in the mask register. When the mask register data bit=1, the associated input data bit is written into the memory array. If the mask register data bit=0, the associated input data bit is masked and not written into the memory array.

Block Write

The block write command performs a block write operation to the bank selected by BA. Block write performs simultaneous writing of data into eight consecutive column locations during a single access cycle. The initial column address location and column mask data is specified during the block write command. The consecutive column addresses are generated internally. The data which will be written into the memory array comes from the internal 32-bit color register. The contents of the color register and mask register are specified with the Special Mode Register Set Command. The data in the color register may or may not be written into the memory array depending upon the mask register, column mask and DQM. The internal mask register will be enabled if DSF=high during the Bank Activate Command. If DSF=low during the Bank Activate Command, the internal mask register will be disabled. The color register data will be written into the memory array if the mask register and column mask register data are asserted high (“1”); a low (“0”) will mask the data and will not be written in the memory array. Block writes are non-burst writes and are independent of the burst length that was specified in the mode register set command. Back-to-back block writes may be performed if they are delayed by t_{BWC}.

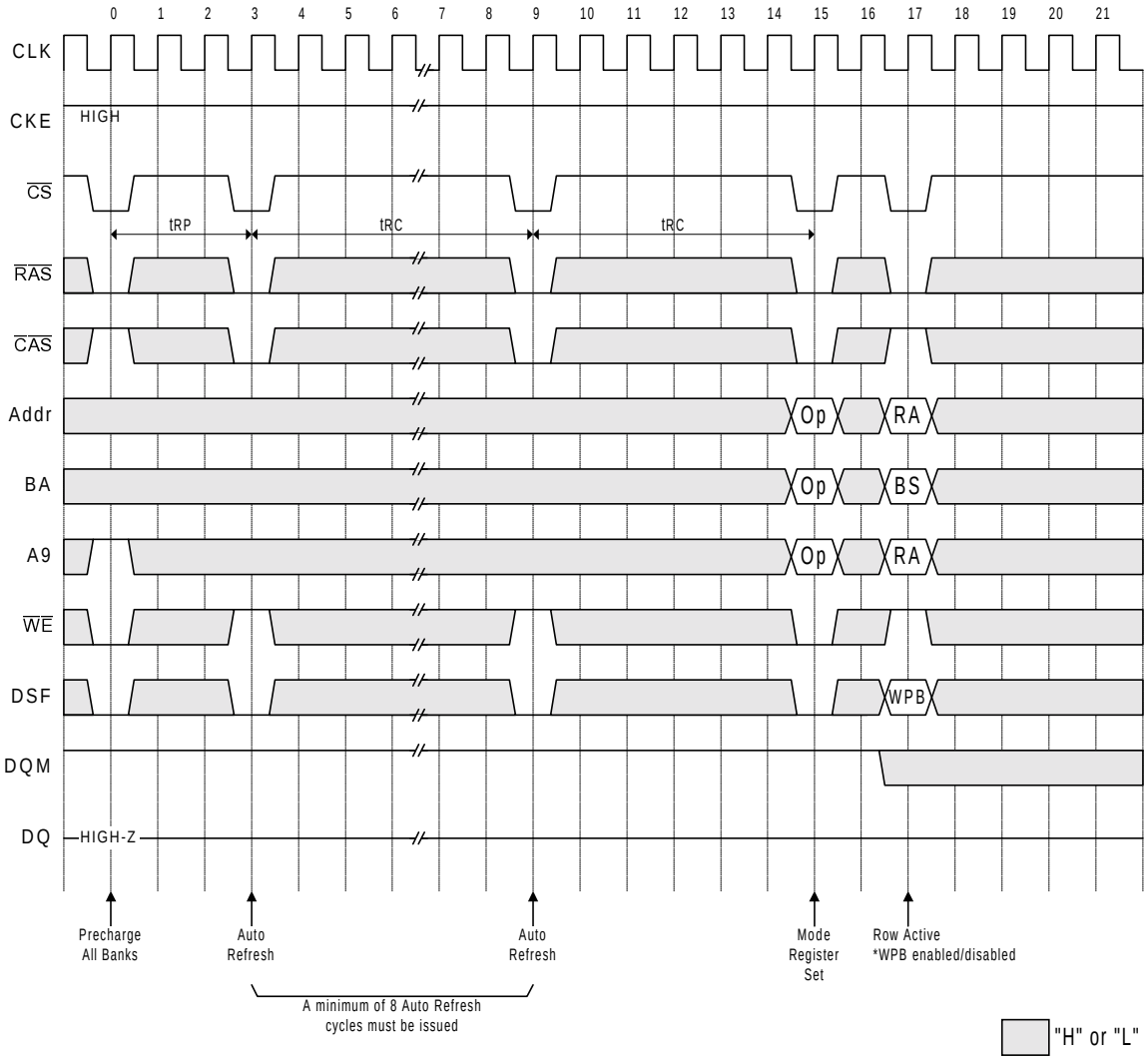


Block Write Column	32 bits per column			
	Bits 0 ~7	Bits 8 ~ 15	Bits 16 ~ 23	Bits 24 ~ 31
0	DQ0	DQ8	DQ16	DQ24
1	DQ1	DQ9	DQ17	DQ25
2	DQ2	DQ10	DQ18	DQ26
3	DQ3	DQ11	DQ19	DQ27
4	DQ4	DQ12	DQ20	DQ28
5	DQ5	DQ13	DQ21	DQ29
6	DQ6	DQ14	DQ22	DQ30
7	DQ7	DQ15	DQ23	DQ31

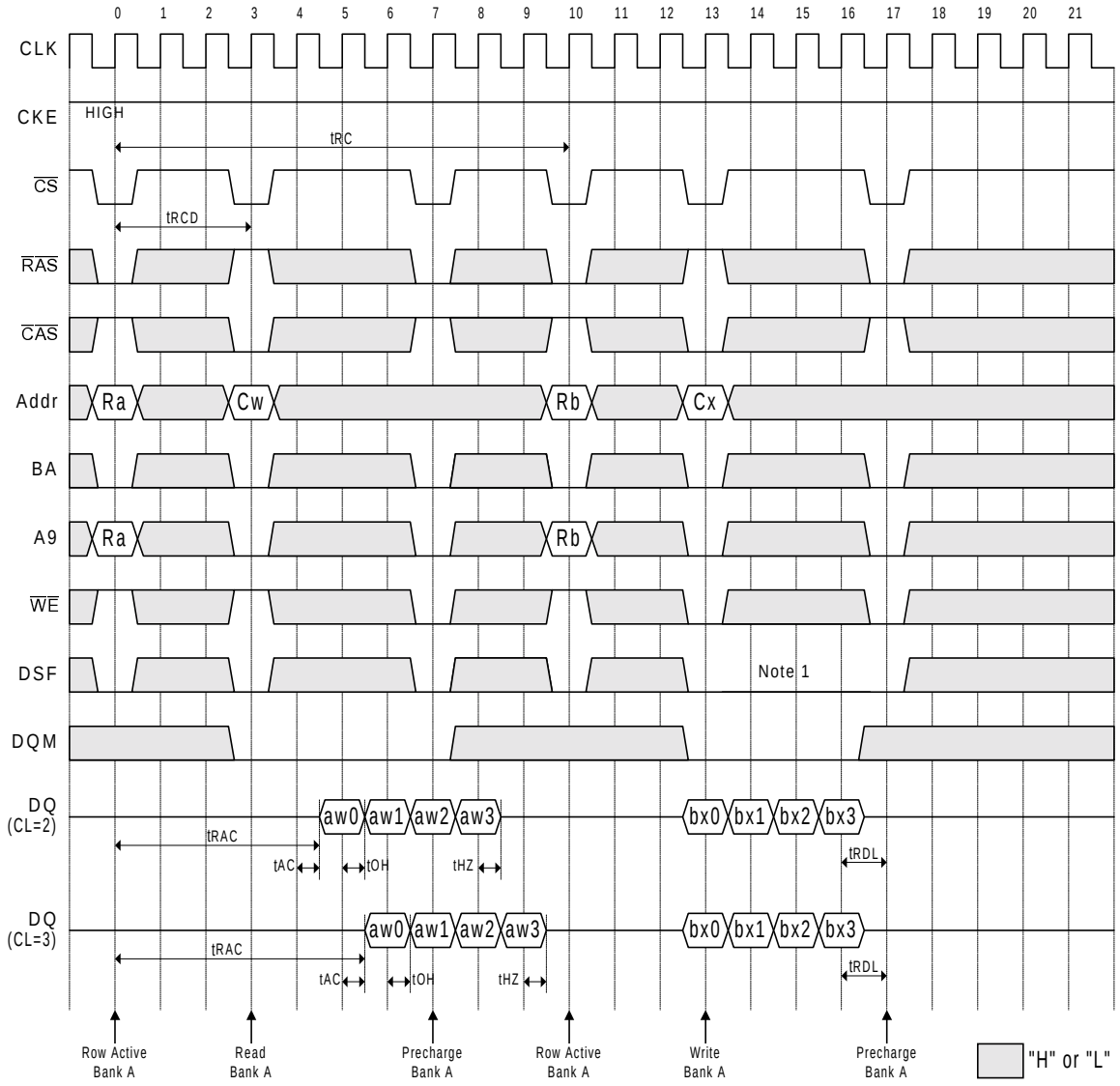
Column Mask

This table depicts the relationship of DQ versus data byte and column. For example, if bits 0 thru 7 of all 8 columns in the block write operation are to be masked, a low “0” is placed on DQ0 thru 7 at the Block Write Command cycle.

Power-Up Sequence

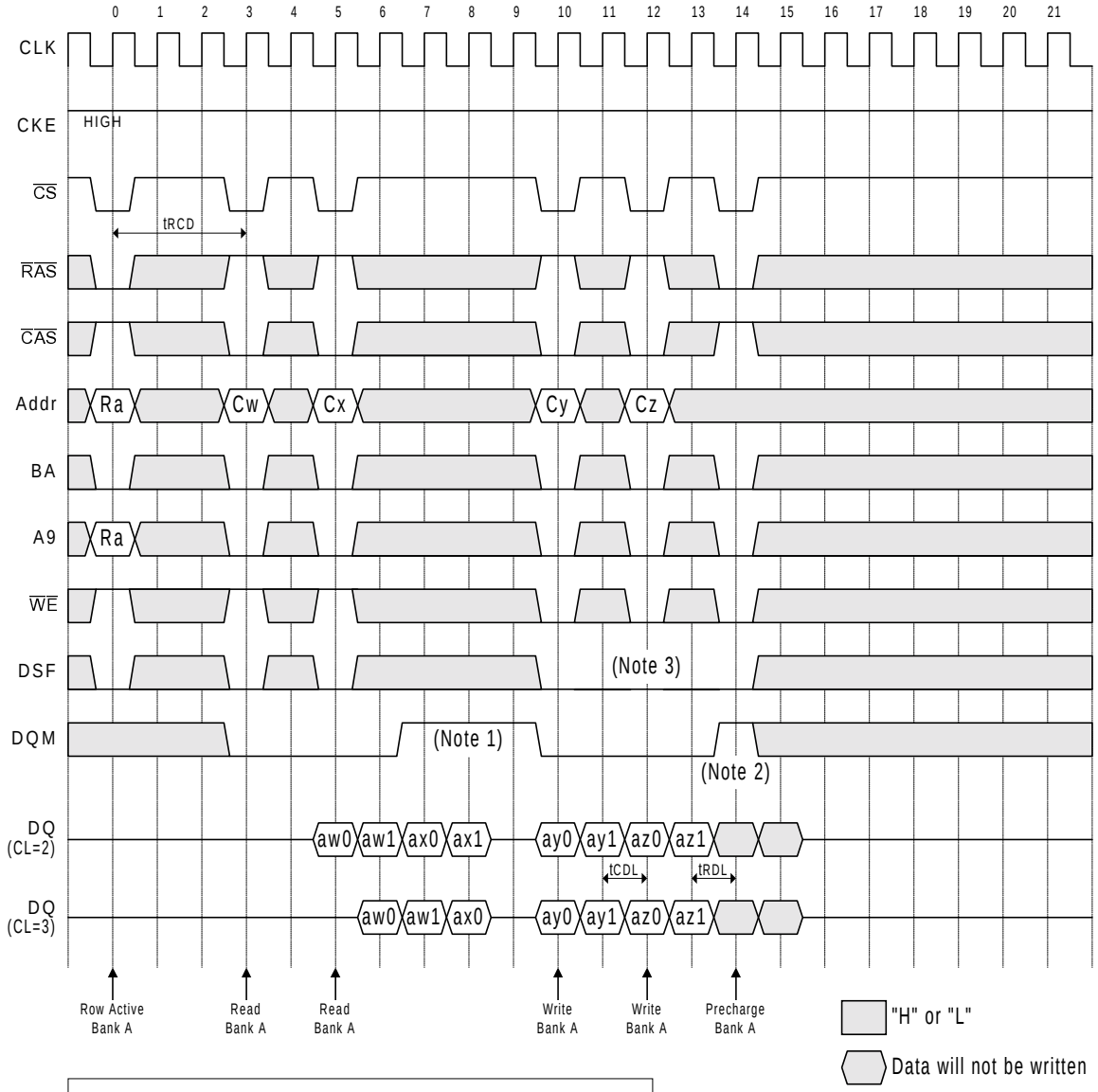


Read/Write Cycle
(same bank, burst length = 4)



Note 1: DSF must be low during a burst write operation.

Read/Write Cycle
(same bank, burst length = 4)

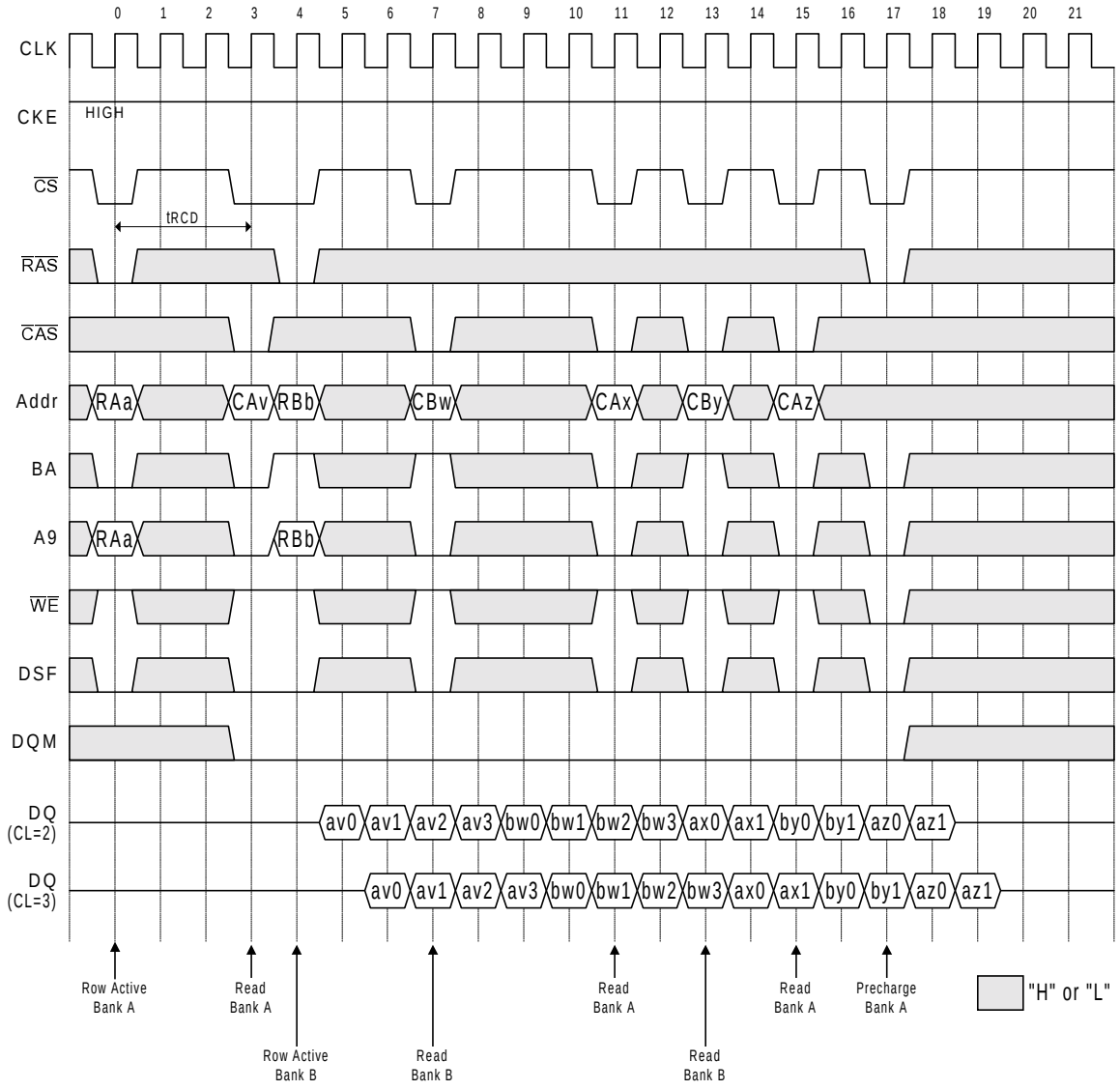


Note 1: When data is written prior to the ending of a burst read, DQM is asserted 3 cycles before the write command to avoid bus contention.

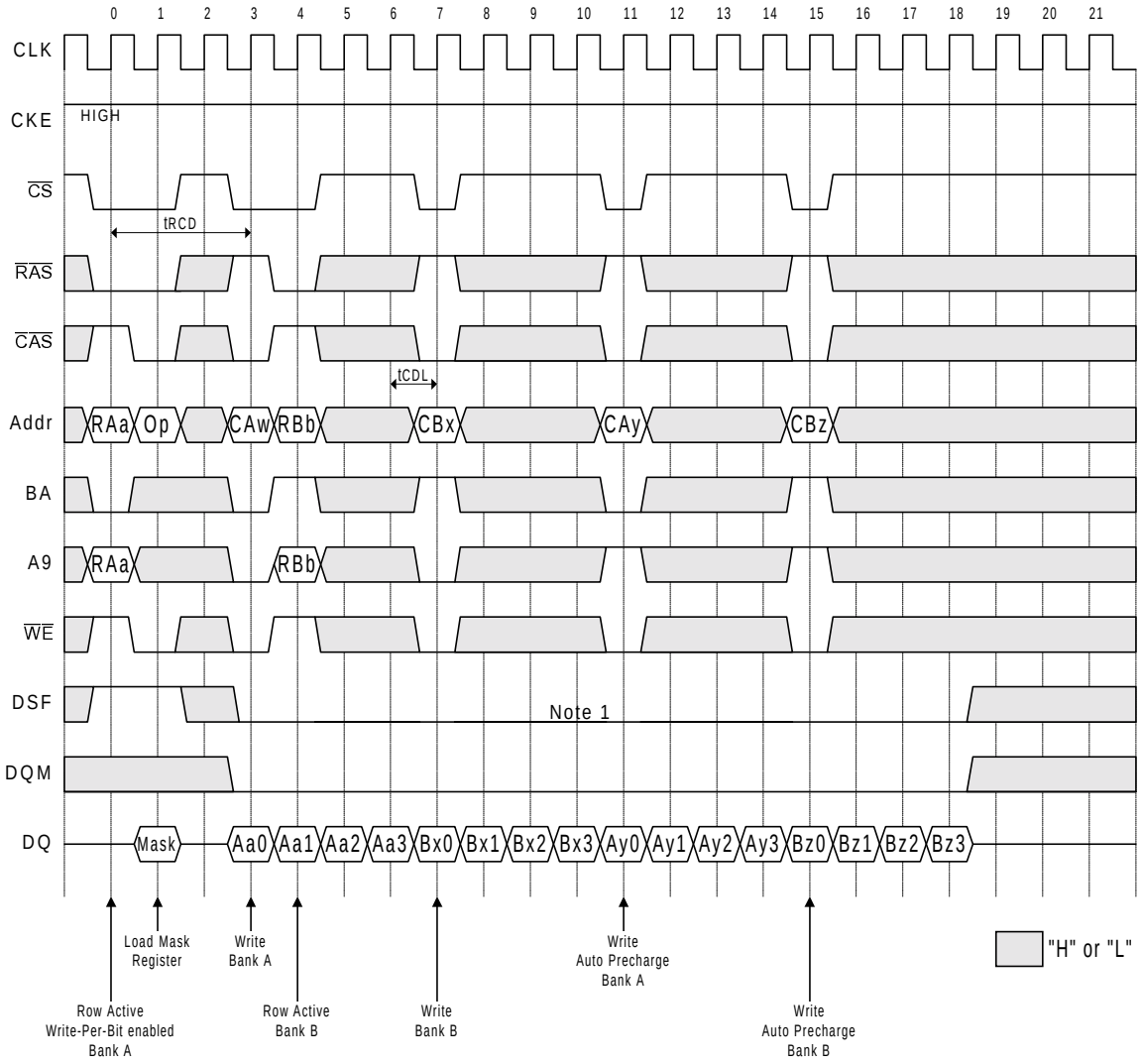
Note 2: When interrupting a write burst with precharge, DQM should be used to mask the input data at the precharge cycle to avoid data corruption.

Note 3: DSF must be low during a burst write operation.

Read Cycle
(interleaved banks, burst length = 4)

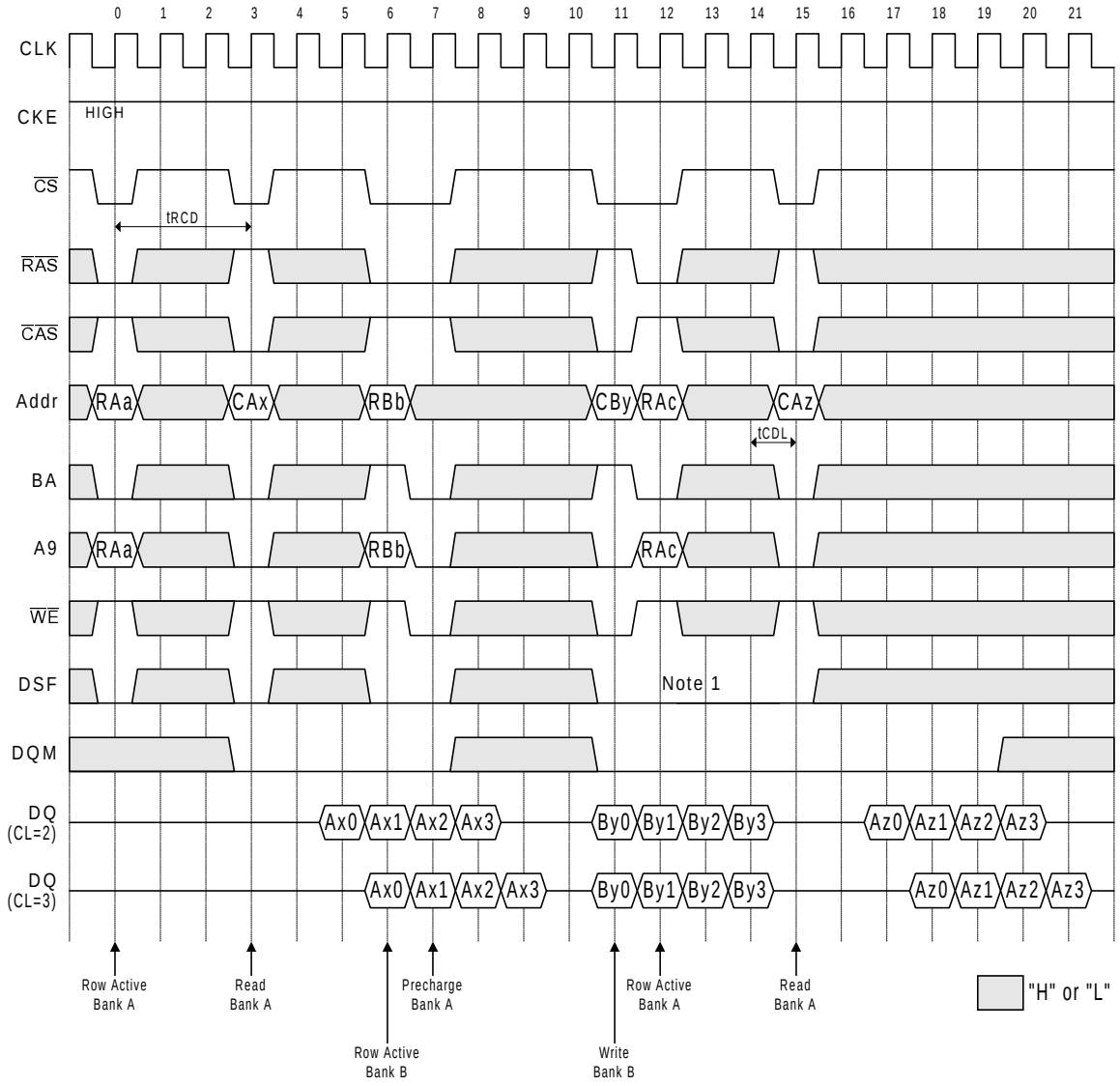


Write Cycle
(interleaved banks, burst length = 4)



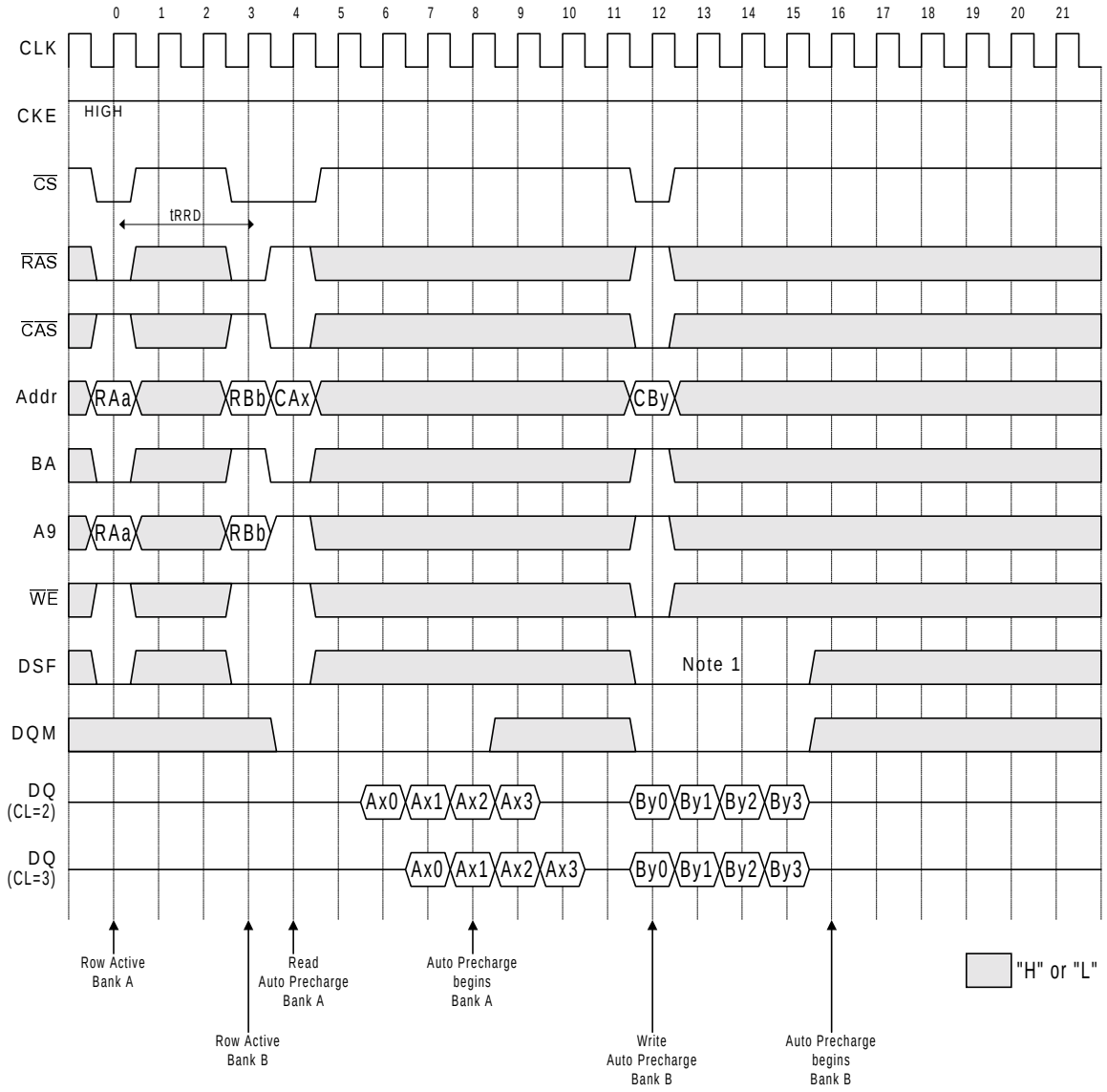
Note 1: DSF must be low during a burst write operation.

Read/Write Cycle
(interleaved banks, burst length = 4)



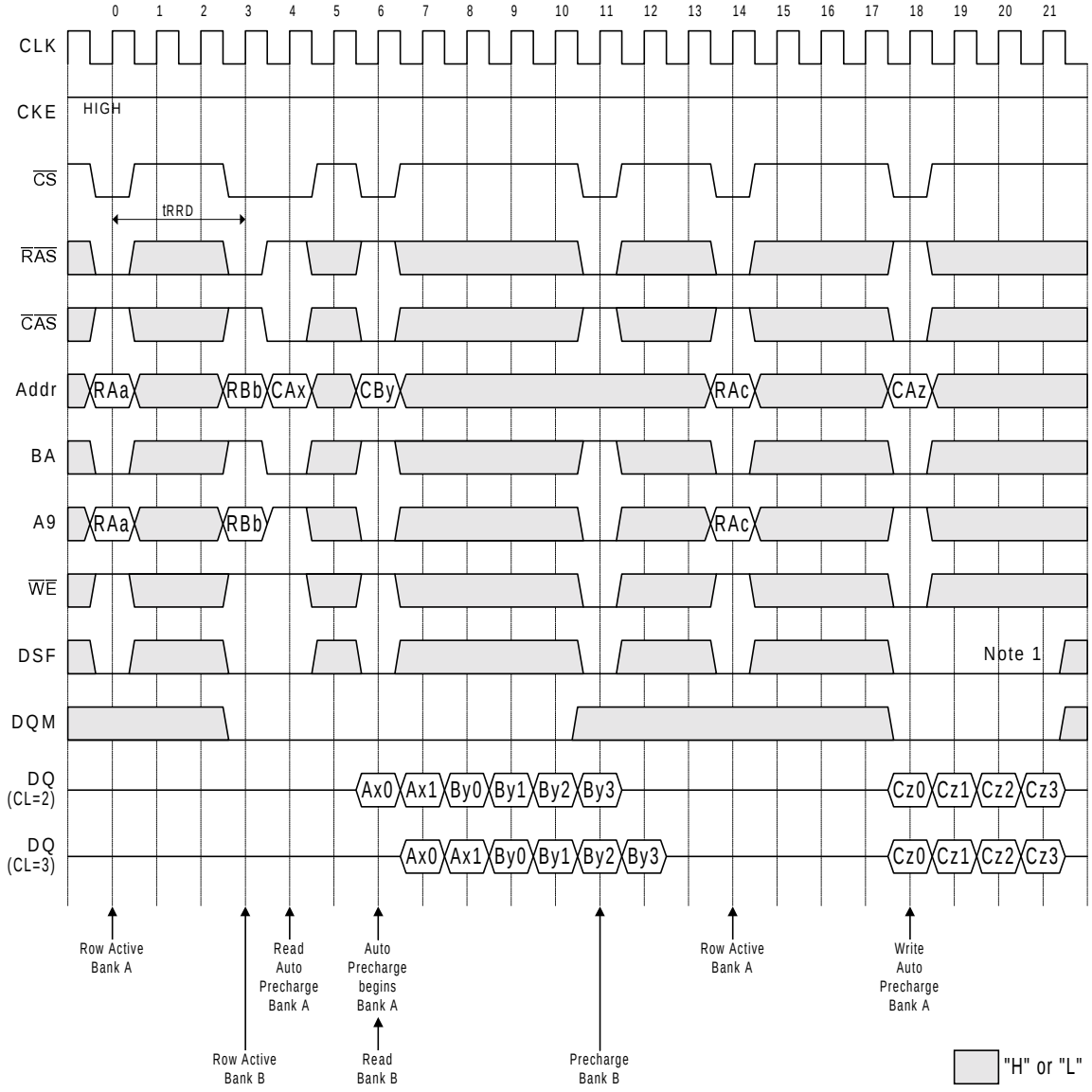
Note 1: DSF must be low during a burst write operation.

Read/Write Cycle
(interleaved banks, auto precharge, burst length = 4)



Note 1: DSF must be low during a burst write operation.

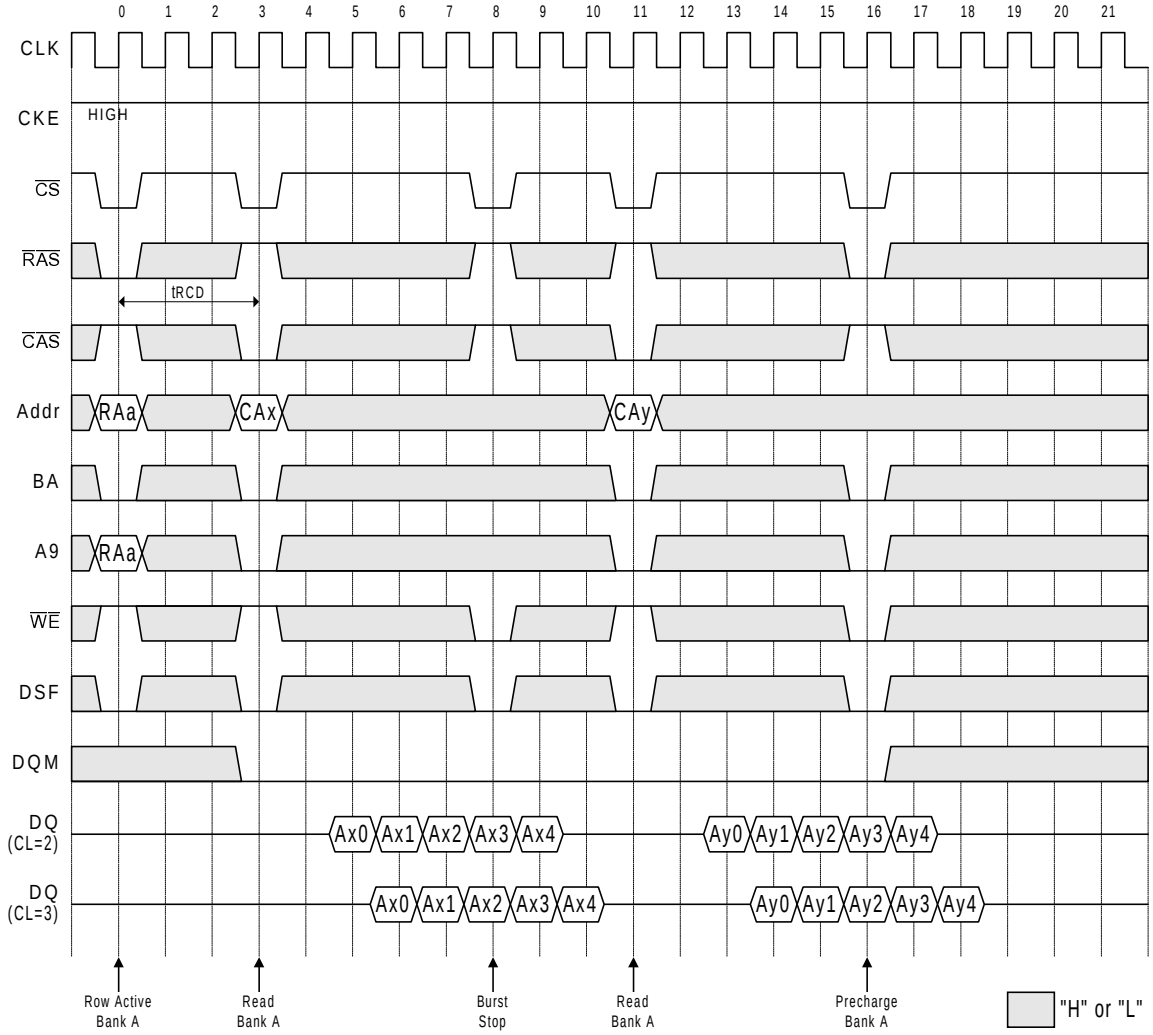
Read/Write Cycle
(interleaved banks, auto precharge, burst length = 4)



Note 1: DSF must be low during a burst write operation.

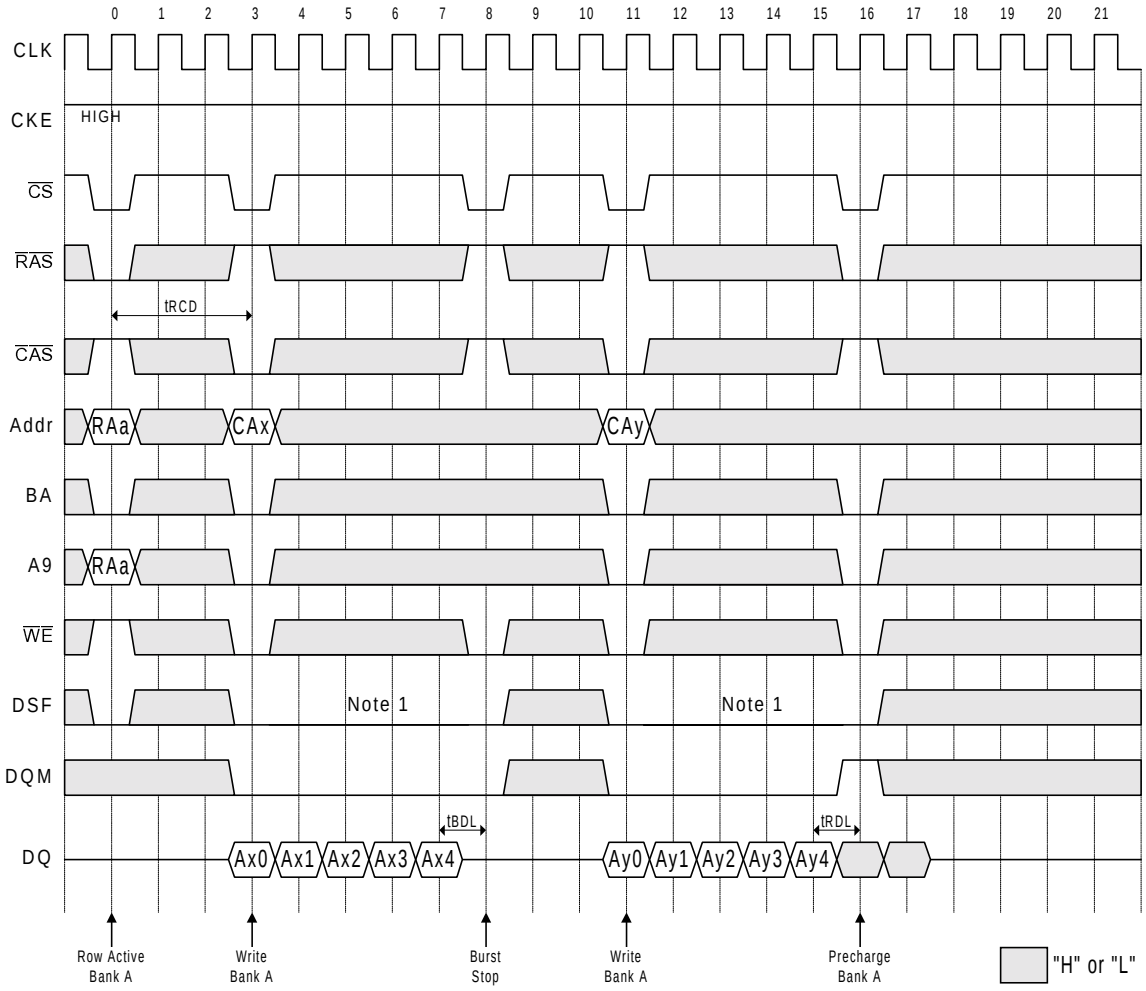
Note:
- A delay of tRP must be met before issuing a new command to a bank that is in the precharge operation.
- If a read/write command is issued before the other bank's auto precharge operation (read/write with auto precharge) has begun, the auto precharge will begin at the point of issuance of the read/write command.

Read Cycle interrupted by Burst Stop and Precharge Command (full page burst)



Note:
- Full page burst Read with Auto Precharge is not a valid operation. The burst data wraps around at the end of the burst.
- The number of valid output data after a burst stop or precharge = "$\overline{CAS}$ latency-1". Ex: CL=2, one data is valid after a burst or precharge.

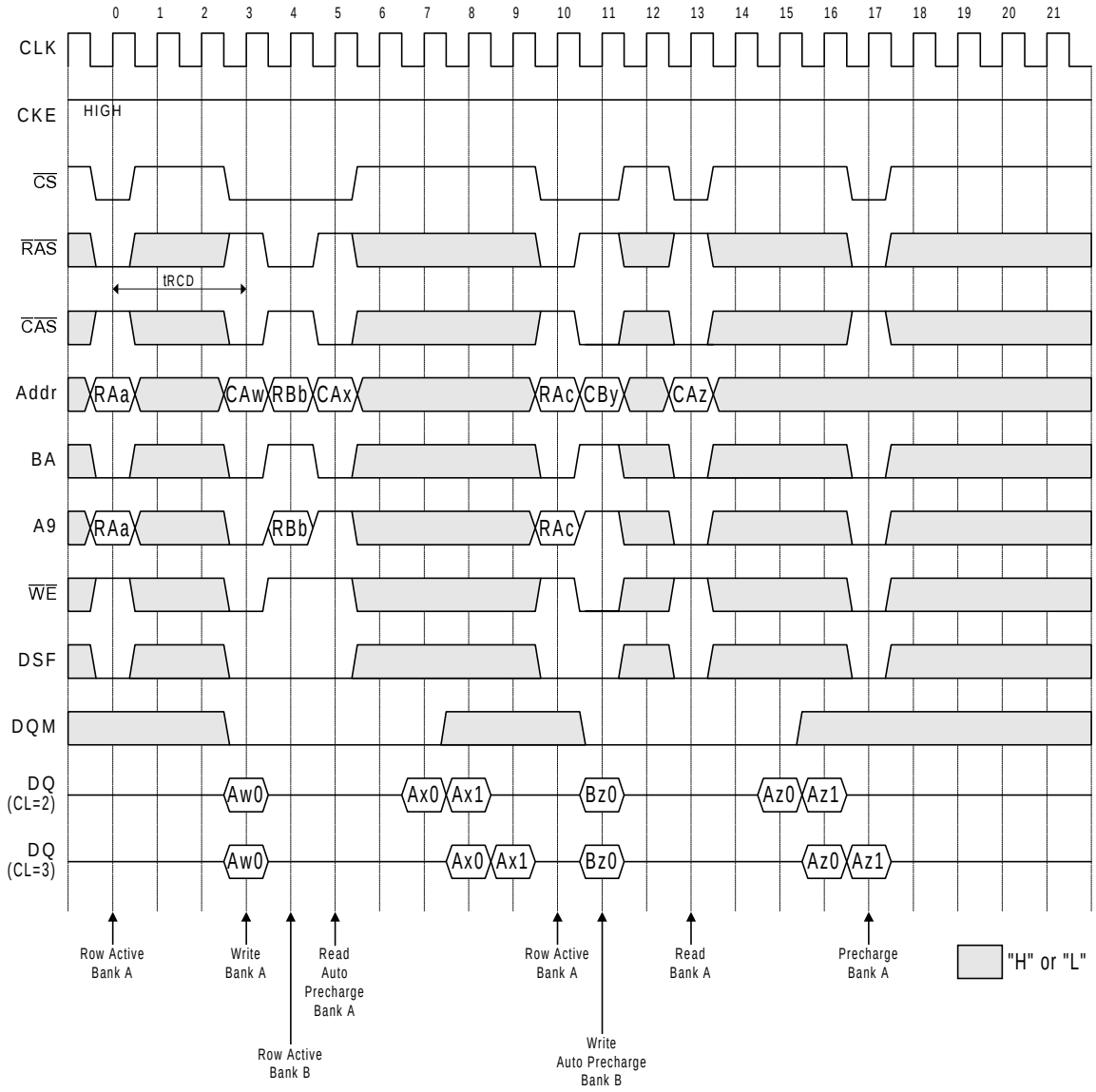
Write Cycle interrupted by Burst Stop and Precharge Command (full page burst)



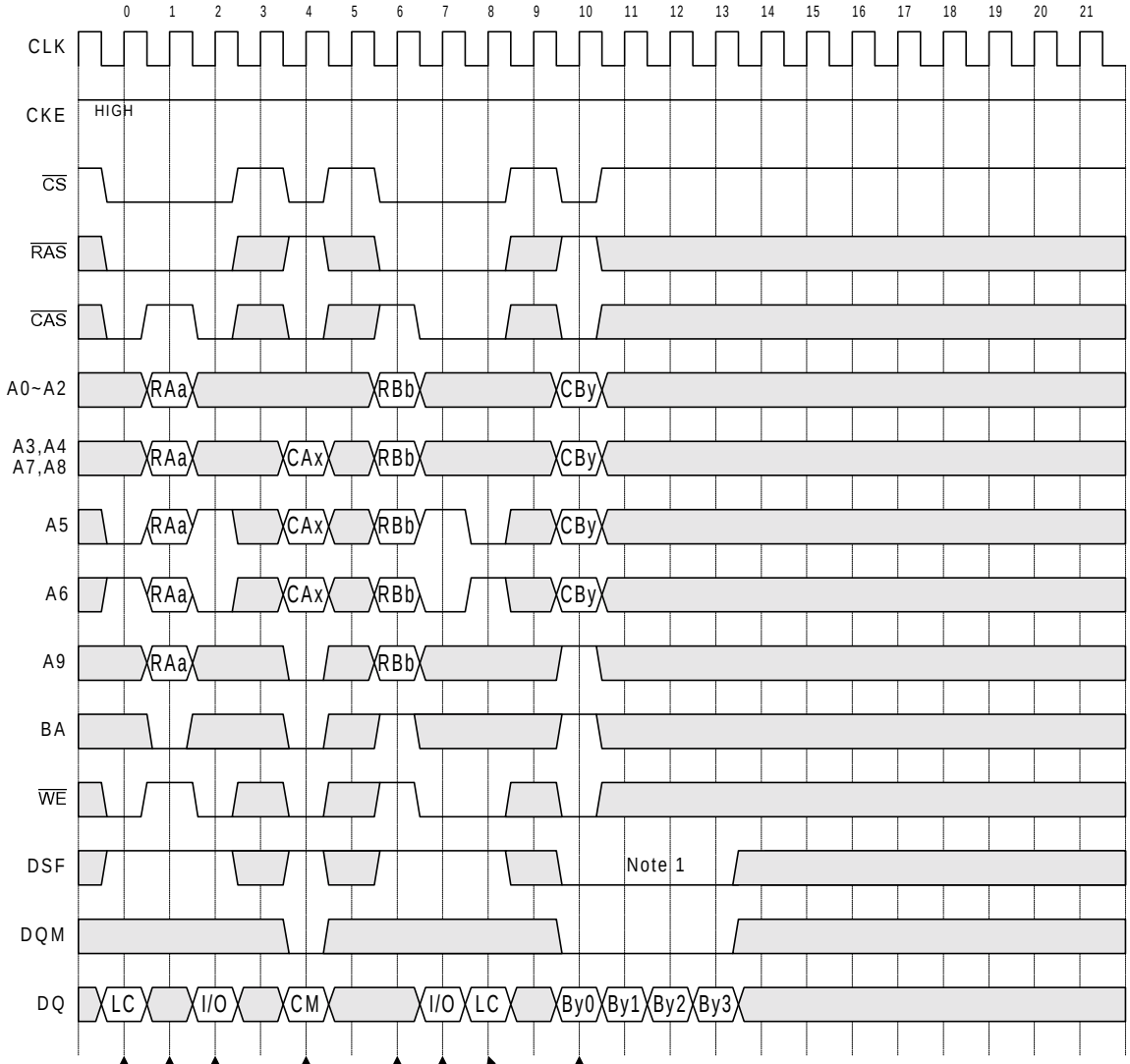
Note 1: DSF must be low during a burst write operation.

Note:
- Full page burst Write with Auto Precharge is not a valid operation. The burst data wraps around at the end of the full page burst.
- When the Precharge command is asserted prior to the completion of the burst, DQM should be asserted at the precharge command to ensure data integrity by masking data input.
- t_{BDL} and t_{RDL} must be maintained to prevent the input data present at the Burst Stop and Precharge Command to be written into the memory.

Burst Read, Single Write Cycle (burst length = 2)



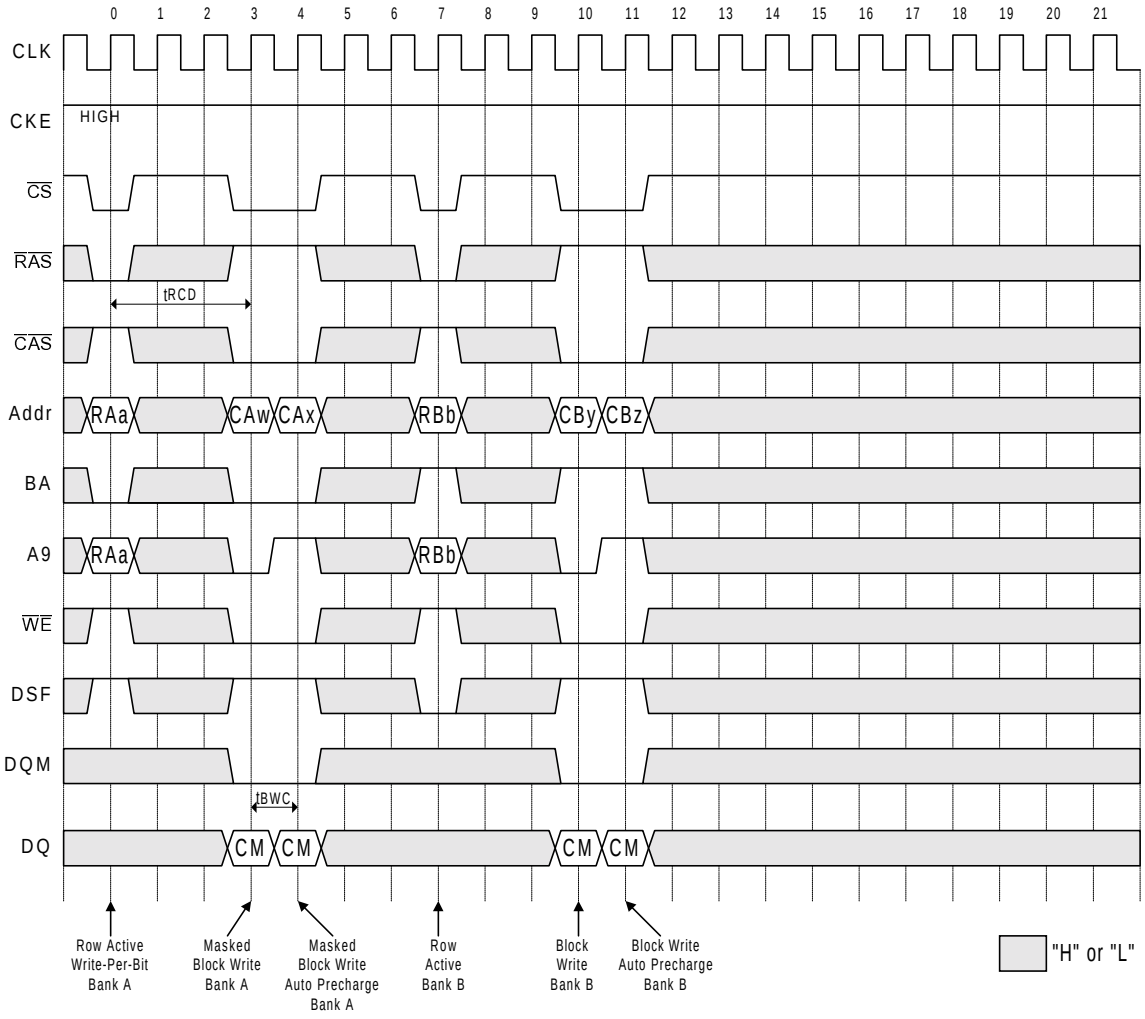
Special Mode Register Set Command with Block Write and Normal Write (burst length = 4)



Definition:
- LC = Load color register
- I/O = Load I/O mask register
- CM = Column mask used with the masked block write command.

Note 1: DSF must be low during a burst write operation.

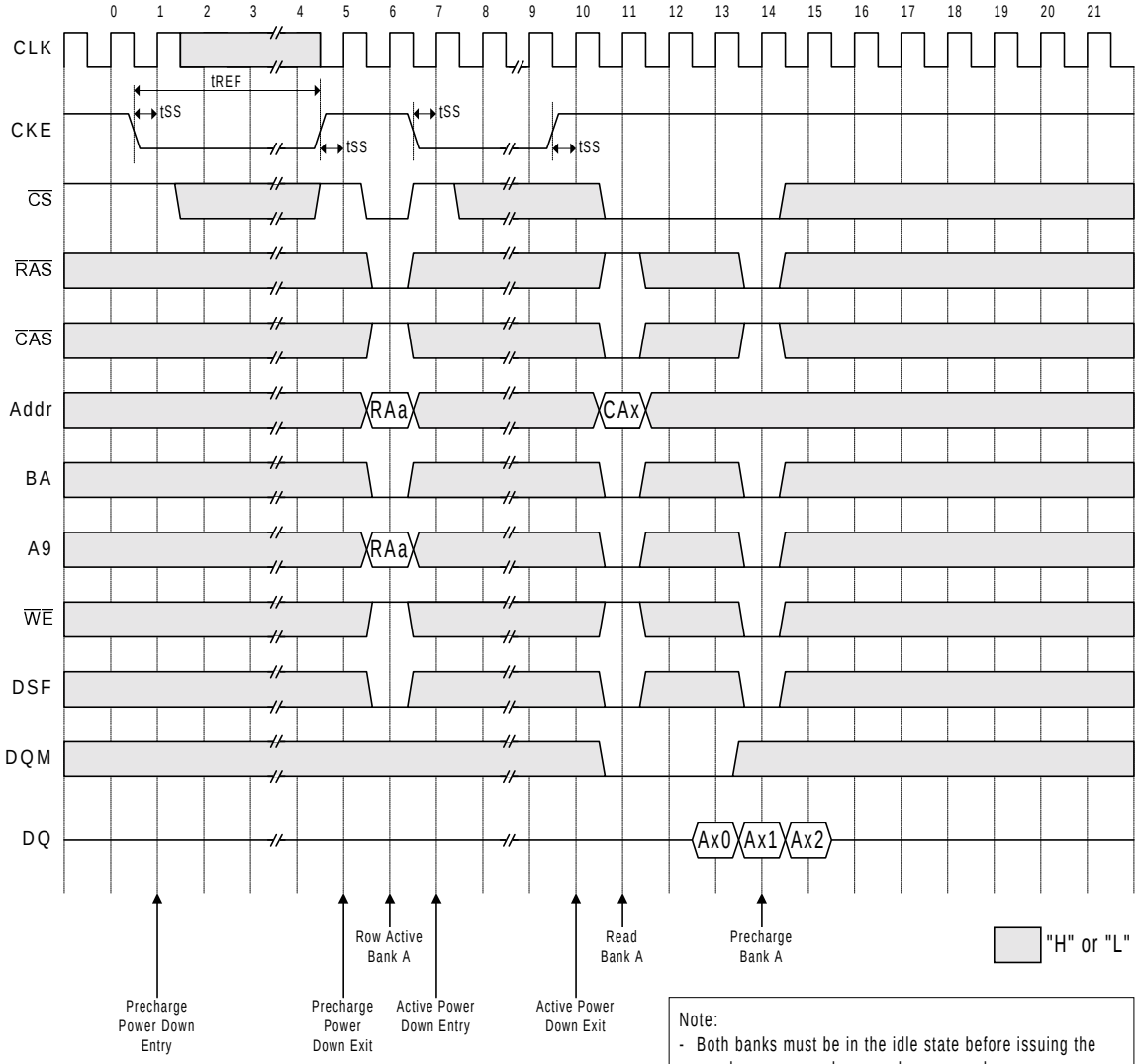
Block Write Cycle with Auto Precharge



Note:
- When DQ=low, column data mask is enabled. When DQ=high, column data mask is not enabled and new data is written into memory.
- Column addresses A0~A2 are ignored. The 3 LSB's are incremented internally for the 8-column block write operation.

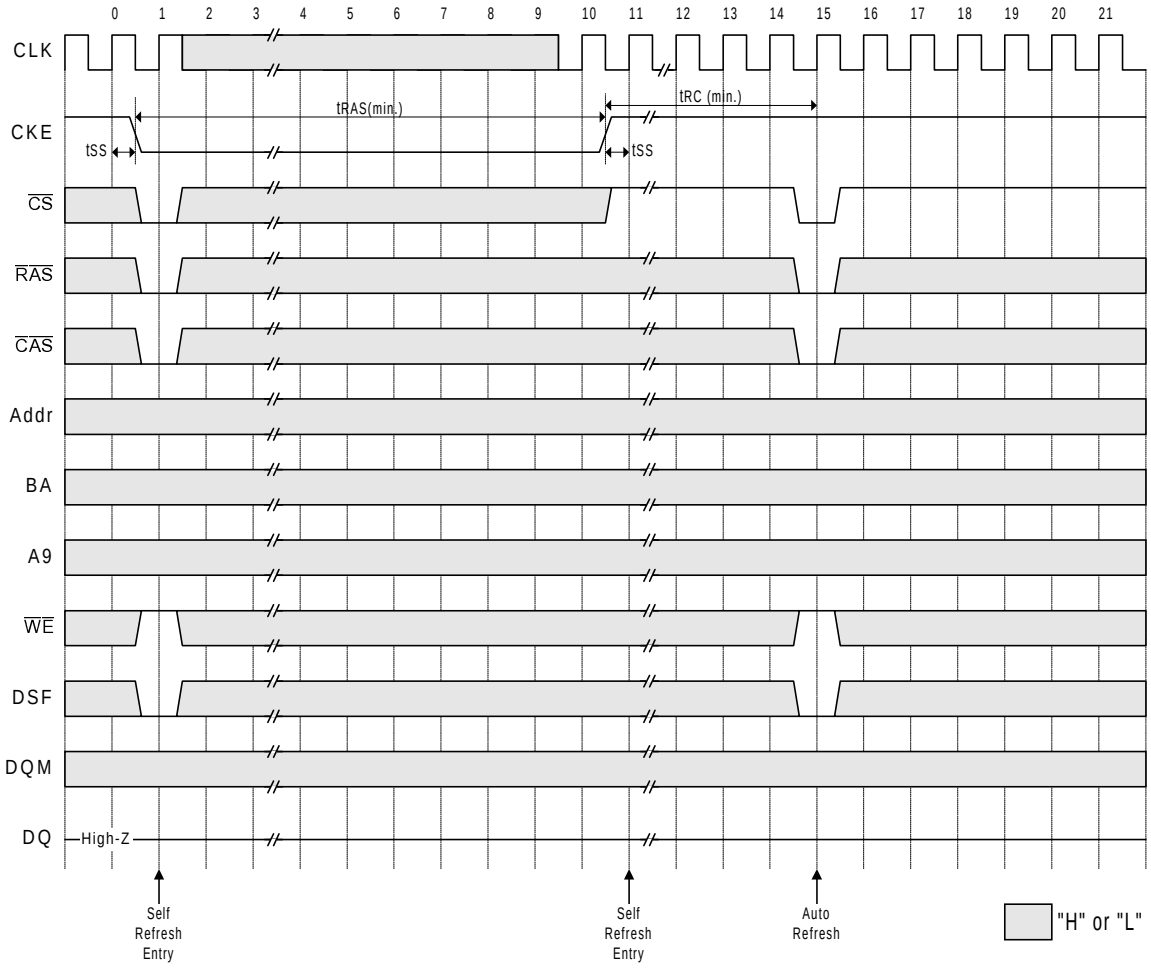
Definition:
- CM = Column mask for the masked block write operation. See column mask versus DQ table.

Active/Precharge Power Down ($\overline{CAS}$ latency = 2, burst length = 4)



Note:
- Both banks must be in the idle state before issuing the precharge power down mode command.
- CKE should be high for a period of "tCK + tSS" before the row active command.

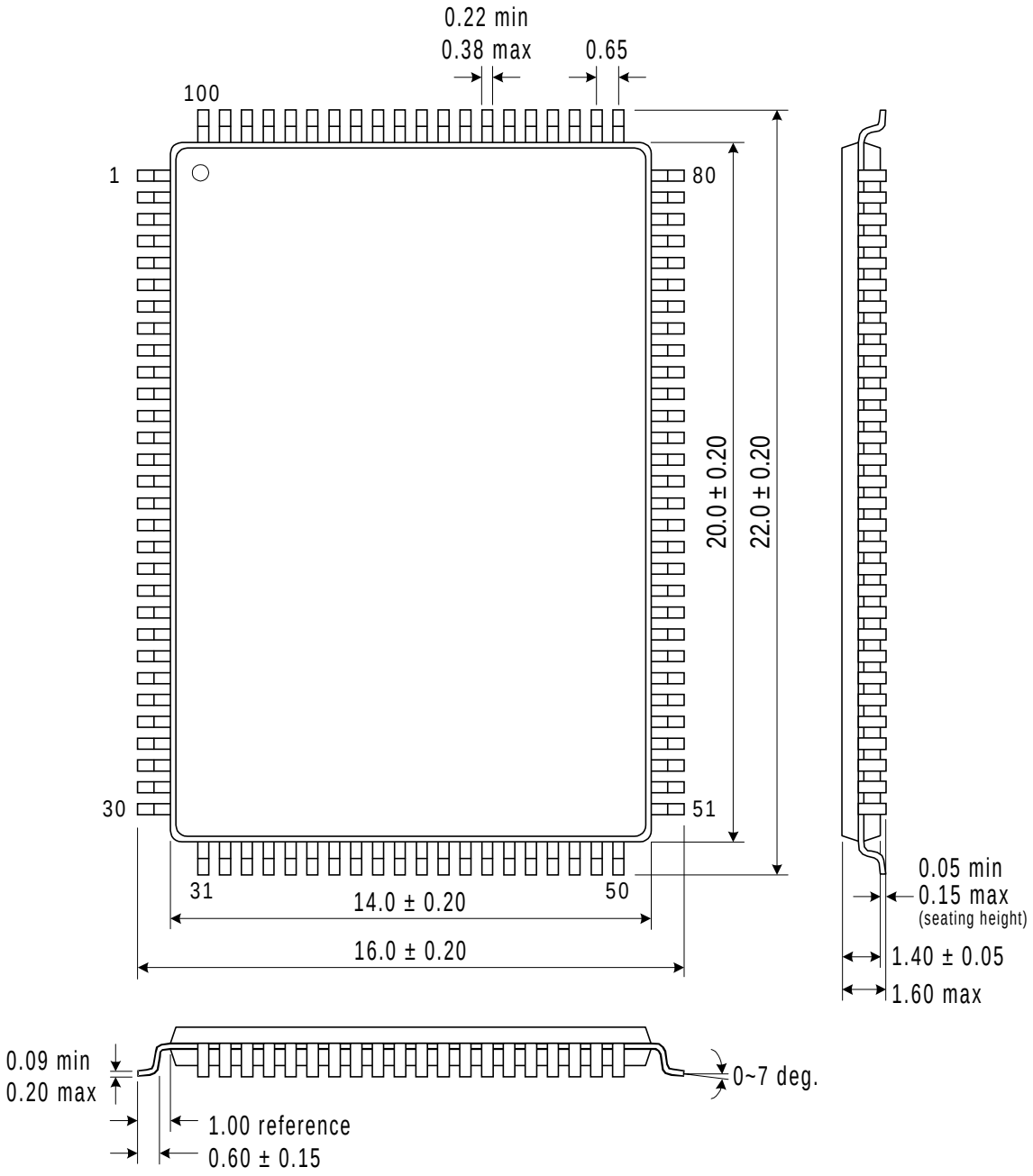
Self Refresh Entry / Exit



Note:
- The device will remain in the Self Refresh Mode while CKE=low.
- CS=high and the system clock must be stable prior to asserting the self refresh mode exit command.
- A minimum of tRC is required after CKE=high to complete the self refresh exit operation.

Package Information

100-Pin LQFP



Note: Dimensions are given in millimeters.