PORT BYPASS CIRCUIT FOR FIBRE CHANNEL AND GIGABIT ETHERNET S2057

FEATURES

- Supports ANSI X3T11 1.0625 Gbps FCAL disk attach
- ANSI x3T11 Fibre Channel Compatible
- IEEE 802.3z Gigabit Ethernet Compatible
- 1250 Mbps (Gigabit Ethernet) operation
- Fully differential for minimum deterministic jitter accumulation (10 ps nominal)
- TTL Bypass Select
- High speed LVPECL I/O
- 0.2 W Typical power dissipation
- 3.3 V power supply
- 20-pin TSSOP

GENERAL DESCRIPTION

The S2057 is a single channel Port Bypass Circuit (PBC), designed to minimize jitter accumulation by providing a high bandwidth fully differential data path. Primary application is in Fibre Channel Arbitrated Loop (FC-AL) disk arrays to allow hot swapping of FC-AL drives. The S2057 is designed to support 1.0625 Gbps and 1.25 Gbps data rates.

The S2057 is a high speed 2:1 multiplexer with 2 modes of operation: Normal and Bypass. A block diagram is shown in Figure 1, and a system diagram showing the S2057 in a single loop of a disk array is shown in Figure 2. A disk drive connects on the Disk Drive input and output ports (DDIP/N, DDOP/N), while the INP/N and OUTP/N ports connect to the upstream and downstream devices in the loop. Normal mode is enabled by setting the SEL pin ACTIVE, which includes the disk in the loop via the DDI/DDO ports. When the disk drive is either absent or non-functional, Bypass mode is selected by setting the SEL pin INACTIVE. This routes data directly from IN to OUT, bypassing the disk ports. Direct attach Fibre Channel Disk Drives have an “LRC Interlock” signal designed to directly control the select function. Table 1 is a truth table describing the data flow through the S2057.

Jitter Performance

The primary AC parameter of importance is deterministic jitter accumulation (data eye degradation) inserted by the port bypass circuit. The S2057 utilizes high bandwidth, low skew differential circuitry to provide symmetric rise and fall times and excellent noise immunity. This results in a nominal deterministic jitter accumulation of ±10 ps.

For arrays of disk drives greater than 4, it is recommended that the S2057 be cascaded with the S2058 (Port Bypass with repeater) in a ratio of 4:1 to perform clock and data retiming. This insures optimal jitter performance for the disk array system.

Table 1. Truth Table

SEL1	OUT	DDO
0	IN	IN
1	DDI	IN

Figure 1. S2057 Block Diagram

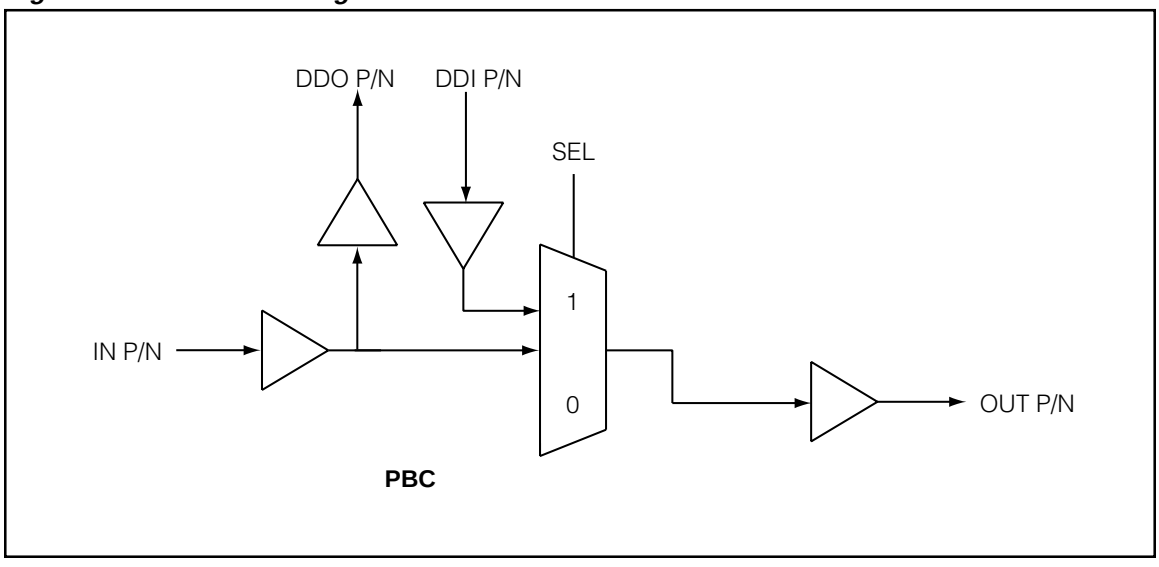


Figure 2. Functional Block Diagram

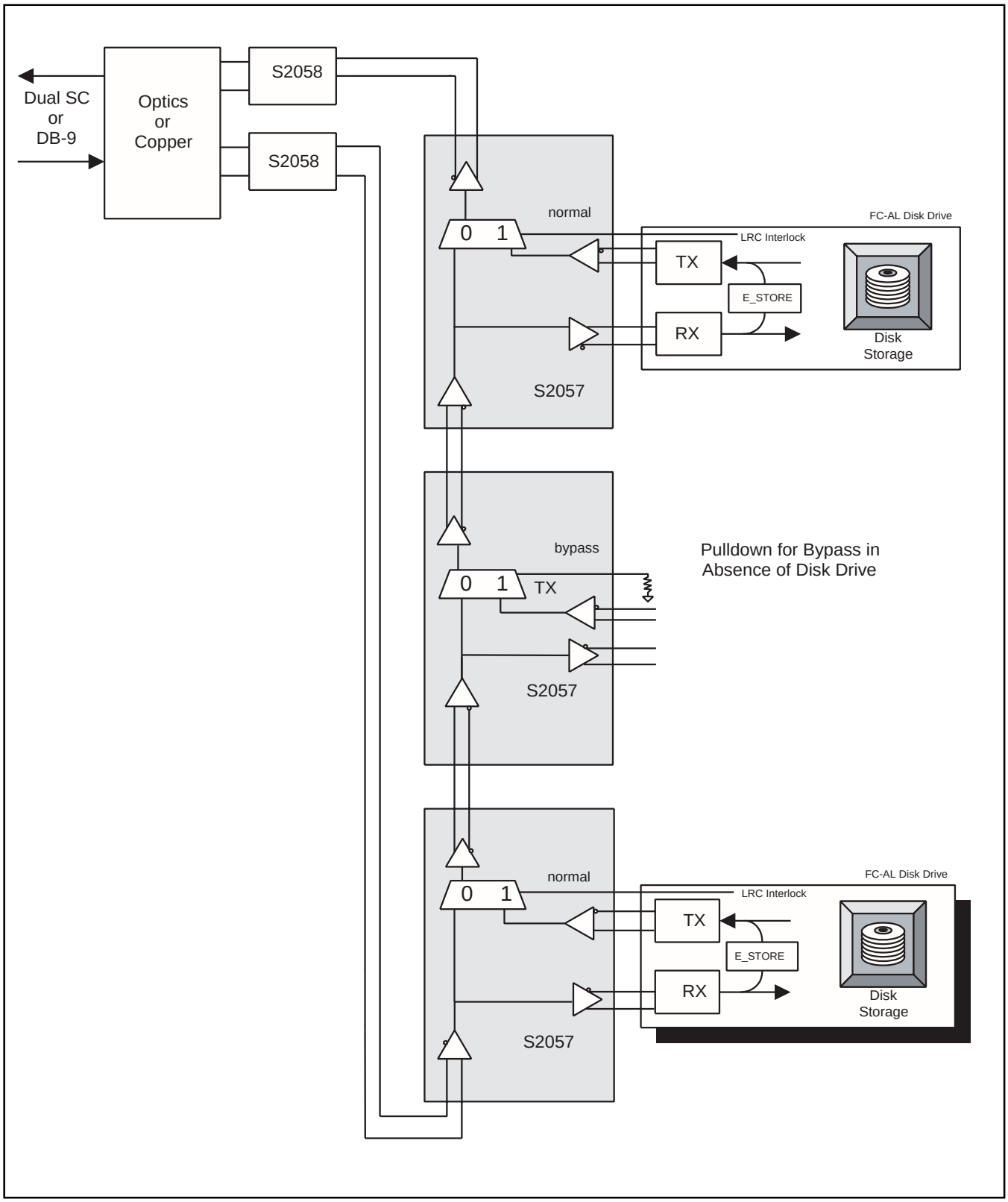


Figure 3. Timing Waveforms

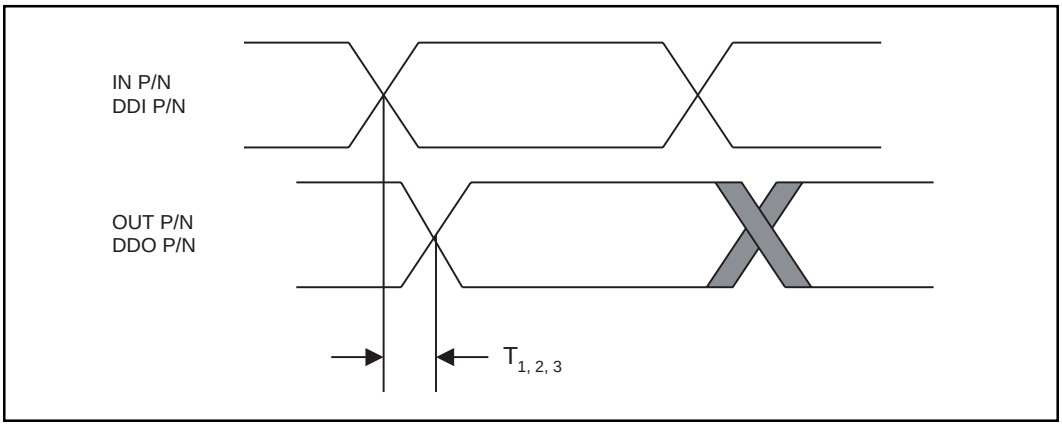


Figure 4. Differential Voltage

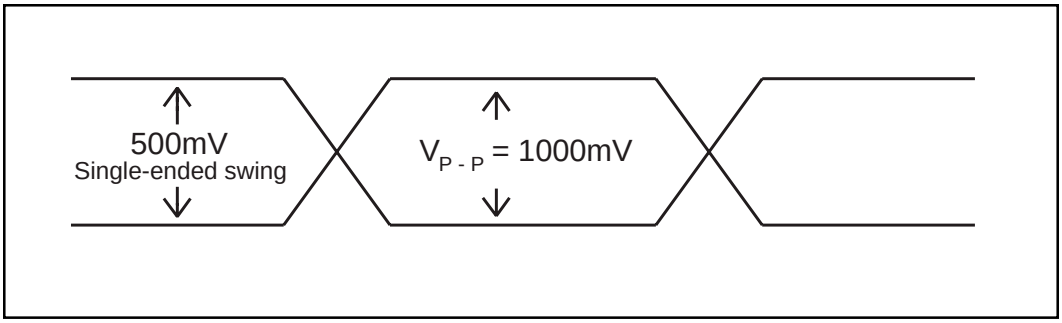


Figure 5. Input Termination

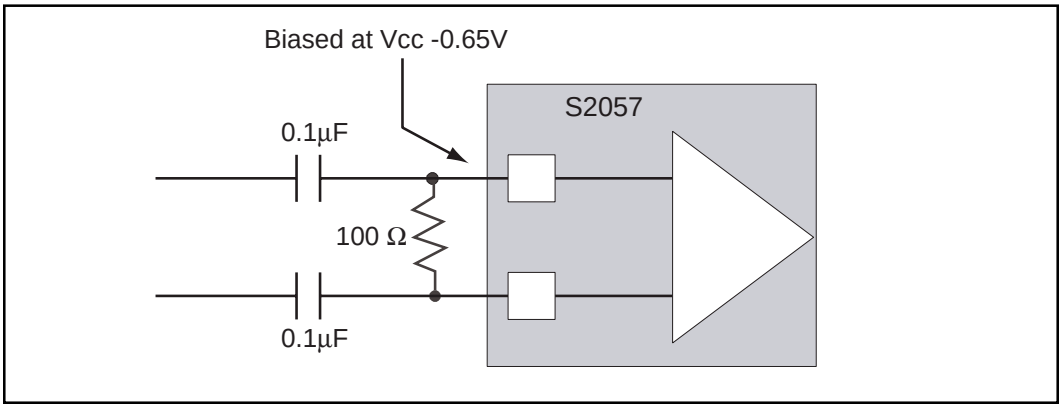


Figure 6. Output Connection

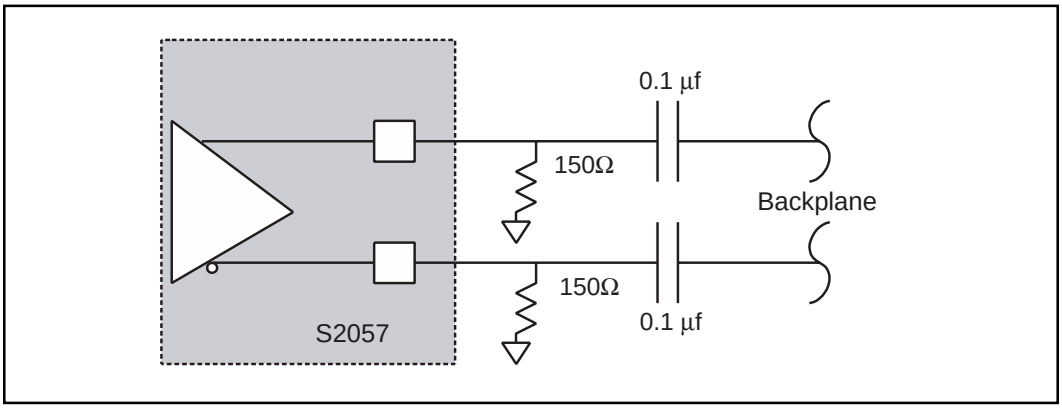


Table 2. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
INP INN	Diff. LVPECL	I	7, 6	Differential inputs from the downstream PBC port.
DDIP DDIN	Diff. LVPECL	I	4, 3	Disk Drive Input. Serial input from the local transmitter on PBC port 1.
SEL	TTL	I	11	A Low selects the "BYPASS" mode causing the output of the previous port to propagate to the next port or OUT. When High, this signal selects "NORMAL" mode which routes the previous port to the local output, DDO and routes the local input, DDI to the next port or OUT.
DDOP DDON	Diff. LVPECL	O	19, 18	Disk Drive Output. Serial output driving the local receiver corresponding to PBC port 1.
OUTP OUTN	Diff. LVPECL	O	15, 14	Serial output driving the upstream PBC port.
VCC	+3.3V		1, 2, 10, 12, 17, 20	Power Supply. 3.3V nominal.
GND	GND		5, 8, 9, 13, 16	Ground. Ground pins are phyisically attached to the die mounting surface, and are an important part of the thermal path. For best thermal performance, all ground pins should be connected to a ground plane, using multiple vias if possible.

Figure 7. S2057 Pinout Package

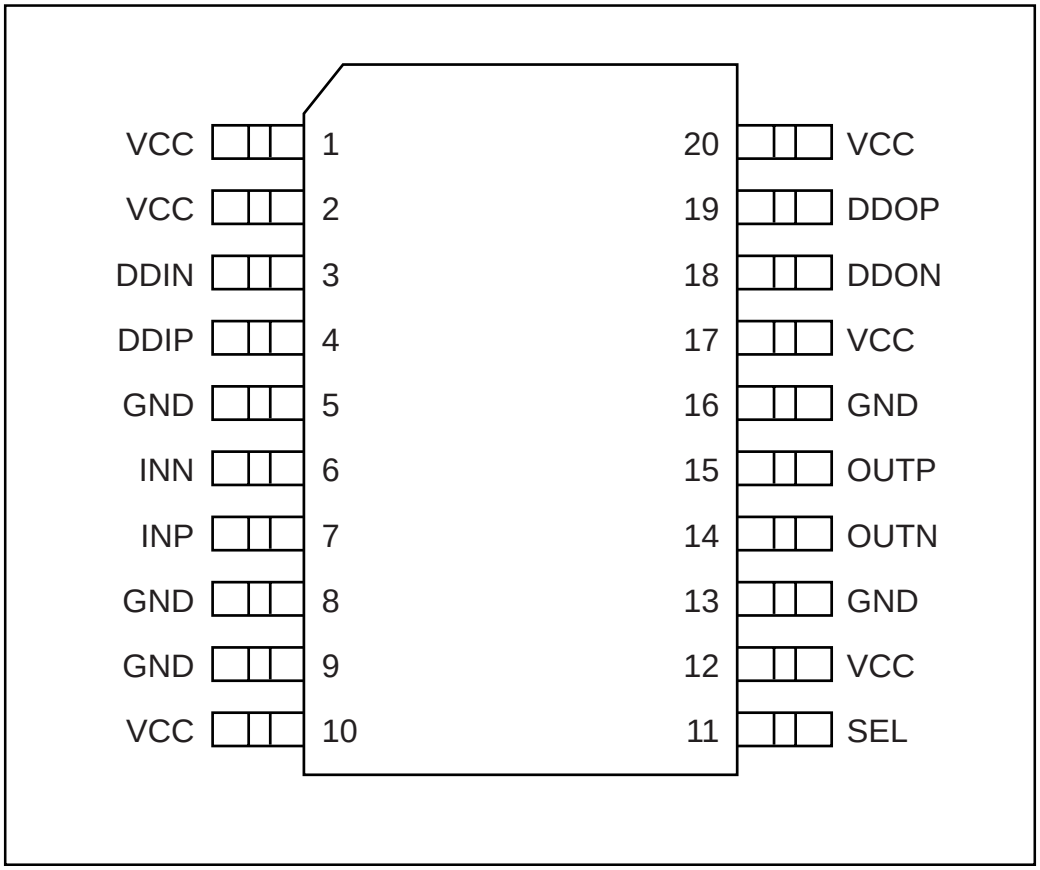
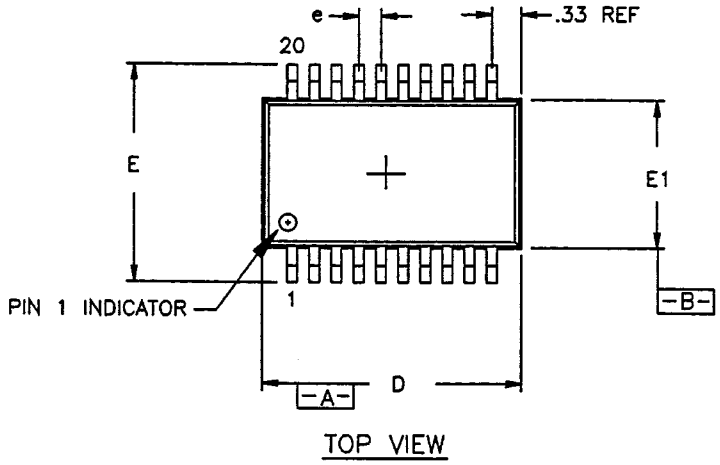
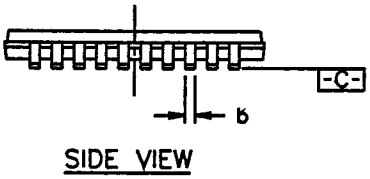
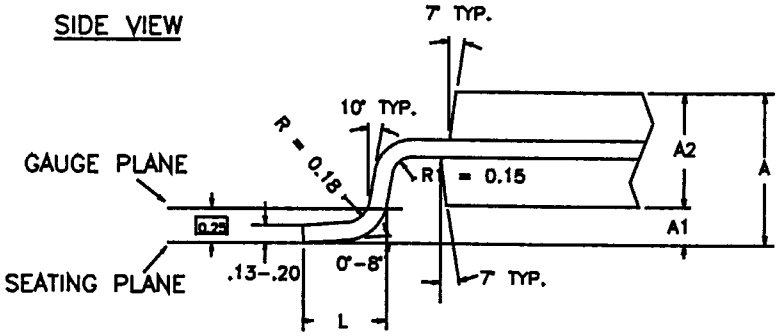


Figure 8. S2057 20 TSSOP (4.4 mm) Package







BODY SIZE PLUS LEADS / DIM LTR	TOL	2.0 MM FOOTPRINT 20
e	BASIC	0.65
b	±.05	0.22
A	MAX	1.20
A_1		.05 MIN/.10 MAX
A_2	NOM	0.90
D	±.05	6.50
E	±.10	6.40
E_1	±.10	4.40
L	±.15	0.60

Table 3. AC Characteristics *(Over recommended operating conditions.)*

Parameter	Description	Typ	Max	Units	Conditions
T_{RDDO} T_{FDDO}	Serial Data rise and fall time (Disk drive outputs, DDO).	185	350	ps	20% to 80% tested on a sample basis.
T1	Flow through propagation delay IN to OUT.	530	1000	ps	Delay with all circuits bypassed. 50 Ohm load.
T2	Flow through propagation delay IN to DDO.	580	1000	ps	Delay with PBC in Normal or Bypass mode. 50 Ohm load.
T3	Flow through propagation delay DDI to OUT.	560	1000	ps	Delay with PBC in Normal mode. 50 Ohm load.
T_{ROUT} T_{FOUT}	Serial data rise and fall time (Bypass output, OUT).	122	200	ps	20% to 80% tested on a sample basis.
$T_{jitterRMS}$	Random jitter accumulation	3	5	ps	RMS output jitter accumulated with K28.7 code from IN to OUT - PBC in bypass mode. Tested on a sample basis.
$T_{jitterDJ}$	Deterministic jitter accumulation	±10	±30	ps	Deterministic output jitter accumulated K28.5 code from IN to OUT, both PBC stages bypassed. 941 ps input pulse width. Tested on a sample basis.

Table 4. DC Characteristics *(Over recommended operating conditions.)*

Parameter	Description	Min	Typ	Max	Units	Conditions
$V_{IH(ITL)}$	Input HIGH voltage (SEL-TTL)	2.0		3.47	V	
$V_{IL(ITL)}$	Input LOW voltage (SEL-TTL)	0		0.8	V	
$I_{IH(ITL)}$	Input HIGH current (SEL-TTL)			50	µA	V_{IN} = 2.4V
$I_{IL(ITL)}$	Input LOW current (SEL-TTL)	-500			µA	V_{IN} = 0.5V
V_{CC}	Supply Voltage	3.13		3.47	V	V_{CC} = 3.30V ± 5%
I_{CC}	Supply Current		50	70	mA	Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation		0.18	0.25	W	Outputs open, V_{CC} = V_{CC} max
$\Delta V_{IN(DF)}$	Receiver differential peak-to-peak input sensitivity, INP/N & DDIP/N	300		2600	mV_{p-p} [1]	AC Coupled. Internally DC biased V_{CC} - 0.65V
$\Delta V_{OUTN(L\_SO)}$	DDOP/N output differential peak-to-peak voltage swing	1000	1400	2200	mV_{p-p} [1]	50Ω to V_{CC} -2.0V
$\Delta V_{OUTN(OUT)}$	OUTP/N output differential peak-to-peak voltage swing	1200	1300	2200	mV_{p-p} [1]	50Ω to V_{CC} -2.0V

Table 5. Absolute Maximum Ratings[1]

Parameter	Min	Typ	Max	Units
TTL Power Supply Voltage (V_{CC})	-0.5		+4	V
PECL DC Input Voltage (V_{INP})	-0.5		V_{CC}+0.5	V
TTL DC Input Voltage (V_{INP})	-0.5		3.47	V
DC Voltage applied to outputs for High output state ($V_{IN\ TTL}$)	-0.5		V_{CC}+0.5	V
TTL Output Current (I_{OUT}) (DC, output High)			50	mA
PECL Output Current (I_{OUT}), (DC output High)			50	mA
Case Temperature Under Bias (T_C)	-55		125	C°
Storage Temperature (T_{STG})	-65		150	C°
Maximum Input			1000	V

1. CAUTION: Stresses listed under “Absolute Maximum Ratings” may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 6. Recommended Operating Conditions [2]

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{CC})	+3.13		+3.47	V
Ambient Operating Temperature Range (T)	0		70	C°

2. AMCC guarantees the functional and parametric operation of the part under “Recommended Operating Conditions” (except where specifically noted in the AC and DC Parametric tables).

Ordering Information

Grade	Device	Package	Speed Grade
S – Commercial	2057	A – 20 TSSOP	*Note:* For Fibre Channel rates (1.062 Gbps), this part does not have a speed grade designation.

Grade	Device	Package	Speed Grade
S – Commercial	2057	A – 20 TSSOP	12 – 1.25 Gbps (Gigabit Ethernet)

X	–	XXXX	X	–	XX
Grade		Part Number	Package		Speed Grade

ISO 9001 CERTIFIED

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