

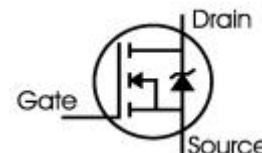
Fast CoolMOS™ Power Transistor

FEATURES:

- New revolutionary high voltage technology
- Ultra low gate charge
- Worlbest $R_{DS(on)}$ per chip area
- Ultra low effective capacitances
- Improved noise immunity

Applications:

- SMPS, resonant applications



Chip Type	V_{DS}	I_D	Die Size	Package	Ordering Code
SIPC02N60S5	600V	1A	1.42 x 1.42 mm ²	sawn on foil	Q67050-A4091-A001

MECHANICAL PARAMETER:

Raster size	1.42 x 1.42	mm
Source pad size	0.68 x 1.26	
Gate pad size	0.47 x 0.53	
Area total / active	2.016 / 0.65	mm ²
Thickness	175	μm
Wafer size	150	mm
Flat position	0	grd
Max.possible chips per wafer	7622	
Passivation frontside	Nitride	
Emitter metallization	3200 nm Al Si 1%	
Collector metallization	1400 nm Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	electrically conductive glue or solder	
Wire bond (proposed)	Source: Al, ≤ 500μm; Gate: Al, ≤ 125μm	
Reject Ink Dot Size	Ø 0.30mm	
Recommended Storage Environment	store in original container, in dry nitrogen, < 6 month	

MAXIMUM RATINGS:

Parameter	Symbol	Value	Unit
Drain-Source voltage	V_{DS}	600	V
DC drain current, limited by T_{jmax}	I_D	1	A
Pulsed drain current, t_p limited by T_{jmax}	I_{Dpuls}	2	A
Gate source voltage	V_{GS}	± 20	V
Operating junction and storage temperature	T_j, T_{stg}	-55 ... +150	°C
Reverse diode dv/dt $I_D=1A, V_{DS} \leq V_{DSS}, di/dt=100 A/\mu s, T_{jmax}=150^\circ C$	dv/dt	6	KV/ μs

STATIC CHARACTERISTICS (tested on chip), $T_j=25^\circ C$, unless otherwise specified:

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D = 0.25mA$			600	V
Gate-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=0.5A$		6	$6.2^{1)}$	Ω
Gate threshold voltage	$V_{GS(th)}$	$I_D=29\mu A, V_{GS}=V_{DS}$	2.05	3.0	3.95	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=600V, V_{GS}=0V$		0.1	25	μA
Gate-source leakage current	I_{GSS}	$V_{DS}=0V, V_{GS}=20V$			100	nA

¹⁾ this correlates to a max. $R_{DS(on)}$ -value of 6 Ω at $V_{GS}=10V, I_D=0.5A$ of this chip packaged in a TO220-package

ELECTRICAL CHARACTERISTICS (tested at component):

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	$V_{DS}=25V,$	-	100	-	pF
Output capacitance	C_{oss}	$V_{GS}=0V,$	-	40	-	
Reverse transfer capacitance	C_{rss}	$f=1MHz$	-	2.5	-	

SWITCHING CHARACTERISTICS (tested at component), Inductive Load

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	$T_j=25^\circ C$	-	30	-	ns
Rise time	t_r	$V_{DD}=350V,$	-	25	-	
Turn-off delay time	$t_{d(off)}$	$I_D=0.8 A,$	-	55	-	
Fall time	t_f	$V_{GS}=10V,$	-	30	-	
		$R_G= 100\Omega$				

CHIP DRAWING:

LEGENDE

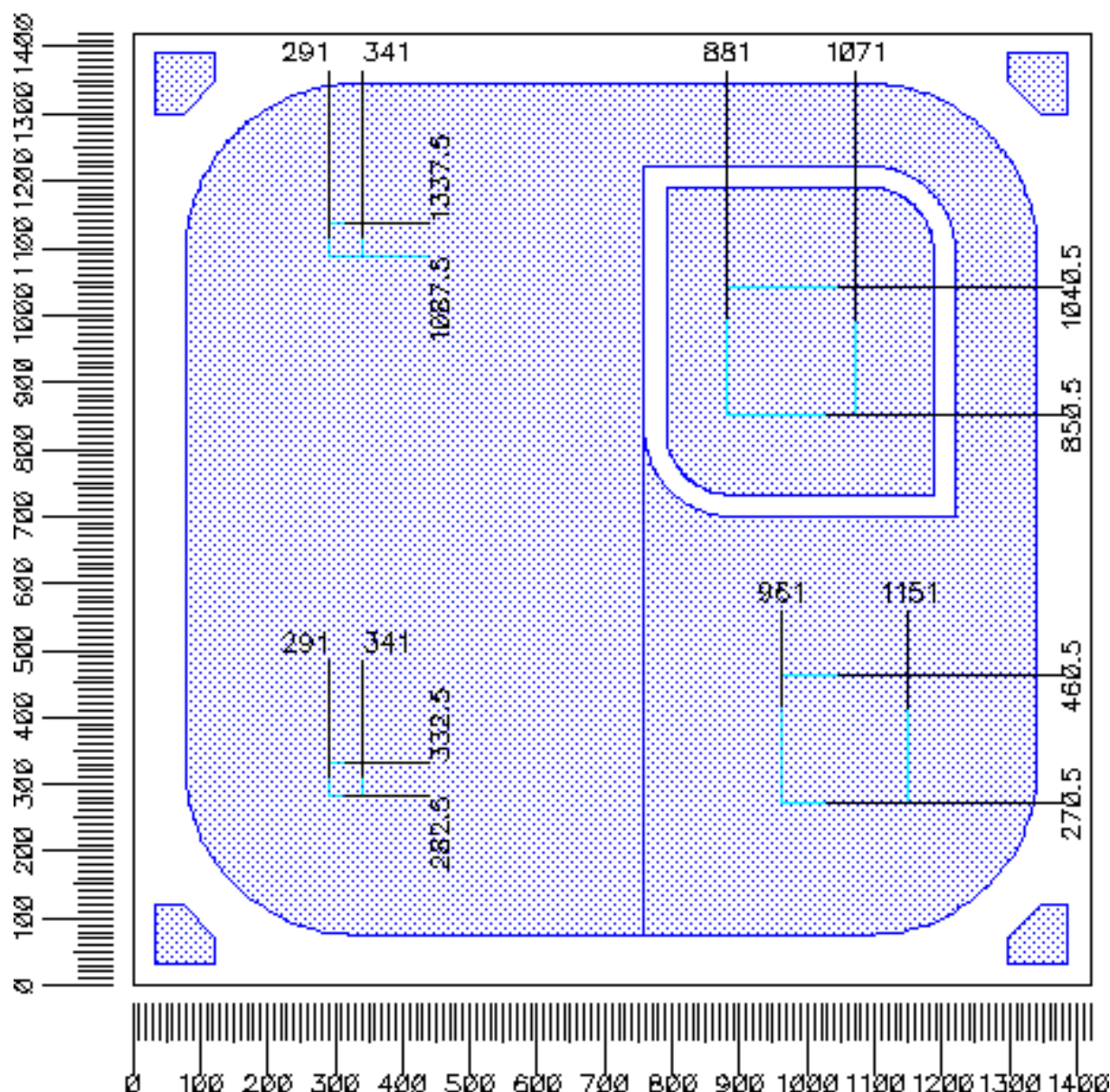
Layer Mask Technology

	8	F	Alu[metal1]
	18	S	Imide

Design: L545A11

Die-Size: 1.420 x 1.420 um

Flat-Side





Preliminary

SIPC02N60S5

FURTHER ELECTRICAL CHARACTERISTICS:

This chip data sheet refers to the device data sheet		
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DESCRIPTION:

AQL 0,65 for visual inspection according to failure catalog
Electrostatic Discharge Sensitive Device according to MIL-STD 883
Test-Normen Villach/Prüffeld

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