"CROSSBOW" 32 X 32 800 MBIT/S CROSSPOINT SWITCH S2024

FEATURES

- Full broadcast switching capability
- 32 x 32 crosspoint structure, expandable to 64 x 64 with no external components
- ECL 10K data path and TTL I/O for configuration control provide high speed with easy interfacing to slower-speed circuitry
- Up to 800 Mbit/s NRZ data rate in transparent mode, 400-Mbit/s operation in synchronous mode
- 196-pin LDCC package
- Reconfigurable without disturbing operation
- Differential or single-ended clocking

APPLICATIONS

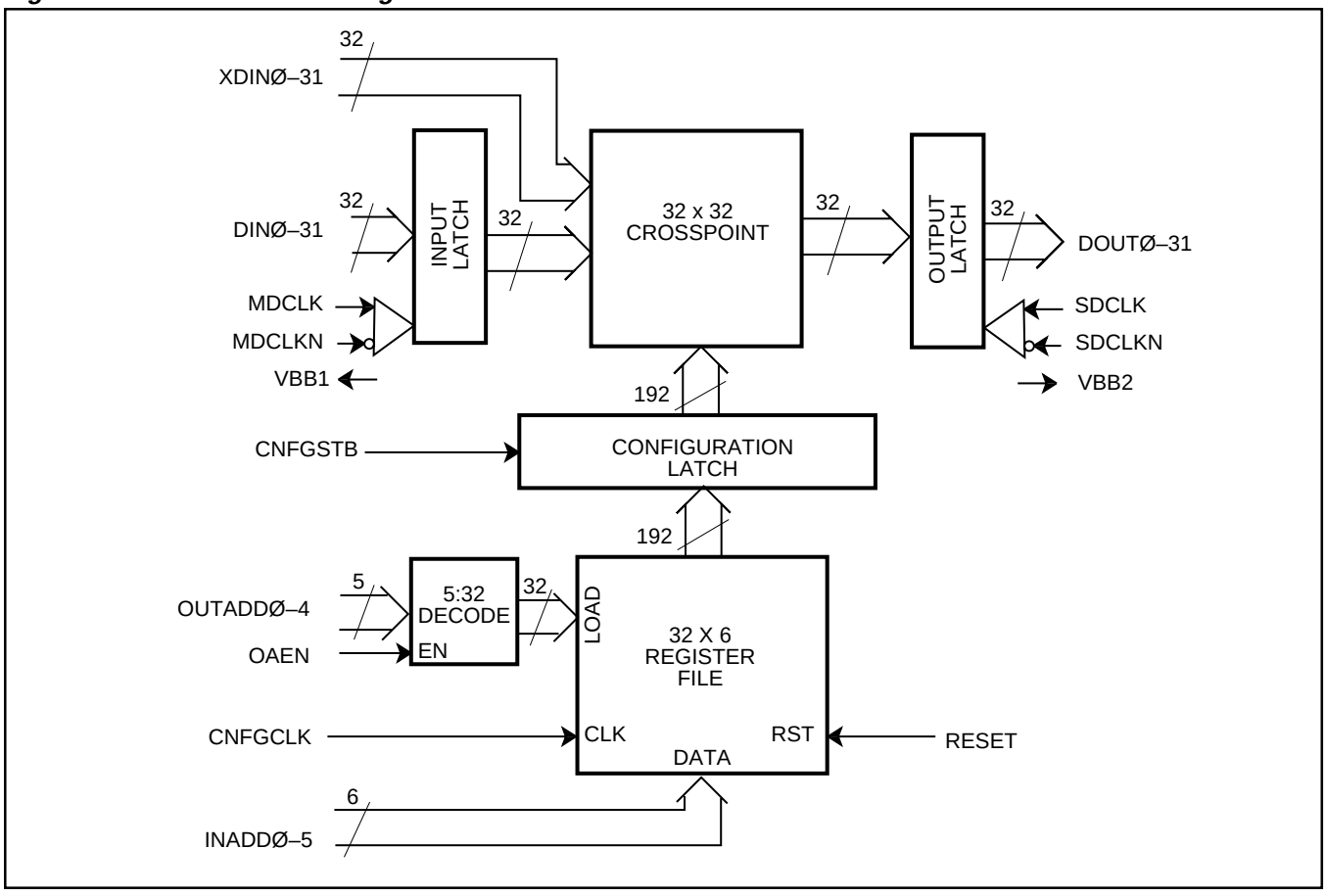
- Internet switches
- Digital video
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Datacom or telecom switching

GENERAL DESCRIPTION

The S2024 "Crossbow" is a high-speed 32 x 32 crosspoint switch with full broadcast capability—any of its 32 inputs can be connected independently to any or all of its 32 outputs. In addition, the S2024 can be expanded, through use of its expansion data inputs (XDIN0–XDIN31), to a 64 x 64 crosspoint switch with no external components. Further expansion is possible with external addressing logic.

Two operating modes—synchronous (400 Mbit/s) and transparent (800 Mbit/s)—provide maximum flexibility across a range of applications. The 10K ECL logic data path makes the part ideal for high-speed applications, while the S2024's TTL addressing and control simplify interfacing to slower-speed circuitry. The switch can be completely reconfigured in only 4 ns without disturbing switch operations.

Figure 1. Functional Block Diagram



OPERATING MODES

SYNCHRONOUS MODE

In synchronous mode, two clock signals, MDCLK for data input and SDCLK for data output, provide the latch enable strobes to allow the input data and output data to be stored in 32-bit latches. The S2024 is capable of 400-Mbit/s operation in this mode. The data is latched on the falling edge of SDCLK and MDCLK.

Inputs MDCLK/MDCLKN and SDCLK/SDCLKN can be used as true differentials or as single-ended clocking signals. Onboard voltage reference outputs VBB1 and VBB2 allow single-ended clocking capability when configured as shown in Figure 8.

TRANSPARENT MODE

In transparent, or asynchronous, mode, any data appearing at the input will be passed immediately through to its designated output. Transparent transfer of data through the latches takes place when both MDCLK and SDCLK clock inputs are held high. In this mode the S2024 is capable of up to a 800 Mbit/s NRZ data rate.

RECONFIGURATION MODE

The S2024 can be selectively reconfigured one output at a time, or any number of outputs can be reconfigured simultaneously. Configuration data is stored in 32 registers, one register for each output data pin. The 6-bit content of each register selects the input data pin which is to be connected to that output data pin. To connect an output to a given input, the output to reconfigure is selected using OUTADD0–4 and OAEN to enable the appropriate output configuration register. With the output configuration register selected, the desired input pin connection is provided on INADD0–5. The input pin selection on INADD0–5 will be stored into the selected output configuration register on the rising edge of CNFGCLK.

When the switch is to be reconfigured, the S2024 minimizes the time required through the use of an additional configuration latch. While the switch is operational (and prior to the time at which it must be reconfigured) a new set of input addresses can be loaded into the register file. When all registers have been updated, the contents of the registers are parallel-transferred to the configuration latch, when CNFGSTB goes high. This process allows a switch reconfiguration in just 4 ns.

Figure 2. Synchronous Mode

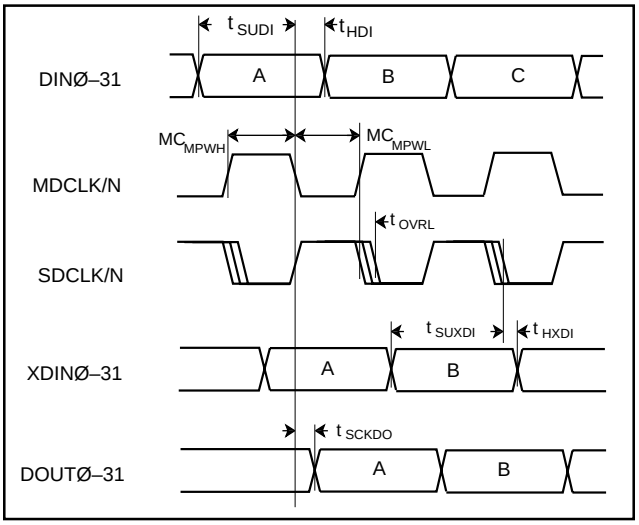


Figure 3. Transparent Mode

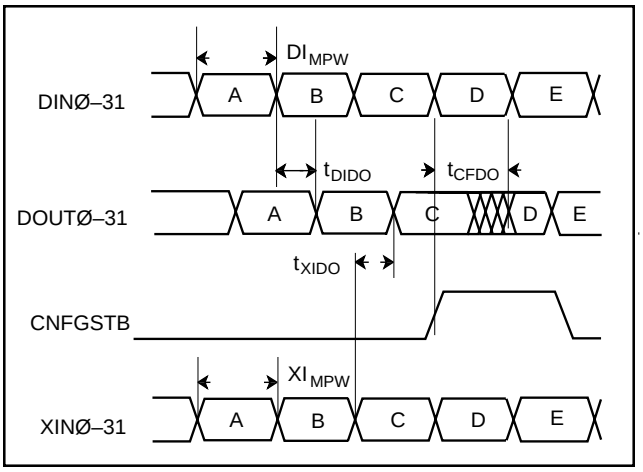


Figure 4. Reconfiguration Mode

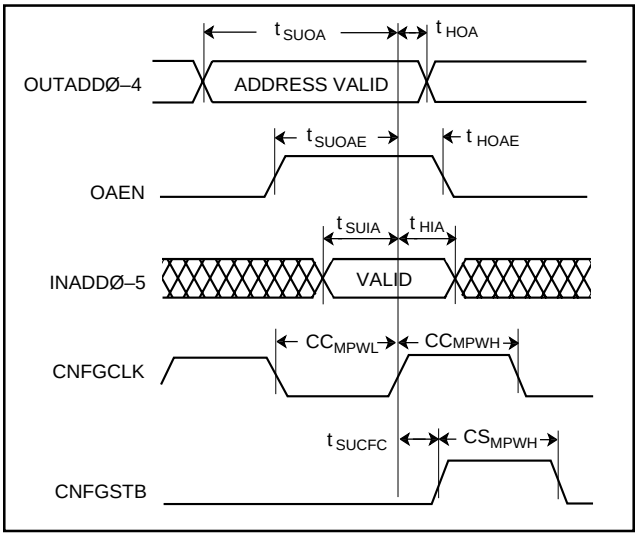


Table 1. Synchronous Mode Timing

Symbol	Description	S2024B-8		S2024B-6		
		Min	Max	Min	Max	Units
t_{SUDI}	Setup time of DIN0–31 before falling edge of MDCLK/N	1160		980		ps
t_{HDI}	Hold time of DIN0–31 after falling edge of MDCLK/N	1220		770		ps
t_{OVRL}	Overlap when MDCLK/N and SDCLK/N are high		1860		1760	ps
t_{SUXDI}	Setup time of XDIN0–31 before falling edge of SDCLK/N	1160		1040		ps
t_{HXDI}	Hold time of DIN0–31 after falling edge of SDCLK/N	1400		680		ps
t_{SCKDO}	Propagation delay from rising edge of SDCLK/N to DOUT0–31		3400		2770	ps
MC_{MPWH}	Pulse width high of MDCLK/N or SDCLK/N	630		790		ps
MC_{MPWL}	Pulse width low of MDCLK/N or SDCLK/N	500		660		ps
F_{MAX}	Data Rate		400		300	Mbit/s

Table 2. Transparent Mode Timing

Symbol	Description	S2024B-8		S2024B-6		
		Min	Max	Min	Max	Units
t_{DIDO}	Propagation delay from DIN0–31 to DOUT0–31		4180		5125	ps
t_{XIDO}	Propagation delay from XIN0–31 to DOUT0–31		3040		3400	ps
t_{CFDO}	Propagation delay from rising edge of CNFGSTB to DOUT0–31 valid		3760		4150	ps
DI_{MPW}	Pulse width high of DIN0–31	860		1030		ps
XI_{MPW}	Pulse width high of XDIN0–31	910		1090		ps
F_{MAX}	Data Rate		800		600	Mbit/s

Table 3. Reconfiguration Timing (S2024B-8, S2024B-6)

Symbol	Description	Min	Max	Units
t_{SUOA}	Setup time of OUTADD0–4 before rising edge of CNFGCLK	4360		ps
t_{HOA}	Hold time of OUTADD0–4 after rising edge of CNFGCLK	560		ps
t_{SUOAE}	Setup time of OAEN before rising edge of CNFGCLK	3860		ps
t_{HOAE}	Hold time of OAEN before rising edge of CNFGCLK	–140		ps
t_{SUIA}	Setup time of INADD0–5 before rising edge of CNFGCLK	2660		ps
t_{HIA}	Hold time of INADD0–5 before rising edge of CNFGCLK	980		ps
t_{SUCFC}	Setup time of CNFGCLK to CNFGSTB so that the rising edge of CNFGSTB will start reconfiguration	760		ps
t_{SUCFG}	Setup time of CNFGSTB falling edge before the rising edge of CNFGCLK	1960		
CC_{MPWL}	Pulse width low of CNFGCLK	4200		ps
CC_{MPWH}	Pulse width high of CNFGCLK	4200		ps
CS_{MPWH}	Pulse width low of CNFGSTB	4200		ps

Table 4. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DIN31 DIN30 DIN29 DIN28 DIN27 DIN26 DIN25 DIN24 DIN23 DIN22 DIN21 DIN20 DIN19 DIN18 DIN17 DIN16 DIN15 DIN14 DIN13 DIN12 DIN11 DIN10 DIN9 DIN8 DIN7 DIN6 DIN5 DIN4 DIN3 DIN2 DIN1 DIN0	ECL	I	181 180 179 177 176 175 174 169 167 166 164 161 160 159 157 156 155 154 153 152 150 145 143 142 141 140 139 137 136 134 135 131	Intput data. Active High.
OUTADD4 OUTADD3 OUTADD2 OUTADD1 OUTADD0	TTL	I	13 5 3 2 1	Output configuration register address. Used to select the output configuration registers in the register file.
INADD5 INADD4 INADD3 INADD2 INADD1 INADD0	TTL	I	21 20 19 18 15 14	Input data addresses. Used to select the input data pin connected to each output data pin. Stored into register file by CNFGCLK. INADD5=1 is used to select the expansion data inputs.
OAEN	TTL	I	190	Output address enable. When high, enables the selection of appropriate output configuration register.
MDCLK MDCLKN	ECL	I	66 65	Master latch clock inputs (input data). True differential inputs. Can be used single-ended with VBB1 and VBB2.

Table 4. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
XDIN31 XDIN30 XDIN29 XDIN28 XDIN27 XDIN26 XDIN25 XDIN24 XDIN23 XDIN22 XDIN21 XDIN20 XDIN19 XDIN18 XDIN17 XDIN16 XDIN15 XDIN14 XDIN13 XDIN12 XDIN11 XDIN10 XDIN9 XDIN8 XDIN7 XDIN6 XDIN5 XDIN4 XDIN3 XDIN2 XDIN1 XDIN0	ECL	I	183 184 185 192 194 8 11 12 27 29 33 36 37 38 39 41 42 43 44 45 47 48 49 52 54 55 56 57 58 59 62 61	Expansion input data. Active High. These inputs are selected by the most significant bit of the output configuration registers.
SDCLK SDCLKN	ECL	I	70 69	Slave latch clock inputs (output data). True differential inputs. Can be used single-ended with VBB1 and VBB2.
CNFGCLK	TTL	I	188	Address configuration clock. On rising edge, stores data into output configuration register.
RESET	TTL	I	191	Chip reset. Active High. Asynchronously resets the register file.
CNFGSTB	TTL	I	189	Reconfiguration enable input. The contents of the register file are parallel-loaded into the configuration latch when CNFGSTB goes high, causing switch reconfiguration.
VBB1 VBB2	–	O	64 72	Reference threshold voltage outputs to allow provision for single-ended capability for clock inputs.

Table 4. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DOUT31 DOUT30 DOUT29 DOUT28 DOUT27 DOUT26 DOUT25 DOUT24 DOUT23 DOUT22 DOUT21 DOUT20 DOUT19 DOUT18 DOUT17 DOUT16 DOUT15 DOUT14 DOUT13 DOUT12 DOUT11 DOUT10 DOUT9 DOUT8 DOUT7 DOUT6 DOUT5 DOUT4 DOUT3 DOUT2 DOUT1 DOUT0	ECL	O	130 129 127 125 121 119 117 116 115 111 110 107 106 105 104 103 100 99 96 94 93 92 91 90 89 87 86 85 83 80 79 78	Output data. Active High.
ACTEST	–	O	6, 31	Used during device testing to determine AC performance of chip. Signal is the output of a 9-stage ring oscillator followed by two divide-by-2 circuits. Minimum acceptable output frequency is 32.6 MHz.
THDIODE	–	–	146, 147	Thermal diode connections
EGND	GND	–	7, 30, 32, 68, 77, 101, 109, 112, 187	ECL I/O Power Supply
+5V	+5V	–	50, 98, 148, 196	TTL I/O Power supply

Table 4. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
– 5.2V	– 5.2V	–	17, 24, 25, 26, 35, 63, 73, 75, 76, 84, 113, 122, 123, 124, 133, 162, 170, 171, 173, 182	Core Power Supply
GND	GND	–	4, 10, 16, 22, 28, 34, 40, 46, 51, 53, 60, 67, 71, 74, 81, 88, 95, 97, 102, 108, 114, 120, 126, 132, 138, 144, 149, 151, 158, 165, 168, 172, 178, 186, 193, 195	Ground
NC	–	–	9, 23, 82, 118, 128, 163	No Connection

Figure 5. S2024 Pinout

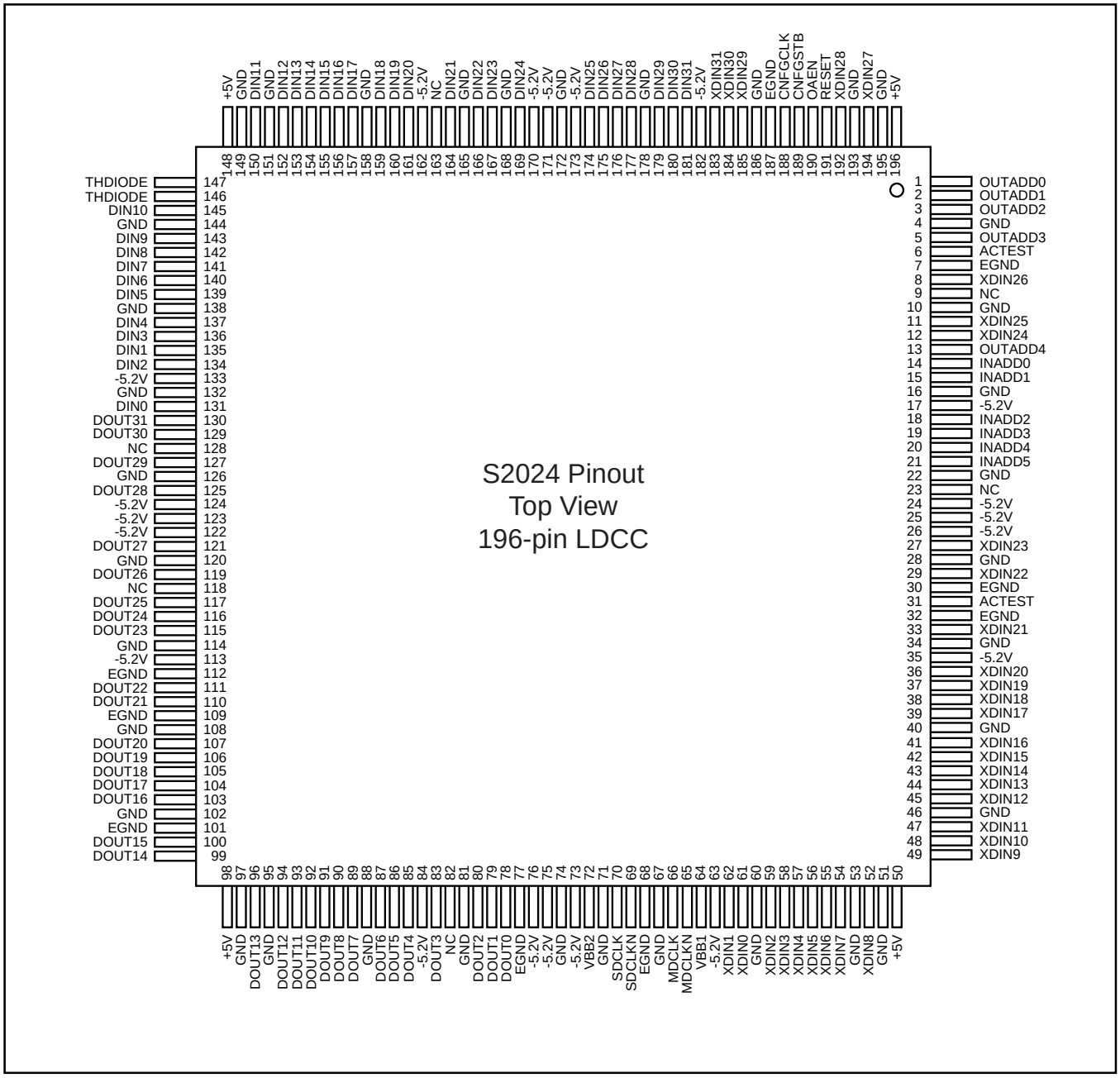
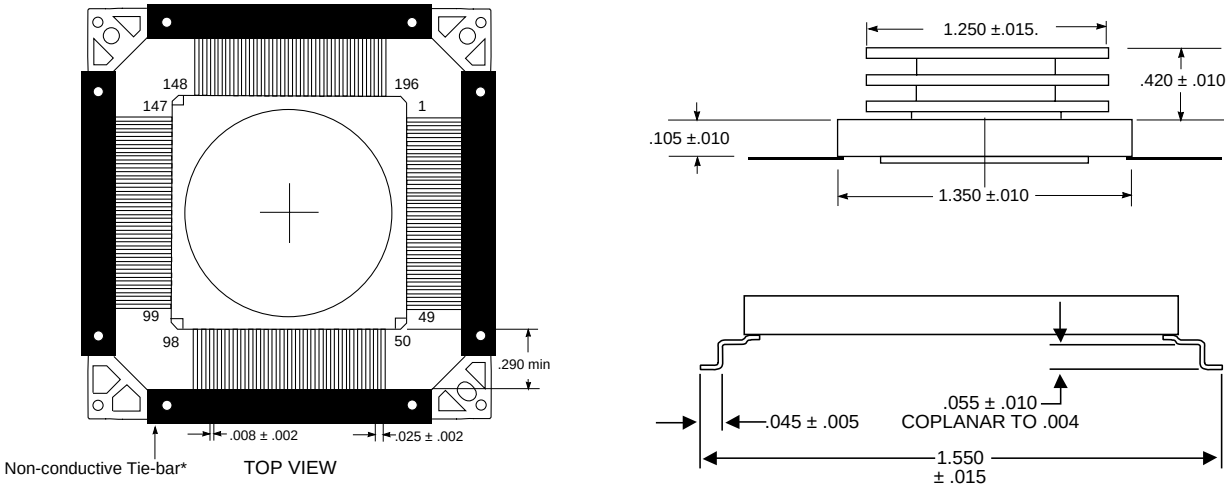


Figure 6. 196 LDCC Package



All dimensions nominal in inches.
*Trim non-conductive tie-bar prior to board attachment.

Table 5. Thermal Management

Symbol	Description	Airflow	Value	Units
Θjc	Thermal resistance from junction to case		2.3	°C/W
Θjc	Thermal resistance from junction to ambient	Still air	25.6	°C/W
Θjc	Thermal resistance from junction to ambient with heatsink	400 LFPM	4.8	°C/W

Note: S2024 requires an AMCC heatsink 45-10 with an airflow of 400 LFPM for operation over commercial temperatures.

Figure 7. AMCC Heatsink 45-10

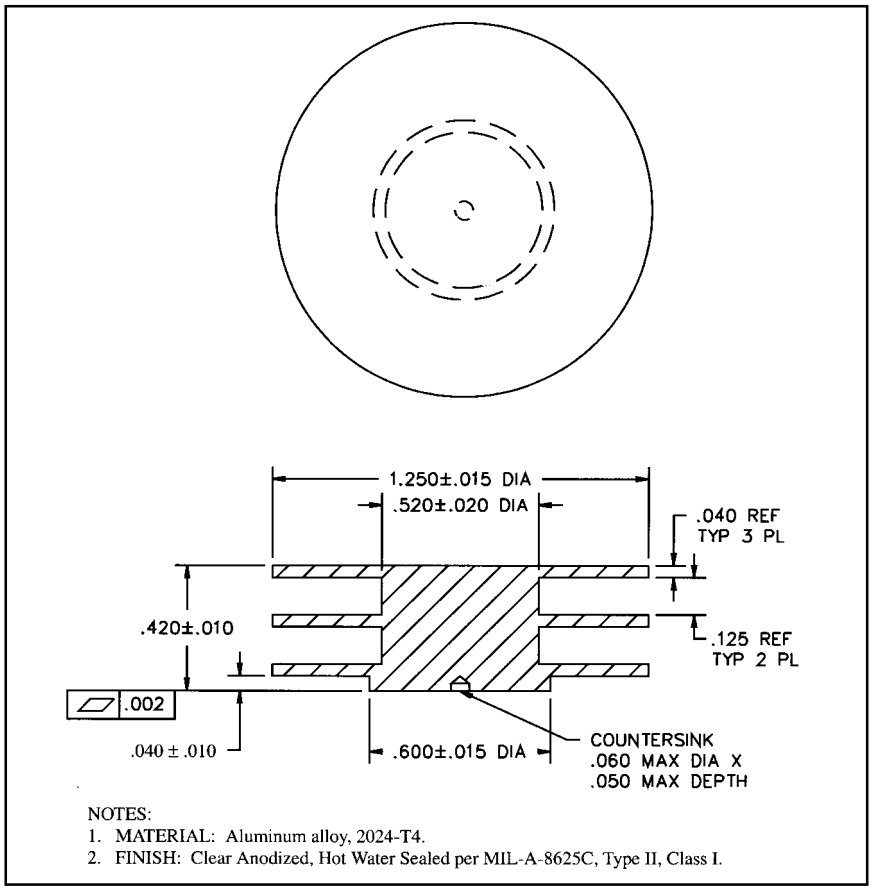


Figure 8. Differential to Single-Ended Conversion

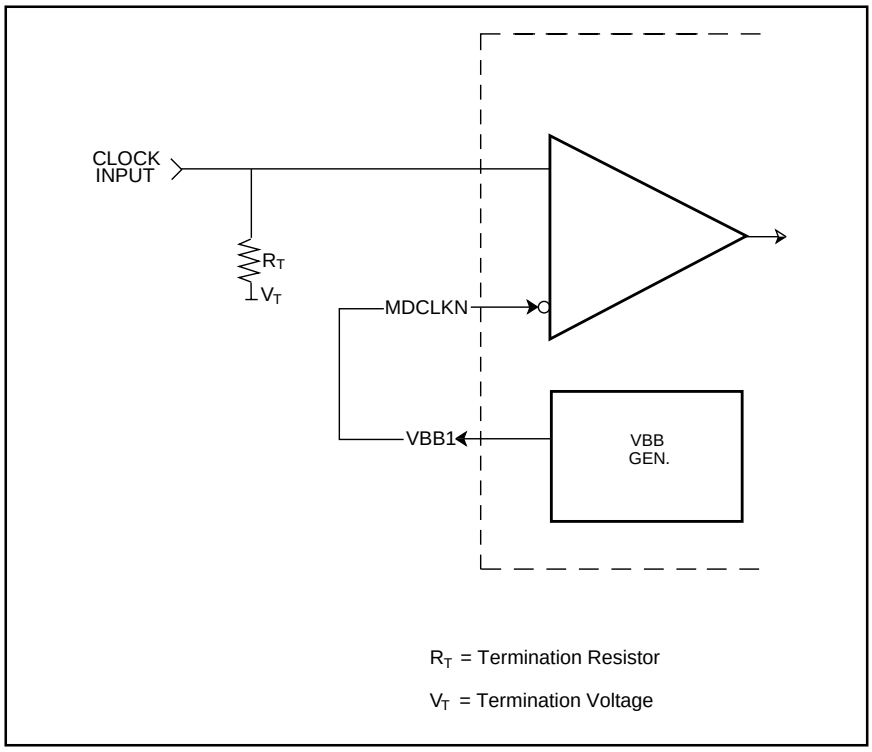


Table 6. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
ECL Supply Voltage VEE (VCC = 0)			–8.0	V/DC
ECL Input Voltage (VCC = 0)	GND		–3.0	V
ECL Output Source Current (continuous)			–50	mA/DC
TTL Supply Voltage VCC (VEE = 0)			7.0	V
TTL Input Voltage (VEE = 0)			5.5	V
Operating Temperature	–55 (ambient)		+125 (case)	°C
Operating Junction Temperature			+150	°C
Storage Temperature	–65		+150	°C

Table 7. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
ECL (10K) Supply Voltage (VEE) V_{CC} = 0	–4.94	–5.2	–5.46	V
ECL Input Signal Rise/Fall Time		1.0	3.0	ns
TTL Supply Voltage V_{CC}	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)		70 (ambient)	°C
Junction Temperature			130	°C
I_{CC}			194	mA
I_{EE}			1589	mA
P_{OEF}			0.58	W

Table 8. ECL 10K Input/Output DC Characteristics V_{EE} = –5.2 V[1]

	$T_{ambient}$			
	0 °C	25 °C	70 °C	**Units**
V_{OHmax}	–770	–730	–650	mV
V_{IHmax}[3]	–720	–680	–600	mV
V_{OHmin}	–1000	–980	–920	mV
V_{IHmin}[3]	–1145	–1105	–1045	mV
V_{ILmax}[3]	–1490	–1475	–1450	mV
V_{OLmax}	–1625	–1620	–1585	mV
V_{OLmin}	–1980	–1980	–1980	mV
V_{ILmin}[3]	–2000	–2000	–2000	mV
IIH^2MAX	30	30	30	µA
IIH^2MAX	–.5	–.5	–.5	µA

Table 9. TTL Input/Output DC Characteristics

Symbol	**Parameter**	**Test DC Conditions**	**COMM 0° /+70° C**			**Units**
			Min	**Typ [2]**	**Max**	
V_{IH}[3]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V_{IL}[3]	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = –18mA		–0.8	–1.2	V
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V			50	µA
I_I	Input HIGH current at MAX	V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
I_{IL}	Input LOW current	V_{CC} = Max, v_{IN} = 0.5V			–0.4	mA

Notes

1. Data measured with V_{EE} = –5.2 ± .1V assuming a +50°C rise between ambient (T_a) and junction temperature (T_j) for 0°C, +25°C, and +70°C. These conditions will be met with an airflow of 400 for commercial environment.
2. Typical limits are at 25°C, V_{CC} = 5.0V.

3a. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

3b. Use extreme care in defining input levels for dynamic testing. Many ouputs may be charged at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for dynamic TTL testing and V_{ILMIN} and V_{IHMAX} for ECL testing.

EXPANDING THE S2024 TO A 64 X 64 CROSSPOINT SWITCH

Four S2024s can be easily connected to form a 64 x 64 crosspoint switch. In order to accomplish this, the switches must be configured so that any input can be multiplexed to any output. The accompanying figure provides an example of a 64 x 64 switch, making use of the S2024's expansion data inputs.

This arrangement allows all outputs to select input data from any bit of the 64-bit data bus. The two secondary S2024s receive data from the two primaries by means of the expansion data inputs. The expansion inputs are used when the switching operation has been realized by the previous switches and only a flow through is needed.

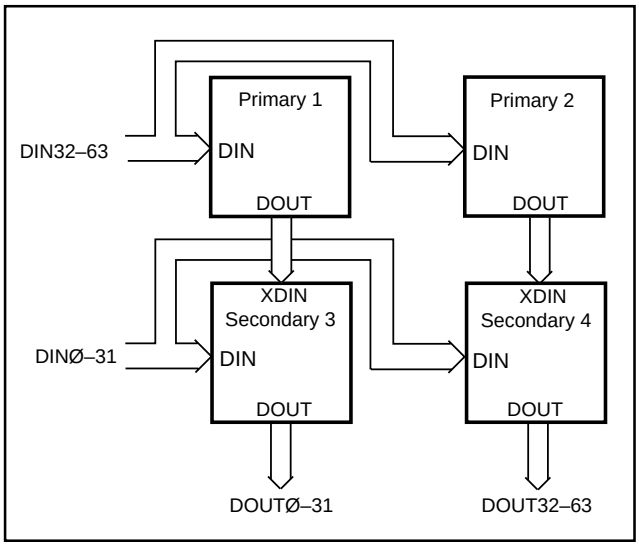
Crosspoint 1 switches D32–D63 to Crosspoint 3.

Crosspoint 2 switches D32–D63 to Crosspoint 4.

Crosspoint 3 switches D0–D31 to O0–O31 and/or reproduces the outputs of Crosspoint 1 through the expansion inputs.

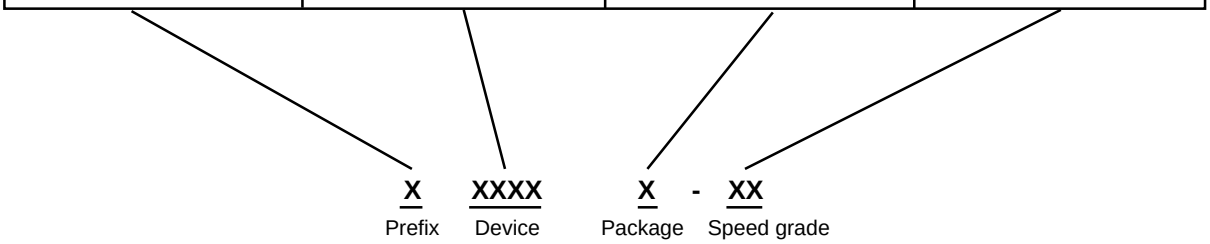
Crosspoint 4 switches D0–D31 to O32–O63 and/or reproduces the outputs of Crosspoint 2 through the expansion inputs.

Figure 9. S2024 Expansion Diagram



Ordering Information

PREFIX	DEVICE	PACKAGE	SPEED GRADE
S – Integrated Circuit	2024	B – 196 LDCC with straight leads C – 196 LDCC leadformed with heatsink unattached	6 – 600 Mbit/s 8 – 800 Mbit/s



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