16 x 16 1.5 GBIT/S DIFFERENTIAL CROSSPOINT SWITCH S2016

FEATURES

- 16 x 16 differential crosspoint switch
- Full broadcast switching capability
- Differential 10K PECL data path
- Up to 1.5 Gbit/s NRZ data rate
- TTL configuration controls
- Reconfigurable without disturbing operation
- 120-pin PQFP/TEP package
- +5V only power supply

APPLICATIONS

- Internet switches
- Digital video
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Datacom or telecom switching

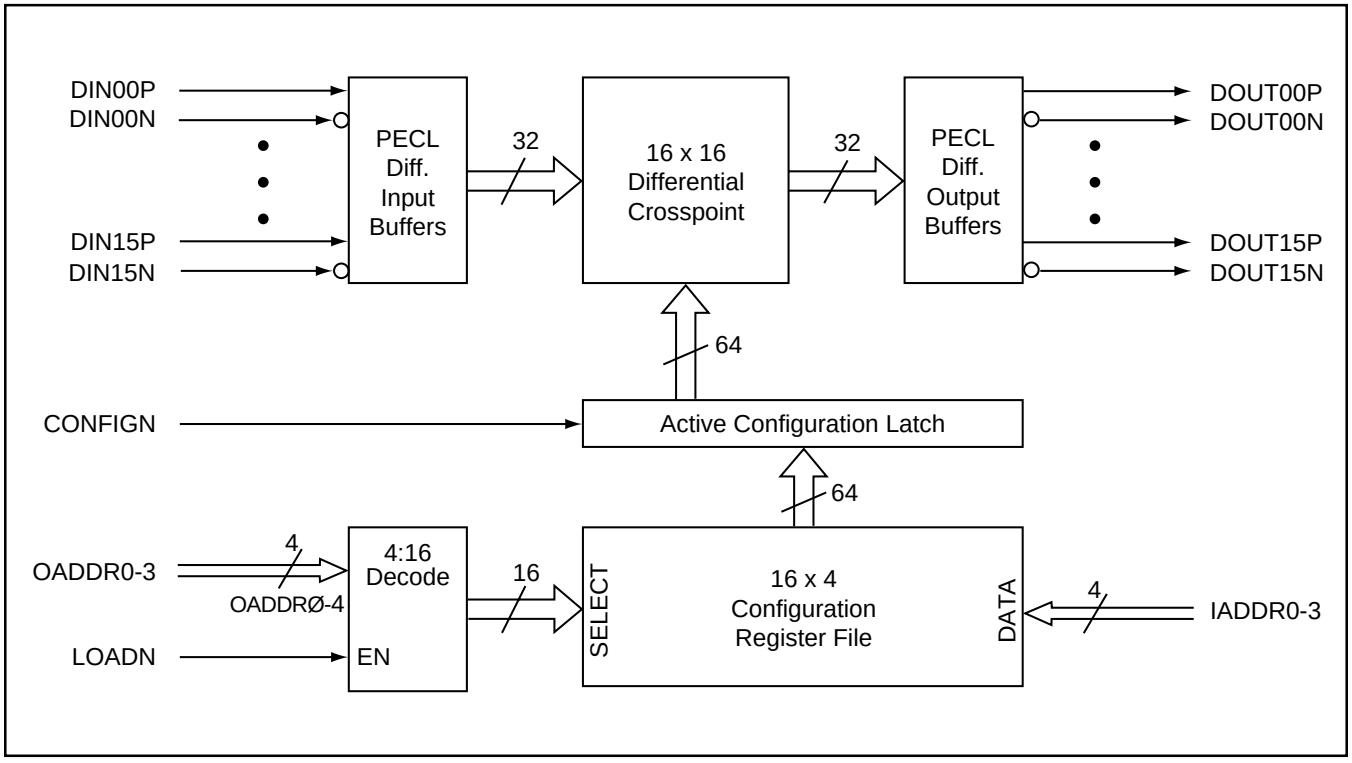
GENERAL DESCRIPTION

The S2016 is a very high-speed 16 x 16 differential crosspoint switch with full broadcast capability. Any of its 16 differential PECL input signal pairs can be connected to any or all of its 16 differential PECL output signal pairs.

The differential 10K PECL logic data path makes the part ideal for high-speed applications. The differential nature of the data path is retained throughout the crosspoint structure, to minimize data distortion and to handle NRZ data rates up to 1.5 gigabits per second.

TTL configuration controls simplify interfacing to slower speed circuitry. Once a new configuration has been entered into the configuration register file, the S2016 can be completely reconfigured by pulsing the CONFIGN input.

Figure 1. Functional Block Diagram



DATA TRANSFER

For each configured connection between a differential input pair and an enabled output pair, any data appearing at the input pair will be passed immediately through to the output pair.

RECONFIGURATION

The S2016 can be selectively reconfigured one output pair at a time, or any number of output pairs can be reconfigured simultaneously. Configuration data is stored in 16 registers, one register for each output pair. As shown in Figure 1, the configuration data is passed in parallel from all 16 registers to a latch which holds the active switch configuration. This two-stage arrangement allows one or more output pairs to be reconfigured simultaneously.

To connect an output pair to a given input pair, the output pair to be reconfigured is selected using the OADDR0-3 (OADDR3=MSB) inputs. With the output pair configuration register selected, the desired input pair selection is provided on the IADDR0-3 (IADDR3=MSB) inputs. The IADDR0-3 information will be stored into the selected output pair configuration register by the LOADN strobe.

When the differential switch is to be reconfigured, the S2016 minimizes the time required through the use of an active configuration latch. While the switch is operational, and prior to the time at which it must be reconfigured, a new configuration can be loaded into the output pair configuration registers. Once the 16 output pair configuration registers contain the desired connection and output pair driver enable information, the contents of the registers are transferred in parallel to the active configuration latch by the CONFIGN strobe. This allows multiple connections to be simultaneously changed.

The configuration latch can be made transparent by driving the CONFIGN input to a logic 0. When this is done, changes strobed into the output pair configuration registers by the LOADN input pair will be passed immediately to the switch.

Figure 2. Data Transfer Waveforms

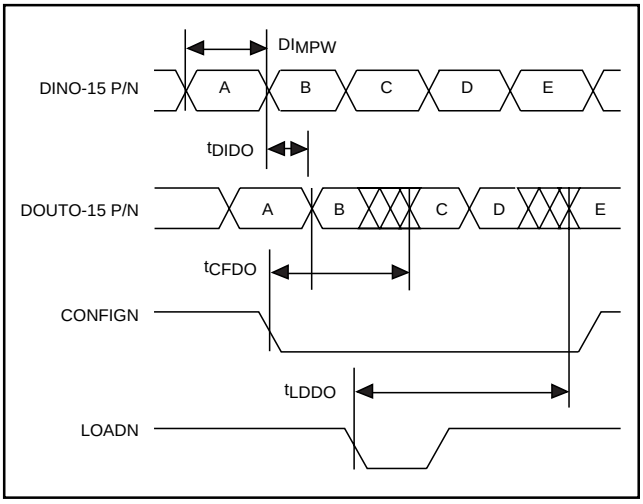


Figure 3. Reconfiguration Waveforms

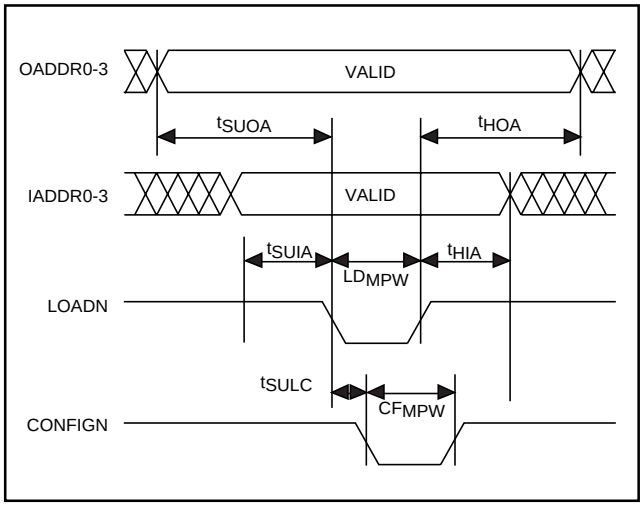


Table 1. Data Transfer Timing[1]

Symbol	Description	Min.	Max.	Units
t_{DIDO}	Propagation delay from DIN0–15 P/N to DOUT0–15 P/N		3	ns
t_{CFDO}	Propagation delay from falling edge of CONFIGN to DOUT0–15 P/N valid		6	ns
t_{LDDO}	Propagation delay from falling edge of LOADN to DOUT0–15 P/N valid (When CONFIGN is held low)		7	ns
DI_{MPW}	Pulse width of DIN0–15 P/N	0.650		ns
F_{MAX}	Data rate	1500		Mbit/s

Table 2. Reconfiguration Timing[2]

Symbol	Description	Min.	Max.	Units
t_{SUOA}	Setup time of OADDR0-3 before falling edge of LOADN	2000		ps
t_{HOA}	Hold time of OADDR0-3 after rising edge of LOADN	500		ps
t_{SUIA}	Setup time of IADDR0-3 before falling edge of LOADN	1000		ps
t_{HIA}	Hold time of IADDR0-3 after rising edge of LOADN	1500		ps
t_{SULC}	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration	0		ps
LD_{MPW}	Pulse width low of LOADN	4200		ps
CF_{MPW}	Pulse width low of CONFIGN	4200		ps

1. All timing measured from the V_{CC} -1.3V point on the signals.
2. All timing measured from the 1.5V point on the signals.

S2016 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DIN15P DIN15N DIN14P DIN14N DIN13P DIN13N DIN12P DIN12N DIN11P DIN11N DIN10P DIN10N DIN9P DIN9N DIN8P DIN8N DIN7P DIN7N DIN6P DIN6N DIN5P DIN5N DIN4P DIN4N DIN3P DIN3N DIN2P DIN2N DIN1P DIN1N DIN0P DIN0N	Diff. PECL	I	115 116 36 35 111 112 40 39 109 110 42 41 107 108 44 43 103 104 48 47 101 102 50 49 99 100 52 51 95 96 56 55	Input data. Differential. Can be used as single-ended inputs with VBB tied to one side of each differential input pair.
OADDR3 OADDR2 OADDR1 OADDR0	TTL	I	64 57 34 27	Output address, active High. Used to select an output configuration register in the configuration register file.
IADDR3 IADDR2 IADDR1 IADDR0	TTL	I	86 94 117 5	Input address, active High. IADDR3-0 selects the input pair to connect to the output pair selected by OADDR3-0.
LOADN	TTL	I	46	Load strobe, active Low. When low, stores the configuration data on IADDR0-3 into the configuration register file.
CONFIGN	TTL	I	105	Configuration strobe, active Low. When low, parallel loads the contents of the configuration register file into the active configuration latch.

S2016 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DOUT15P DOUT15N DOUT14P DOUT14N DOUT13P DOUT13N DOUT12P DOUT12N DOUT11P DOUT11N DOUT10P DOUT10N DOUT9P DOUT9N DOUT8P DOUT8N DOUT7P DOUT7N DOUT6P DOUT6N DOUT5P DOUT5N DOUT4P DOUT4N DOUT3P DOUT3N DOUT2P DOUT2N DOUT1P DOUT1N DOUT0P DOUT0N	Diff. PECL	O	26 25 22 21 20 19 18 17 15 14 13 12 11 10 7 6 65 66 69 70 71 72 73 74 76 77 78 79 80 81 84 85	Output data. Differential.
VCC	+5V	–	4, 16, 28, 33, 45, 58, 63, 75, 87, 93, 106, 118	Core Power Supply
TTLGND	GND	–	3, 29, 62, 88	TTL Ground
ECLVCC	+5V	–	8, 24, 37, 54, 67, 83, 97, 114	ECL I/O Power Supply
TTLVCC	+5V	–	32, 59, 92, 119	TTL Power Supply

S2016 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
GND	GND	–	9, 23, 38, 53, 68, 82, 98, 113	Core Ground
NC	–	–	1, 2, 30, 31, 60, 61, 89, 90, 91, 120	No Connection

Figure 4. S2016 Pinout

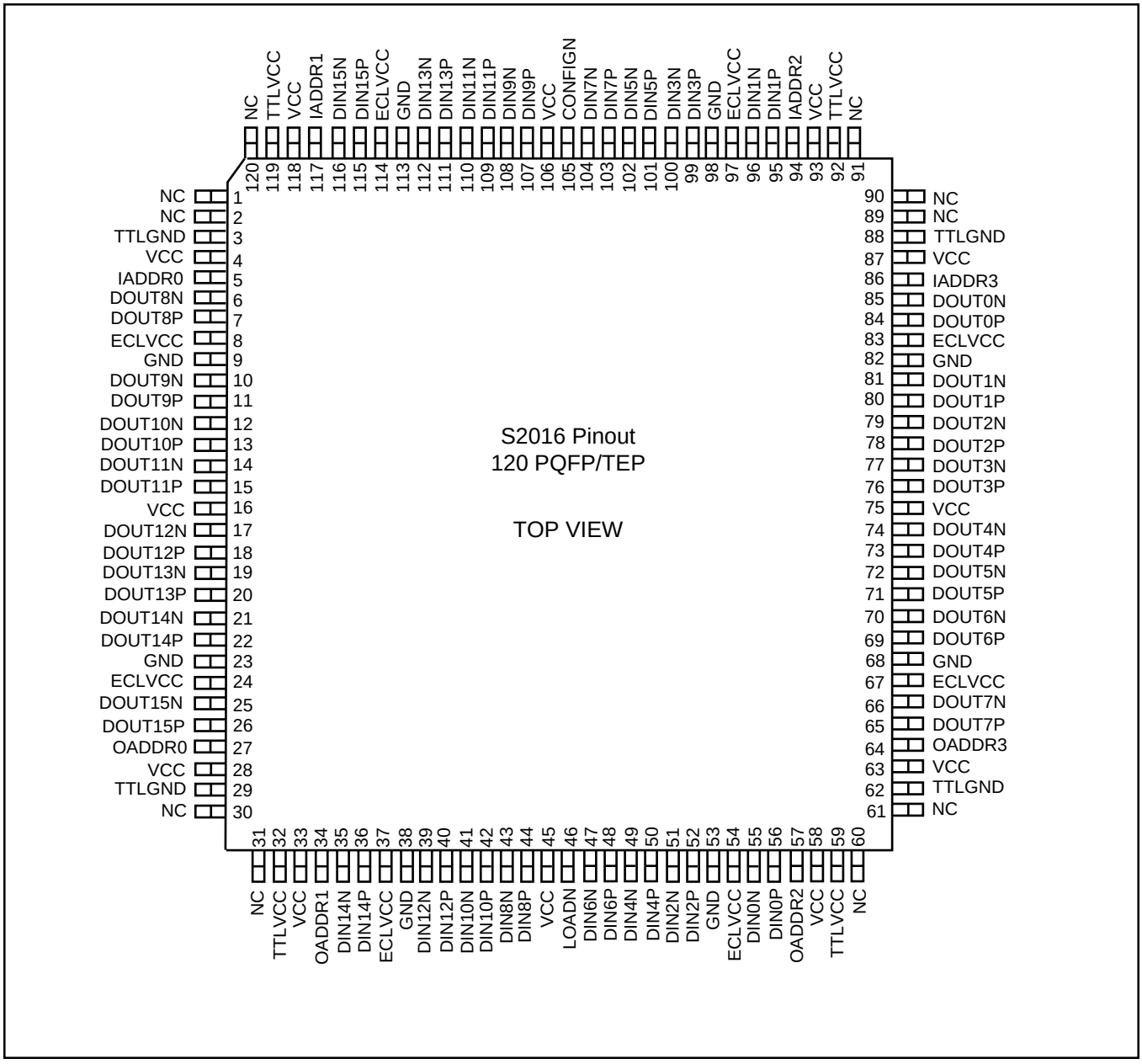
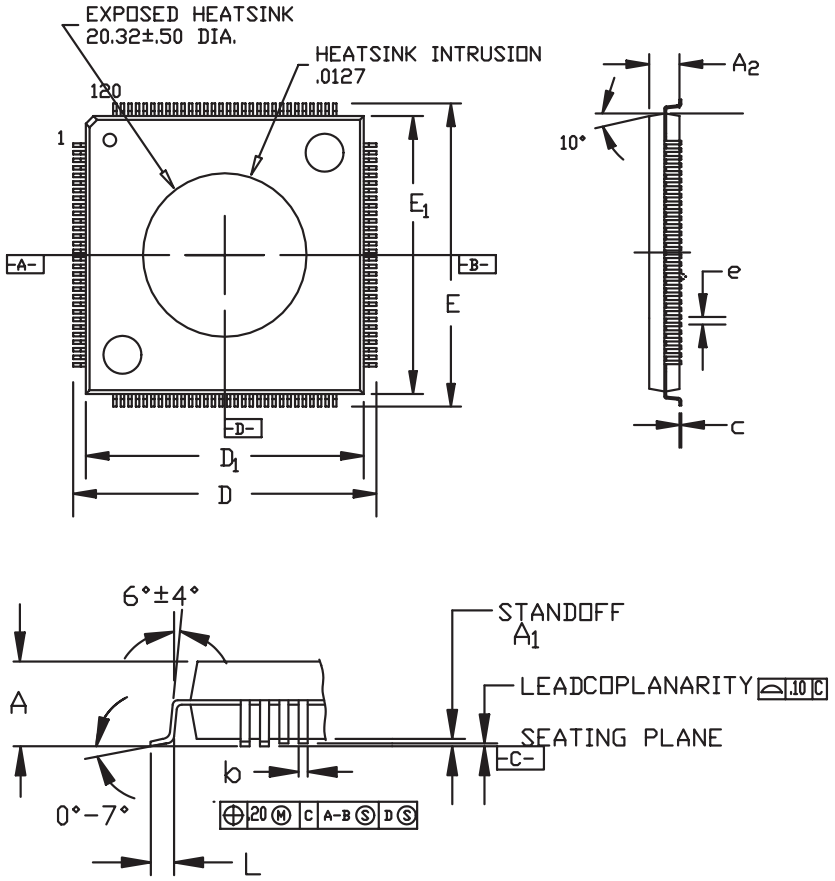


Figure 5. 120-Pin PQFP/TEP Package



DIMENSIONS (are in millimeters)

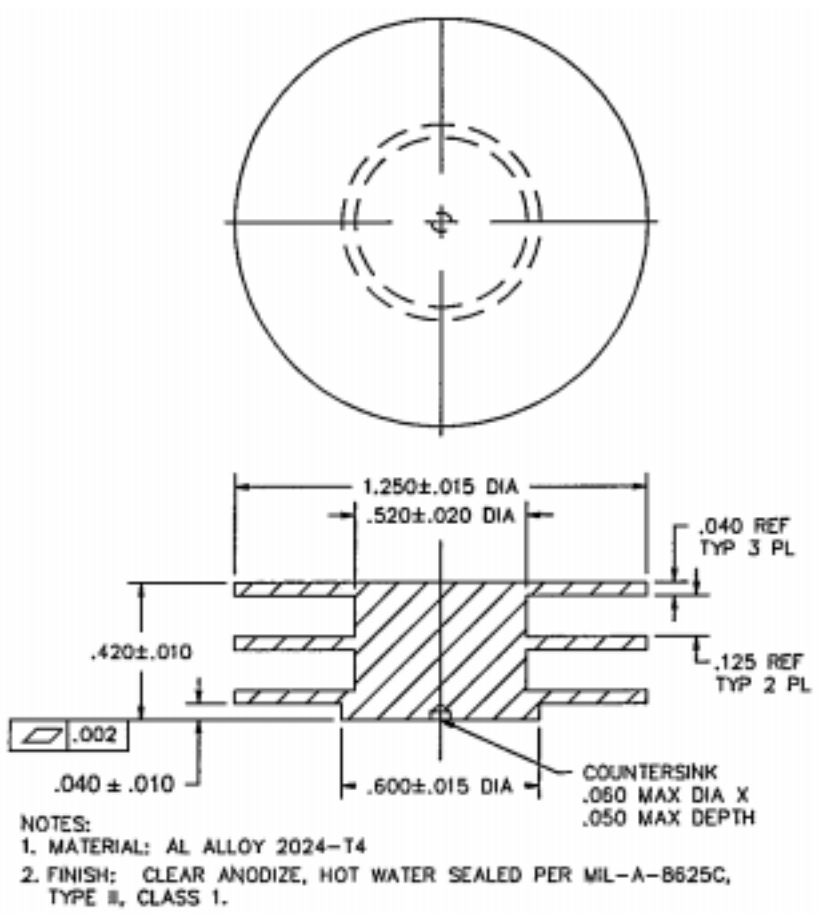
UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.25	3.39	31.00	27.90	31.00	27.90	0.78	0.80 BSC.	0.30	
NOM			3.49	31.20	28.00	31.20	28.00	0.88		0.35	
MAX	4.10	0.50	3.59	31.40	28.10	31.40	28.10	1.03		0.40	0.17

Thermal Management

Maximum VEE Supply	Power	Θja Still Air w/DW0045-10 Heatsink	Max Still Air [1] w/DW0045-10 Heatsink	Required Air [2] w/DW0045-10 Heatsink
5.25V	6.3W	18.0˚ C/W	+17˚ C	200 LFPM

1. Max ambient temperature permitted in still air to maintain Tj ≤ 130˚C.
2. Airflow required in 70˚C ambient conditions to maintain Tj ≤ 130˚C.

Figure 6. Heatsink DW0045-10



Dimensions are nominal in inches.

Table 3. Absolute Maximum Ratings

Supply Voltage V_{CC}	7.0V
PECL Input Voltage	V_{CC} – 2.5V to V_{CC}
PECL Output Source Current (continuous)	-50mA DC
TTL Input Voltage	5.5V
Operating Junction Temperature T_j	+150°C
Storage Temperature	-65°C to +150°C

Table 4. Recommended Operating Conditions

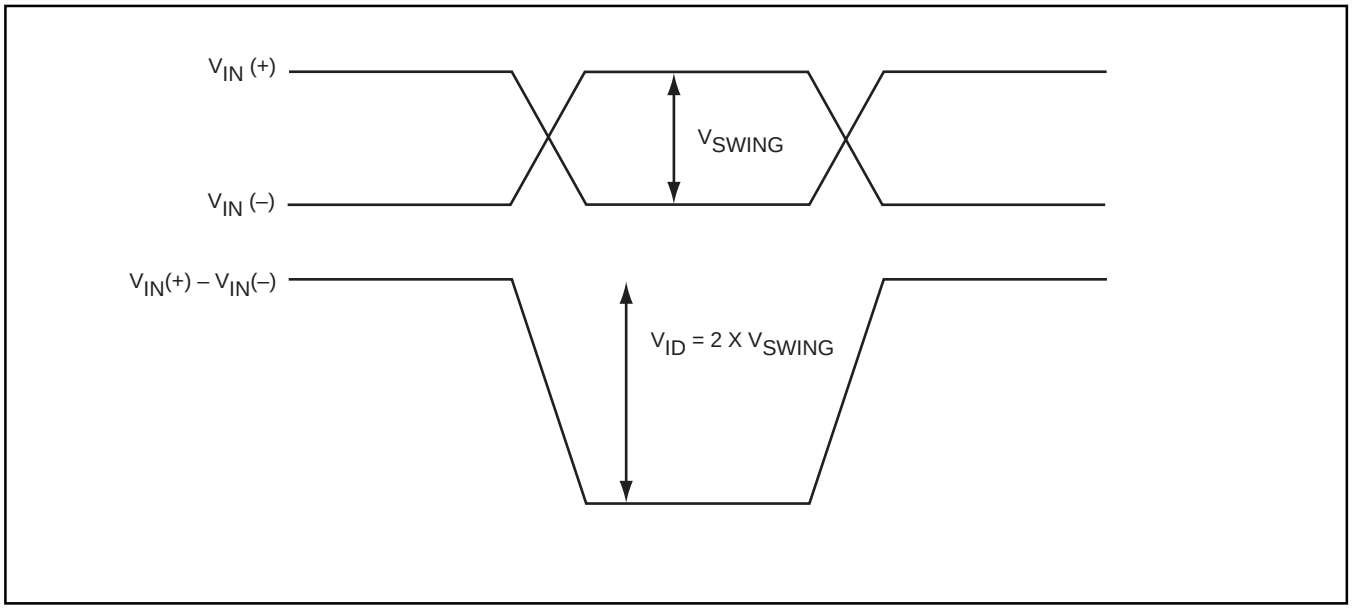
Parameter	Min	Nom	Max	Units
Supply Voltage V_{CC}	4.75	5.0	5.25	V
Ambient Temperature	0		70	°C
Junction Temperature			130	°C
I_{CC}		865	1199	mA

Table 5. TTL Input DC Characteristics

Symbol	Parameter	Conditions	Commercial 0° to 70°C			Unit
			Min	Typ[1]	Max	
V_{IH}[2]	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all input pairs	2.0			V
V_{IL}[2]	Input LOW Voltage	Guaranteed Input LOW Voltage for all input pairs			0.8	V
V_{IK}	Input Clamp Diode Voltage	V_{CC} = MIN, I_{IN} = -13 mA		-0.8	-1.2	V
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V			5	µA
I_I	Input HIGH Current at Max.	V_{CC} = MAX, V_{IN} =V_{CC} + 0.3V			1	mA
I_{IL}	Input LOW Current	V_{CC} = MAX,V_{IN} = 0.5V			-0.4	mA

1. Typical limits are at 25°C, V_{CC} = 5.0V.
2. These input levels provide a zero noise immunity and should only be tested in a static, noise-free environment.

Figure 7. Differential Input Voltage



Note: $V_{IN}(+) – V_{IN}(-)$ is the algebraic difference of the input signals.

Table 6. PECL DC Characteristics[3]

Symbol	Min	Typ	Max	Unit
V_{IH} [2]	V_{CC} – 1145		V_{CC} – 600	mV
V_{IL} [2]	V_{CC} – 2000		V_{CC} – 1450	mV
V_{BIAS} [1,2]		V_{CC} – 1300		mV
I_{IH} [2]			30	µA
I_{IL} [2]			–0.5	µA

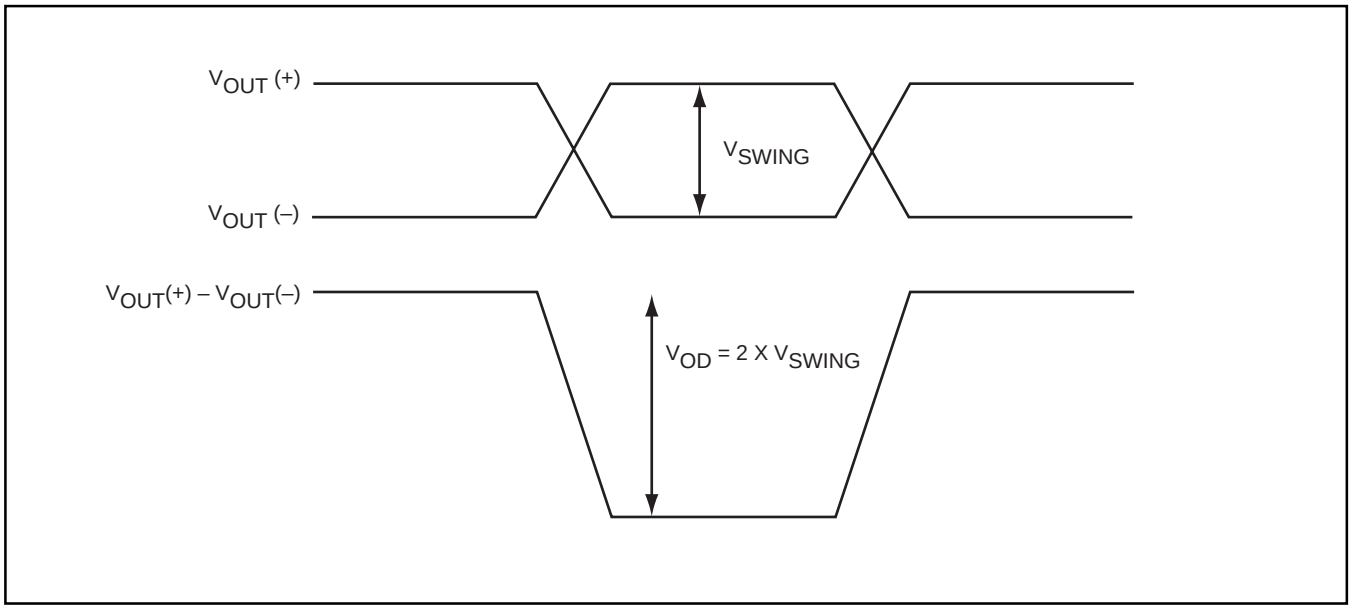
1. Internal bias point.
2. Single-ended connection.
3. DC is considered to be an input signal between 0Hz and 1KHz.

Table 7. Differential PECL Characteristics

Symbol	Min	Typ	Max	Unit
V_{ID} [1]	500		2800	mV

1. Differential input voltage – algebraic difference.

Figure 8. Differential Output Voltage



Note: $V_{OUT}(+) – V_{OUT}(-)$ is the algebraic difference of the input signals.

Table 8. PECL DC Characteristics[2]

Symbol	Min	Typ	Max	Unit
V_{OH}[1]	V_{CC} – 1095		V_{CC} – 695	mV
V_{OL}[1]	V_{CC} – 1900		V_{CC} – 1365	mV
I_{OH}		20		mA
I_{OL}		5		mA

1. All outputs are loaded with 50Ω to V_{CC} –2V
2. DC is considered to be an output signal between 0Hz and 1KHz.

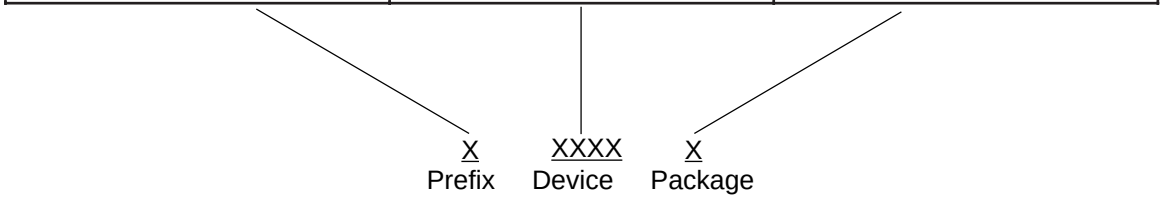
Table 9. Differential PECL Characteristics

Symbol	Min	Typ	Max	Unit
V_{OD}[1]	700		2330	mV

1. Differential output voltage – algebraic difference.

Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	2016	A – 120 PQFP/TEP Lead formed with Heatsink unattached



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