SARA®-2
ATM Cell Processing IC Device
TXC-05551

DATA SHEET
PRODUCT PREVIEW

FEATURES

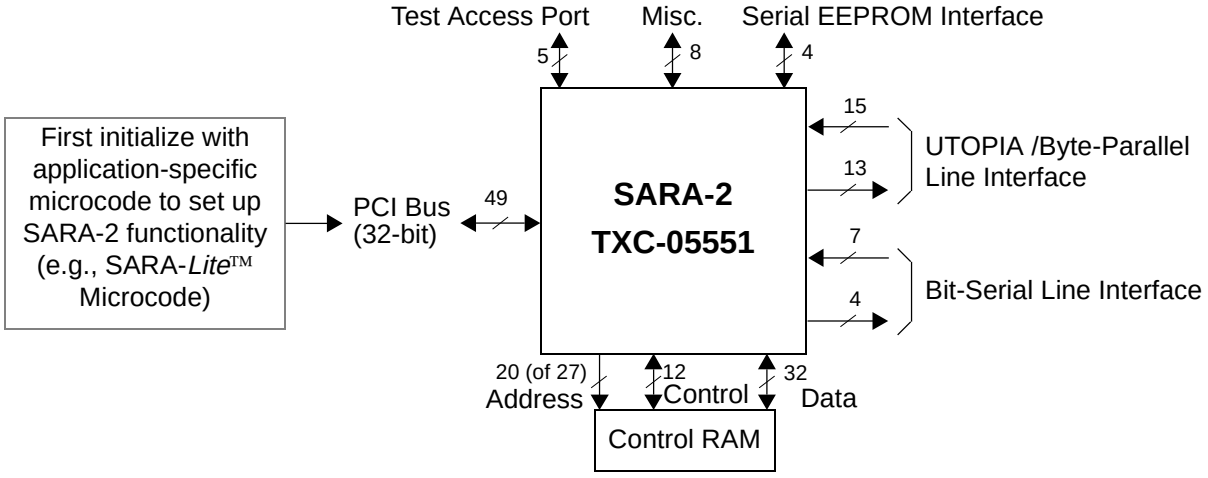
- Functionality enabled by application-specific microcode (e.g., SARA-*Lite*™ Microcode)
- Full-duplex segmentation and reassembly of multiple VCs up to 155 Mbit/s in each direction
- Integrated SONET/SDH 155 Mbit/s framer
- Optional 8-bit UTOPIA interface
- PCI bus master and slave interface supports efficient, low latency burst transfers
- Complete SAR functions for AAL5, AAL3/4 and AAL0 (null) in host memory
- Support for AAL1
- Provides over 64,000 virtual connections on transmit and receive
- Includes non-contiguous variable size packet buffers providing scatter and gather function with arbitrary byte alignment and byte order.
- Flexible scheduler provides per-connection rate management for VBR and CBR
- Programmable RISC core supports customization and vendor-specific additional features
- Supports ATM Forum UBR traffic flow control.
- Reassembly on the basis of any arbitrary subfield of the 24/28-bit VPI/VCI field
- Provides host-controlled OAM/Signalling cell insertion and extraction
- Supports ATM Forum MIB
- Boundary scan capability (IEEE 1149.1)
- Single +3.3 V, ± 5% power supply
- 225-lead plastic ball grid array package

DESCRIPTION

The SARA-2 device is intended to be used with feature/application-specific microcode that gives it a particular set of ATM segmentation and reassembly (SAR) performance characteristics. It can be used to implement low-cost ATM adapter cards, legacy LAN to ATM hubs, and routers. It provides a PCI-based host interface to segment and reassemble packets directly in the host memory. In the transmit direction, it generates cells that conform to the ATM Forum traffic management service classes, such as CBR, VBR, and UBR. On the receive side, the SARA-2 allows simultaneous reassembly of over 64,000 connections directly in the host memory. The host buffers may be arbitrarily-sized blocks placed on arbitrary byte boundaries. An integrated SONET/SDH STS-1/STS-3c/STM-1 framer and overhead termination supports complete framing, cell delineation and cell rate decoupling functions. The UTOPIA interface supports connection to other line rates or ATM layer devices.

APPLICATIONS

- ATM LAN hub
- Router
- Adapter cards



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OVERVIEW

The SARA-2 device is intended to be used with feature/application-specific microcode for its integral RISC CPU core that gives it a particular set of ATM segmentation and reassembly (SAR) performance characteristics. It can be used to implement low-cost ATM adapter cards, legacy LAN to ATM hubs, and routers. This Data Sheet describes the performance of the device, but in some areas it describes characteristics which are present only when the microcode is installed. The Data Sheet describes the characteristics that support the first such microcode introduced by TranSwitch, which is the SARA-*Lite*™ Microcode. The combination of the SARA-2 device and the SARA-*Lite*™ Microcode provides for AAL type 0 or type 5 segmentation and reassembly with Constant Bit Rate (CBR), Variable Bit Rate (VBR) and Unspecified Bit Rate (UBR) traffic management, and supports frame relay and LAN emulation applications, which may be implemented via software. Further information on this combination is provided in the SARA-*Lite* Product Summary document, number TXC-05551-SCDA-PS1.

The SARA-2 device is provided in a 225-lead plastic ball grid array package with solder ball leads and operates from a single +3.3 V supply. The device incorporates AAL processing for full-duplex operation up to 155 Mbit/s. The SARA-2 integrates a PCI-based host interface to segment and reassemble packets directly in the host memory. The device is capable of supporting over 64,000 connections simultaneously in the transmit and receive directions. In the transmit direction, the SARA-2 generates cells that conform to the ATM Forum traffic management service classes, such as CBR, VBR, and UBR. On the receive side, the SARA-2 allows simultaneous reassembly of over 64,000 connections directly in the host memory. The host buffers may be arbitrarily-sized blocks placed on arbitrary byte boundaries. An integrated SONET/SDH STS-1/STS-3c/STM-1 framer and overhead termination supports complete framing, cell delineation and cell rate decoupling functions. The UTOPIA interface supports connection to other line rates or ATM layer devices.

Major Features

- **Full-duplex cell processing at 155.52 Mbit/s data rates:** Concurrent, uninterrupted, bidirectional data streams can be supported by the SARA-2 at a maximum bit rate of 155.52 Mbit/s. The autonomous operational model used by the SARA-2, together with an efficient message-passing host interface, minimizes the host device driver overhead required to support these data rates.
- **50 MHz RISC CPU core:** The RISC core executes up to 50 million instructions per second, allowing it to perform many of the ATM and AAL protocol functions in firmware. The firmware for the core resides in on-chip RAM for maximum flexibility and easy upgrades. The RISC core also contains a 2048-byte instruction cache for executing instructions from external memory and a 1024-byte hardware-managed data cache to speed up loads and stores. The core communicates with the remainder of the logic via on-chip queues and device registers, which are mapped into the core register set to permit fast, low-overhead access. The RISC core performs most of the host communication tasks, allowing for a highly flexible implementation that can perform full-duplex segmentation and reassembly of 53-byte ATM cells at a 155.52 Mbit/s data rate.
- **Support for multiple AAL protocols:** The SARA-2 permits the AAL5, AAL3/4, AAL1 and AAL0 (raw cells) protocols to be assigned on a per-virtual-circuit basis, regardless of the number of active virtual circuits. For AAL1, the SARA-2 generates and verifies a header conforming to AAL 1 protocol without clock recovery. In AAL0 mode, either 64 bytes or 48 bytes of information may be copied between external host memory and internal cell buffers. Full transfer bandwidth can be maintained for all AAL types supported.
- **Support for Convergence Sublayer protocols:** The SARA-2 provides complete AAL3/4 and AAL5 Convergence Sublayer (CS) protocols encapsulation and termination in hardware. The AAL1 CS protocol is performed in firmware. The SARA-2 inserts a CSI bit provided by the host for transmit and extracts a received CSI bit for forwarding to the host. Firmware running on the RISC core facilitates flexible implementation and application specific customization for Frame Relay, LAN Emulation and video distribution applications.

- **Traffic Shaper:** The SARA-2 implements hardware-based traffic shaping for CBR and VBR traffic classes and provides hardware-assisted, firmware-controlled traffic shaping for UBR traffic classes.
- **PCI-based host interface port.** A fully compliant (PCI Local Bus Specification revision 2.1) PCI bus interface unit is provided to allow interfacing to host processors that support the PCI bus. All internal device registers and local memory resources available to the SARA-2 are also visible from the host interface port. Two 64-byte burst FIFOs allow the PCI bus interface to operate with PCI bus clock rates of up to 33 MHz with no wait states, yielding a peak transfer bandwidth of 132 Mbyte/s. A set of on-chip communication registers and hardware communication queue logic are provided to facilitate communications between the SARA-2 and a host processor.
- **Non-Volatile Memory Interface for PCI configuration:** The SARA-2 provides a serial EEPROM interface to support optional customization of the PCI configuration space.
- **Integrated SONET/SDH Framer:** The SARA-2 contains an on-chip SONET/SDH framer unit, which frames incoming and outgoing serial/parallel data at 51.84 Mbit/s and 155.52 Mbit/s rates using the STS-1 and STS-3c/STM-1 line codes, respectively. An external clock and data recovery device and appropriate transceivers (optical or electrical) are the only additional components needed to interface to the physical medium. It also contains functional blocks that perform cell delineation, payload descrambling, HEC single bit error correction and cell rate decoupling.
- **UTOPIA Interface:** The device contains a full-duplex, byte-wide cell interface compliant to the ATM Forum Level 1 UTOPIA specification. The cell interface can be programmed to operate as either a UTOPIA PHY-layer interface or an ATM-layer interface to allow seamless connection to an ATM switching port or to other physical layer devices. The device also supports both cell-level handshake and byte-level handshake.
- **Number of active virtual circuits limited only by external memory:** The SARA-2 imposes no internal hardware limit on the number of active virtual circuits for either transmit or receive; the number of virtual circuits is limited only by the local memory space required to hold segmentation and reassembly data structures.
- **Hashing Function:** The SARA-2 implements a programmable hashing function to support arbitrary VPI/VCI assignment and to speed up virtual circuit table lookups for reassembly functions.
- **Low-latency cell processing algorithms:** Novel recirculating cell buffer algorithms, coupled with a dedicated cell buffer queue, are used to allow high-throughput, low-latency cell processing without complex firmware or host device driver interactions. The on-demand, low-latency processing also permits the use of a small number of constantly recycled cell buffers, rather than a large number of expensive data buffers, without compromising performance.

BLOCK DIAGRAM

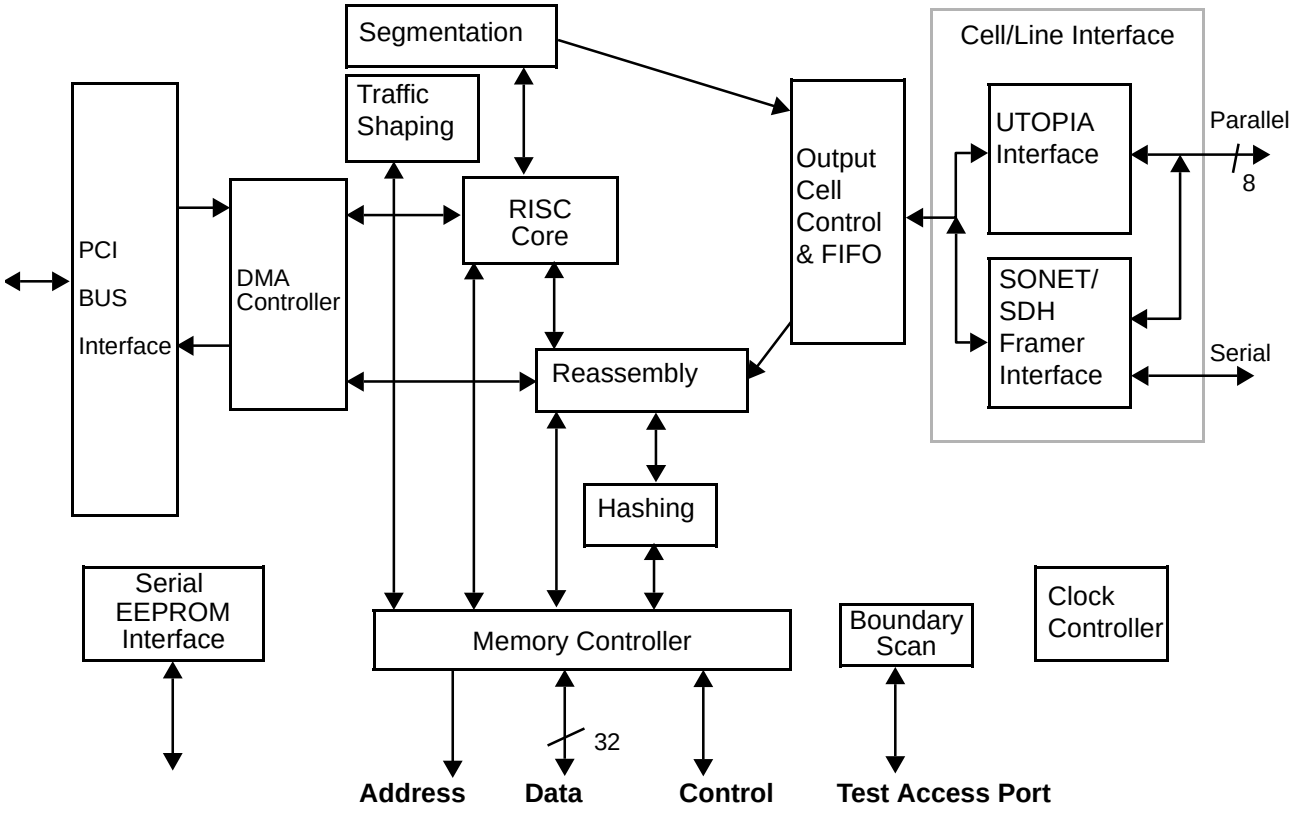

Figure 1. SARA-2 TXC-05551 Block Diagram

BLOCK DIAGRAM DESCRIPTION

A block diagram of the SARA-2 ATM Cell Processing IC device is shown in Figure 1. The SARA-2 consists of several functional blocks which are described in the following paragraphs.

- The *PCI Bus Interface* block implements the complete PCI bus protocol and acts as both a bus master and slave on the PCI bus. It provides access to the SARA-2 registers and the local memory, allowing the host processor to configure, control and communicate with the SARA-2. The interface is a bus-master interface for reading and writing cells from/to the packet memory for segmentation and reassembly.
- The *DMA Controller* block handles concurrent bidirectional transfers between the host and the SARA-2, supporting segmentation and reassembly directly in the host memory. The DMA controller incorporates powerful scatter-gather mechanisms using chains of linked buffer descriptors to describe the locations of arbitrarily-sized blocks of transmit or receive data placed on arbitrary byte boundaries.
- The *Memory Controller* block arbitrates access to the local control memory and generates the data transfer signals for the control memory. It is used to access VC structure, buffer descriptor (BD) and cell buffers maintained in the control memory. It provides a direct interface to high speed SRAM memory devices, with no requirement for intermediate 'glue' logic circuits.

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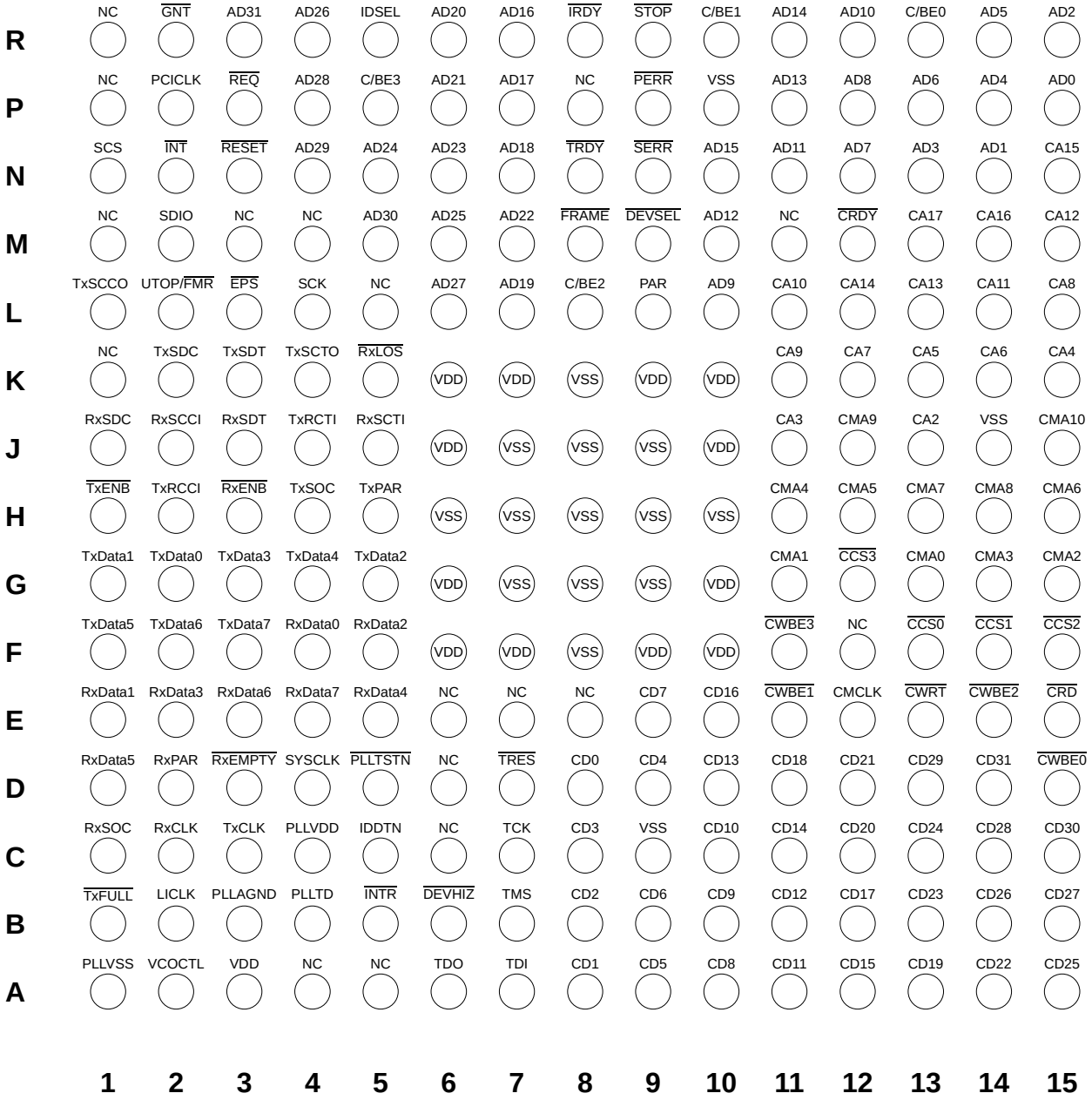
- The *Output Cell Control & FIFO* block supports concurrent bidirectional transfer of data to and from the external line/cell interface. Two-cell deep buffers in the transmit direction and two-cell deep buffers in the receive direction absorb system latencies, enhancing throughput.
- The *Hashing* block implements a hardware hash table lookup mechanism that uses hash buckets in the local memory to locate the VC state information required for reassembly of received cells. The hashing mechanisms allow support of arbitrary VPI/VCI assignment when a connection is established.
- The *Cell/Line Interface* block can be configured as either a UTOPIA interface or a byte-parallel or bit-serial SONET/SDH interface. When configured as a UTOPIA interface, it is used for transferring ATM cells to the external logic. Optionally, a built-in STS-1/STS-3c/STM-1 framer can be used to interface to external clock recovery devices. The built-in framer performs complete line framing, cell delineation and cell rate decoupling functions. When the internal framer is used, a serial interface is also supported.
- The *Segmentation* and *Reassembly* blocks perform all functions related to AAL3/4 and AAL5 processing and a majority of the functions required for AAL1 processing.
- The *Traffic Shaping* block is responsible for scheduling and rate management for all connections.
- The *RISC Core* block is responsible for control and supervisory functions and for communication with the host.
- The *Serial EEPROM Interface* block is used to support optional customization of PCI configuration space on power-up reset.
- The *Boundary Scan* block provides a Test Access Port capability conforming to the IEEE 1149.1 standard.

Further information on device operation and the interfaces to external circuits is provided below in the Operation section.

LEAD DIAGRAM



Notes: This is the bottom view. The leads are solder balls. See Figure 38 for package information.
Some signal Symbols have been abbreviated to fit the space available.

Figure 2. SARA-2 TXC-05551 Lead Diagram

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LEAD DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECT LEADS

Symbol	Solder Ball No.	I/O/P *	Type	Name/Function
VDD	A3, F6, F7, F9, F10, G6, G10, J6, J10, K6, K7, K9, K10	P		**V_{DD}**: +3.3 volt supply voltage, ± 5%
VSS	C9, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, J14, K8, P10	P		**V_{SS}**: Ground, 0 volt reference.
PLLVDD	C4	P		**PLL V_{DD}:** RC-decoupled +3 volt supply voltage, for analog section V_{DD} of device.
PLLAGND	B3	P		**PLL AGND:** Ground, 0 volt reference, for analog section ground of device.
PLLVSS	A1	P		**PLL V_{SS}:** Ground, 0 volt reference, for analog section V_{SS} of device.
NC	A4, A5, C6, D6, E6, E7, E8, F12, K1, L5, M1, M3, M4, M11, P1, P8, R1	--		**No Connect**: NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of NC leads may impair performance or cause damage to the device. Some NC leads may be assigned functions for manufacturing test purposes or in future upgrades of the device. Backwards compatibility of the upgraded device in existing applications may rely upon these leads having been left floating.

*Note: I = Input; O = Output; P = Power; (T) = Tri-state

PCI INTERFACE

Symbol	Solder Ball No.	I/O/P	Type *	Name/Function
PCICLK	P2	I	LVPCI-5	**PCI Bus Clock:** Provides the timing for all transactions on the PCI bus. All other bus signals are sampled on the rising edge of this clock.
AD(31-0)	R3, M5, N4, P4, L6, R4, M6, N5, N6, M7, P6, R6, L7, N7, P7, R7, N10, R11, P11, M10, N11, R12, L10, P12, N12, P13, R14, P14, N13, R15, N14, P15	I/O(T)	LVPCI-5/ PCI	**Address/Data Bus:** Bidirectional multiplexed Address and Data leads for the PCI bus. Each bus transaction consists of an address phase followed by one or more data phases. Address phases are identified when the control signal $\overline{\text{FRAME}}$ is asserted. Data is transferred during those clock cycles where both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted.
C/BE(3-0)	P5 L8 R10 R13	I/O(T)	LVPCI-5/ PCI	**Command/Byte Enable:** During the address phase of a transaction, these leads supply the bus command. During the data phase these leads are used as byte enables for each bus transaction.

*See the Input, Output and I/O Parameters section for Type descriptions.

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Symbol	Solder Ball No.	I/O/P	Type *	Name/Function
PAR	L9	I/O(T)	LVPCI-5/ PCI	**Parity:** Even parity across AD(31-0) and C/BE(3-0) during valid data and address phases. PAR is stable and valid one clock time after the completion of the data or address phase.
$\overline{\text{FRAME}}$	M8	I/O(T)	LVPCI-5/ PCI	**Cycle Frame:** A falling edge indicates the beginning of a bus transaction with an address phase. A rising edge indicates that the next data phase marks the end of the current transaction.
$\overline{\text{IRDY}}$	R8	I/O(T)	LVPCI-5/ PCI	**Initiator Ready:** A low indicates the bus master's ability to complete the current data phase of the transaction. A valid data phase is completed on a clock edge when both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are sampled as asserted.
$\overline{\text{TRDY}}$	N8	I/O(T)	LVPCI-5/ PCI	**Target Ready:** A low indicates the target's ability to complete the current data phase of the transaction. A valid data phase is completed on a clock edge when both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are sampled as asserted.
$\overline{\text{STOP}}$	R9	I/O(T)	LVPCI-5/ PCI	**Stop:** Driven low by the current target to request the master to abort, disconnect or retry the current transaction.
IDSEL	R5	I	LVPCI-5	**Initialization Device Select:** Used as a chip select to select SARA-2 during configuration read and write transactions.
$\overline{\text{DEVSEL}}$	M9	I/O(T)	LVPCI-5/ PCI	**Device Select:** When actively driven low, indicates the driving device has decoded the address placed on AD(31-0) as a valid reference to the target's address space. When SARA-2 acts as a bus target, this signal is held asserted low until $\overline{\text{FRAME}}$ is deasserted.
$\overline{\text{REQ}}$	P3	O(T)	PCI	**Request:** Asserted low by SARA-2 to request control of the bus.
$\overline{\text{GNT}}$	R2	I	LVPCI-5	**Grant:** The PCI bus arbiter asserts this signal low to indicate to SARA-2 that it has been granted control of the PCI bus and may begin a new transaction after the current transaction has completed.
$\overline{\text{INT}}$	N2	OD	PCI	**Interrupt:** This active low signal is used by SARA-2 to signal an interrupt request. This lead must be connected to the INTA line on the PCI bus.
$\overline{\text{PERR}}$	P9	I/O(T)	LVPCI-5/ PCI	**Parity Error:** This active low signal indicates a parity error on the 36 AD(31-0) and C/BE(3-0) lines.
$\overline{\text{SERR}}$	N9	OD	PCI	**System Error**: A low indicates that a parity error has occurred on the 36 AD(31-0) and C/BE(3-0) lines during the address phase.
$\overline{\text{RESET}}$	N3	I	LVPCI-5	**Reset:** This lead, when driven low for a minimum of 64 system clock cycles, will reset all state machines in the device.

PARALLEL LINE INTERFACE

Symbol	Solder Ball No.	I/O/P	Type	Name/Function
RxCLK	C2	I	LVTTL-5	**Receive Input Clock:** Receive clock input used to write data into SARA-2. Framer Mode: Byte-wide data RxData(7-0) is clocked in on the rising edge of this clock whose rate is either 6.48 MHz (STS-1), or 19.44 MHz (STS-3c/STM-1), when control bit RCS in Mode Register 2 is a 0. When control bit RCS is a 1, data is clocked in on the falling edge.
RxData(7-0)	E4, E3, D1, E5, E2, F5, E1, F4	I	LVTTL-5	**Receive Input Data Bus:** UTOPIA Mode: The input data bus carries the ATM cell octets that are written into SARA-2. RxData(7-0) is sampled on the rising edge of RxCLK. Framer Mode: Byte-wide data. The data present on RxData7 is the MSB and the first bit received in the SDH/SONET format. RxData0 is the LSB and the last bit received in the byte.
RxPAR	D2	I	LVTTL-5	**Receive Input Data Parity**: This line serves as the odd parity bit over RxData(7-0). Used only in the UTOPIA mode.
RxSOC	C1	I	LVTTL-5	**Receive Input Start of Cell:** Used in the UTOPIA mode, the cell input start of cell signal marks the first byte of a cell. RxSOC is sampled on the rising edge of RxCLK.
$\overline{\text{RxEMPTY}}$ / RxCLAV / $\overline{\text{RxENB}}$	D3	I	LVTTL-5	UTOPIA-ATM Octet Handshake Mode: **Receive Buffer Empty:** In this mode, the external device should assert this signal low if its receive buffer is empty and no more data can be transferred. It is sampled on the rising edge of RxCLK. UTOPIA-ATM Cell Handshake Mode: **Cell Available Signal:** In this mode, the external device should assert this signal high if it has at least one complete cell to send. UTOPIA-PHY Mode: **Enable Signal:** In this mode (both octet and cell level), the lead acts as an enable signal for the data transfer. The external device should assert this signal low to indicate valid data on the RxData(7-0), RxSOC and RxPAR inputs.
$\overline{\text{RxENB}}$ / $\overline{\text{RxFULL}}$ / RxCLAV	H3	O	LVTTL-5 4mA	UTOPIA-ATM Mode: **Receive Enable Signal:** In this mode (both octet and cell level), the lead acts as an enable signal for the data transfer. Driven low by the SARA-2 to indicate that it is ready to receive data on the RxData(7-0), RxSOC and RxPAR inputs. UTOPIA-PHY Octet Handshake Mode: **Receive Buffer Full:** In this mode, the SARA-2 asserts this signal low if its receive buffer can accept at most 4 bytes. UTOPIA-PHY Cell Handshake Mode: **Cell Available Signal:** In this mode, the SARA-2 asserts this signal high if it can accept a complete cell.

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Symbol	Solder Ball No.	I/O/P	Type	Name/Function
TxCLK	C3	I	LVTTL-5	**Transmit Clock Input:** Transmit clock input used to read data from SARA-2. Data is output on the rising edge of this clock. Framer Mode: Byte-wide data TxData(7-0) is clocked out on the rising edge of this clock whose rate is either 6.48 MHz (STS-1), or 19.44 MHz (STS-3c/STM-1), when control bit TCS in Mode Register 2 is a 0. When control bit TCS is a 1, data is clocked out on the falling edge.
TxData(7-0)	F3, F2, F1, G4, G3, G5, G1, G2	O(T)	LVTTL-5 4mA	**Transmit Output Data:** UTOPIA Mode The cell output data bus carries the ATM cell octets that are read from SARA-2. TxData(7-0) is output on the rising edge of TxCLK. Framer Mode Byte-wide data. The data present on TxData7 is the MSB and the first bit transmitted in the SDH/SONET format. TxData0 is the LSB and the last bit transmitted in the byte. See Note 1.
TxPAR	H5	O(T)	LVTTL-5 4mA	**Transmit Output Data Parity**: This line serves as the odd parity bit over TxData(7-0). Used only in the UTOPIA mode. See Note 1.
TxSOC	H4	O(T)	LVTTL-5 4mA	**Transmit Output Start of Cell:** In UTOPIA mode, this signal marks the first byte of a data transfer. This signal is asserted high during the first byte of a 53-byte cell. See Note 1.
$\overline{\text{TxFULL}}$ / TxCLAV / $\overline{\text{TxENB}}$	B1	I	LVTTL-5	UTOPIA-ATM Octet Handshake Mode: **Transmit Output Buffer Full:** In this mode, the external device should assert this signal low to indicate that it can accept at most 4 bytes. UTOPIA-ATM Cell Handshake Mode: **Cell Available Signal:** In this mode, the external device should assert this signal high to indicate that it can accept a full cell. UTOPIA-PHY Mode: **Transmit Enable Signal:** In this mode (both octet and cell level), the lead acts as an enable signal for the data transfer. It should be driven low by the external device to indicate that it is ready to accept the TxData(7-0), TxSOC and TxPAR outputs. This lead may also be set high to place the TxData(7-0), TxPAR and TxSOC outputs in the tri-state condition.

Note 1: These leads are tri-stated for PHY layer operation when $\overline{\text{TXENB}}$ is deactivated. They are not tri-stated during ATM layer operation.

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Symbol	Solder Ball No.	I/O/P	Type	Name/Function
$\overline{\text{TxENB}}$ / $\overline{\text{TxEMPTY}}$ / TxCLAV	H1	O	LVTTL-5 4mA	UTOPIA-ATM Mode: **Transmit Enable Signal:** In this mode (both octet and cell level), this signal is asserted low by SARA-2 whenever valid data has been placed on the TxData(7-0), TxSOC and TxPAR leads. UTOPIA-PHY Octet Handshake Mode: **Transmit FIFO Empty:** In this mode, the SARA-2 asserts this signal low if its transmit buffer is empty and no more data can be sent. UTOPIA-PHY Cell Handshake Mode: **Cell Available Signal:** In this mode, the SARA-2 asserts this signal high if it can send a complete cell.
UTOP/$\overline{\text{FMR}}$	L2	I	LVTTL-5p	**Utopia / Framer Mode Select:** Set high for UTOPIA mode, low for Framer mode.
LICLK	B2	O	LVTTL-5 4mA	**Line Interface Clock:** This asymmetric clock is an output clock derived from SYSCLK and may be used to drive the line interface clock input of external devices. The frequency is two-fifths the frequency of SYSCLK.

SERIAL LINE INTERFACE

Symbol	Solder Ball No.	I/O/P	Type	Name/Function
RxSCTI	J5	I	PECL	**Receive Serial Clock True Input:** (pseudo-ECL Level). True and complementary data are clocked in on the rising edge of this clock whose rate is either 51.84 MHz (STS-1), or 155.52 MHz (STS-3c/STM-1).
RxSCCI	J2	I	PECL	**Receive Serial Clock Complement Input:** This lead, with its complement RxSCTI, is the input clock that accompanies the data on RxSDT and RxSDC.
RxSDT	J3	I	PECL	**Receive Serial Data True:** This lead, with its complement RxSDC, is the input data to SARA-2.
RxSDC	J1	I	PECL	**Receive Serial Data Complement:** This lead, with its complement RxSDT, is the input data to SARA-2.
$\overline{\text{RxLOS}}$	K5	I	LVTTL-5	**Receive Loss Of Signal In.** An external active low signal from upstream circuitry that indicates a loss of signal condition. This signal is reported as a loss of signal alarm indication.
TxRCTI	J4	I	PECL	**Transmit Serial Reference Clock True Input:** (pseudo-ECL Level). This lead, with its complement TxRCCI, is used to derive the transmit output clock, and to synchronize the transmit data. The clock rate is either 51.84 MHz (STS-1), or 155.52 MHz (STS-3c/STM-1). The retimed clock is output on TxSCTO and TxSCCO.

Symbol	Solder Ball No.	I/O/P	Type	Name/Function
TxRCCI	H2	I	PECL	**Transmit Serial Reference Clock Complement Input:** (pseudo-ECL Level). This lead, with its complement TxRCTI, is used to derive the transmit output clock, and to synchronize the transmit data. The clock rate is either 51.84 MHz (STS-1), or 155.52 MHz (STS-3c/STM-1). The retimed clock is output on TxSCCO and TxSCTO.
TxSCTO	K4	O	PECL 50 ohm	**Transmit Serial Clock True Output:** (pseudo-ECL Level). This lead, with its complement TxSCCO, clocks out data on the rising edge of this clock whose rate is either 51.84 MHz (STS-1), or 155.52 MHz (STS-3c/STM-1). This clock is derived from the transmit input clock TxRCTI.
TxSCCO	L1	O	PECL 50 ohm	**Transmit Serial Clock Complement Output:** This lead, with its complement TxSCTO, is the retimed output of TxRCTI and TxRCCI.
TxSDT	K3	O	PECL 50 ohm	**Transmit Serial Data True:** This lead, with its complement TxSDC, is the output SONET/SDH data.
TxSDC	K2	O	PECL 50 ohm	**Transmit Serial Data Complement:** This lead, with its complement TxSDT, is the output SONET/SDH data.

CONTROL MEMORY INTERFACE

Symbol	Solder Ball No.	I/O/P	Type	Name/Function
CD(31-0)	D14, C15, D13, C14, B15, B14, A15, C13, B13, A14, D12, C12, A13, D11, B12, E10, A12, C11, D10, B11, A11, C10, B10, A10, E9, B9, A9, D9, C8, B8, A8, D8	I/O	LVTTL-5/ LVTTL-5 6mA	**Control Memory Data Bus:** Bidirectional data path to external control memory.
CA(17-2)	M13, M14, N15, L12, L13, M15, L14, L11, K11, L15, K12, K14, K13, K15, J11, J13	O	LVTTL-5 6mA	**Control Memory Address Bus:** Provides bits 17 through 2 of the 24-bit byte address to the external memory devices. In essence, this is the 32-bit word address.
$\overline{\text{CWBE(3-0)}}$	F11, E14, E11, D15	O	LVTTL-5 6mA	**Control Memory Write Byte Enable**: These active low signals are the byte enables during write operation for each of the four bytes of CD(31-0).

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Symbol	Solder Ball No.	I/O/P	Type	Name/Function
CMA(10-0)	J15, J12, H14, H13, H15, H12, H11, G14, G15, G11, G13	O	LVTTL-5 6mA	**Multiplexed Control Memory Address Bus:** These lines can present additional control memory address bits when SRAM is being accessed. The specific bits placed on the bus depend on the MXSEL bits. Please refer to the description of Mode Register 0.
$\overline{\text{CCS(3-0)}}$	G12, F15, F14, F13	O	LVTTL-5 6mA	**Control Memory Chip Select:** These active low signals select one of four memory banks and correspond to the bits 23 and 22 of the 24-bit physical byte address.
$\overline{\text{CRD}}$	E15	O	LVTTL-5 6mA	**Control Memory Read**: This active low lead provides the read signal to the external control memory.
$\overline{\text{CWRT}}$	E13	O	LVTTL-5 6mA	**Control Memory Write:** This active low lead provides the write signal to the external control memory. The individual byte enable signals are provided by $\overline{\text{CWBE(3-0)}}$.
$\overline{\text{CRDY}}$	M12	I	LVTTL-5	**Control Memory Ready**: This input is not used and should be tied low.
CMCLK	E12	O	LVTTL-5 6mA	**Control Memory Clock Output:** This clock is a synthesized version of SYSCLK and is used for timing the control memory interface.

SERIAL EEPROM INTERFACE

Symbol	Solder Ball No.	I/O/P	Type	Name/Function
$\overline{\text{EPS}}$	L3	I	LVTTL-5p	**EEPROM Select:** This active low lead is used to select the external EEPROM for configuring PCI registers.
SCK	L4	O	LVTTL-5 4mA	**Serial EEPROM Clock:** This clock lead is used for the serial EEPROM interface.
SCS	N1	O	LVTTL-5 4mA	**Serial EEPROM Chip Select:** Chip select lead for serial EEPROM interface.
SDIO	M2	I/O	LVTTL-5/ LVTTL-5 4mA	**Serial EEPROM Address Output/Data Input:** Address and Data lead for the serial EEPROM interface.

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MISCELLANEOUS SIGNALS

Symbol	Solder Ball No.	I/O/P	Type	Name/Function
SYSCLK	D4	I	LVTTL	**System Clock:** This clock is used by the device to run the internal state machines and control memory interface. The SYSCLK clock rate must be between 21 MHz and 50 MHz and the duty cycle must be (50±10) %.
$\overline{\text{INTR}}$	B5	I	LVTTL-5	**Interrupt:** This active low signal enables an external device to interrupt the RISC processor within SARA-2.
$\overline{\text{DEVHIZ}}$	B6	I	LVTTL-5p	**Device High Impedance:** This asynchronous input lead, when driven low, will place all of the SARA-2 output leads in a high impedance state, except for TDO, TxSCTO, TxSCCO, TxSDT, TxSDC and VCOCTL.
VCOCTL	A2	I/O	LVCMOS	**VCO Control Voltage Lead:** This is the VCO control voltage lead for connection to an external loop filter.
IDDTN	C5	I	LVTTL-5	**IDD Test Enable:** This is an active high test lead for IDD. For normal operation it MUST be held low.
PLLTD	B4	I	LVTTL	**PLL ByPass Clock:** Input clock bypassing PLL.
$\overline{\text{PLLTSTN}}$	D5	I	LVTTL-5d	**System Clock Selection:** The clock from pin SYSCLK is selected if this pin is tied low. The clock from pin PLLTD is selected if this pin is tied high. If the system clock frequency is less than 50 MHz, this pin should be tied high for proper operation.

BOUNDARY SCAN INTERFACE

Symbol	Solder Ball No.	I/O/P	Type	Name/Function
TCK	C7	I	LVTTL-5	**IEEE 1149.1 Test Access Port Serial Scan Clock:** This signal is used to shift data into TDI and out of TDO.
TMS	B7	I	LVTTL-5p	**IEEE 1149.1 Test Access Port Mode Select:** TMS is sampled on the rising edge of TCK, and is used to place the Test Access Port controller into various states as defined in IEEE 1149.1.
TDI	A7	I	LVTTL-5p	**IEEE 1149.1 Test Access Port Serial Scan Data In:** Serial test instructions and data are clocked into this lead on the rising edge of TCK.
TDO	A6	O(T)	LVTTL-5 4mA	**IEEE 1149.1 Test Access Port Serial Scan Data Out:** Serial test instructions and data are clocked out of this lead on the falling edge of TCK.
$\overline{\text{TRES}}$	D7	I	LVTTL-5p	**IEEE 1149.1 Test Access Port Reset Lead:** This signal will asynchronously reset the Test Access Port (TAP) controller. Upon power-up, $\overline{\text{TRES}}$ must be set low then high; this will set the device into boundary scan bypass mode for normal operation.

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ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	3.9	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD}+0.5	V	Note 1
Operating junction temperature	T_J		125	^oC	Note 1
Storage temperature range	T_S	-40	125	^oC	Note 1
Ambient operating temperature	T_A	0	70	^oC	0 ft/min linear airflow
Lead Temperature x Time	TI		270 x 5	^oC x s	
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, non-condensing	RH		100	%	Note 2
ESD Classification	ESD		±2000	V	per MIL-STD-883D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended or warranted.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient			22	$^oC/W$	0 ft/min linear airflow.

RECOMMENDED OPERATING CONDITIONS AND POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.15	3.30	3.45	V	
I_{DD}			720	mA	
Power dissipation, P_{DD}			2.5	W	Inputs Switching

INPUT, OUTPUT AND I/O PARAMETERS

Input Parameters for LVCMOS (Low Voltage CMOS)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.7 * V_{DD}		V_{DD} + 0.3	V	3.15 ≤ V_{DD} ≤ 3.45
V_{IL}	-0.5		0.2 * V_{DD}	V	3.15 ≤ V_{DD} ≤ 3.45
Input leakage current	-10		10	µA	V_{DD} = 3.45
Input capacitance		5		pF	

Input Parameters for LVTTL (Low Voltage TTL)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		V_{DD} + 0.3	V	3.15 ≤ V_{DD} ≤ 3.45
V_{IL}			0.8	V	3.15 ≤ V_{DD} ≤ 3.45
Input leakage current	-10		10	µA	V_{DD} = 3.45
Input capacitance		5		pF	

Input Parameters for LVTTL-5 (Low Voltage TTL, 5 volt tolerant)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.5	V	3.15 ≤ V_{DD} ≤ 3.45
V_{IL}			0.8	V	3.15 ≤ V_{DD} ≤ 3.45
Input leakage current	-10		10	µA	V_{DD} = 3.45
Input capacitance		5		pF	

Input Parameters for LVTTL-5d (Low Voltage TTL, 5 volt tolerant with pull-down resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.5	V	3.15 ≤ V_{DD} ≤ 3.45
V_{IL}			0.8	V	3.15 ≤ V_{DD} ≤ 3.45
Input leakage current	35	115	222	µA	V_{DD} = 3.45; V_{IN} = V_{DD}
Input leakage current			10	µA	V_{IN} = V_{SS}
Input capacitance		5		pF	

Input Parameters for LVTTL-5p (Low Voltage TTL, 5 volt tolerant with pull-up resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.5	V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current	-35	-115	-214	µA	$V_{DD} = 3.45$; $V_{IN} = V_{SS}$
Input leakage current			10	µA	$V_{IN} = V_{DD}$
Input capacitance		5		pF	

Input Parameters for LVPCI-5 (Low Voltage PCI-compliant, 5 volt tolerant)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	$0.5 * V_{DD}$		5.5	V	$3.15 \le V_{DD} \le 3.45$
V_{IL}	-0.5		$0.3 * V_{DD}$	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current	-10		10	µA	$V_{DD} = 3.45$
Input capacitance		5		pF	

Input Parameters for PECL (Differential Input, Pseudo-ECL)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{REF}		2.0		V	Midpoint of V_A and V_{AN}
V_{IH}	V_{REF} + 0.05			V	$V_A - V_{AN} = 50$ mV
V_{IL}			V_{REF} - 0.05	V	$V_A - V_{AN} = 50$ mV
V_{CM} (common mode)	TBD	TBD	TBD	V	TBD
I_{IL}	-10			µA	$V_{IN} = V_{CC}$
I_{OH}			10	µA	$V_{IN} = V_{SS}$

Output Parameters for LVTTL-5 4mA (Low Voltage TTL, 5 volt tolerant, 4mA)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -4.0
V_{OL}	0		0.4	V	V_{DD} = 3.15; I_{OL} = -4.0
I_{OL}			4.0	mA	V_{OL} = 0.4
I_{OH}			-4.0	mA	V_{OH} = 2.4
I_{OZ}	-10		10	µA	

Output Parameters for LVTTL-5 6mA (Low Voltage TTL, 5 volt tolerant, 6mA)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -6.0
V_{OL}	0		0.4	V	V_{DD} = 3.15; I_{OL} = -6.0
I_{OL}			6.0	mA	V_{OL} = 0.4
I_{OH}			-6.0	mA	V_{OH} = 2.4
I_{OZ}	-10		10	µA	

Output Parameters for PCI (PCI-compliant output at 6mA)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 4.0
I_{OL}			12	mA	V_{OL} = 0.4
I_{OH}			-12	mA	V_{OH} = 2.4

Output Parameters for PECL 50 ohm (Differential Output, Pseudo-ECL, 50 ohms)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.21	2.51	2.78	V	R_T = 50 ohms, VT = 1.7 V
V_{OL}	1.54	1.70	1.86	V	R_T = 50 ohms, VT = 1.7 V
I_{NN}		10		µA	
I_{OH}		-16		mA	R_T = 50 ohms, VT = 1.7 V
V_T		1.7		V	Termination Voltage

OPERATION

SEGMENTATION AND REASSEMBLY OVERVIEW

This section describes the overall segmentation and reassembly process used by the SARA-2. Later sections provide the complete details of the functional blocks, data structures and tables associated with the segmentation and reassembly operation. The host software interacts with the SARA-2 via a service interface consisting of request and indicate message rings (both low and high-priority) in host memory: the host places requests in a request ring, and the SARA-2 places responses and notifications in an indicate ring. The messages and the data exchanged between the host software and the SARA-2 are dependent on the adaptation layer used. In the following sub-section, the Segmentation and Reassembly operation is described with AAL5 as an example.

ATM Adaptation Layer Support

The SARA-2 supports complete segmentation and reassembly functions associated with AAL3/4 and AAL5, including CRC generation and checking. The device also performs most of the SAR function for AAL1. For AAL1, both 47-byte and 48-byte modes of operation are supported. In the 47-byte mode, the device can generate sequence number, CRC-3 and parity in the transmit direction. In the receive direction, all SAR header fields are checked. Cell loss is detected and notified to the host for further processing. The SARA-2 allows pre-formatted OAM cells to be inserted on an active connection. The device calculates CRC-10 for transmitted OAM cells and checks the CRC-10 for received OAM cells. Raw cells or AAL0 cells are also supported.

Segmentation Operation

The SARA-2 continuously segments and transmits ATM cells at up to 155 Mbit/s, supporting CBR, VBR and UBR traffic classes. Simultaneous segmentation of up to 64,000 virtual circuits is supported with each virtual circuit(VC) specified as AAL1, AAL3/4 or AAL5. AAL0 and OAM cells are also supported. For testing and similar purposes, the AAL0 VC has an option that allows the application to specify entire 64-byte cells for transmission. When a VC is established, the Segmentation VC structure and Rate Control Table (RCT) entries are initialized by the host software via a service interface request, supplying the AAL type and the ATM cell header and traffic parameters. The SARA-2 scatter capability enables the host application to supply a packet stored in multiple host buffers, which do not have to be in contiguous host memory. When each host buffer is ready for segmentation, the host software notifies the SARA-2 using the service interface. The “send segment” request includes the host buffer base address and size, which the SARA-2 incorporates into a buffer descriptor (BD) in its control memory.

Traffic Shaper

The SARA-2 contains a traffic shaper (traffic scheduler) which is used to speed up the process of searching the Rate Control Table and UBR circular list for candidate VCs to transmit cells; these searches for future candidates are done concurrently with segmentation. The RCT provides control over CBR and VBR VCs. The UBR circular (linked) list of segmentation UBR VC structures provides control over UBR VCs. For each CBR and VBR VC, the host establishes a VPI/VCI connection and assigns it to certain entries in the RCT. The traffic scheduler traverses the RCT, sequentially looking for VCs that are both active and have packets to send. Note that fields in a RCT entry may also indicate that the entry should be skipped or that idle cells should be inserted into the cell stream. When a candidate VC is found, the associated segmentation VC structure provides a pointer to a buffer descriptor for the host buffer to segment. A burst of cells (Burst_Size field in the segmentation VC structure) from this VC may be sent subject to data availability. If data is not available for CBR/VBR VCs, the available bandwidth is dynamically allocated to UBR VCs.

UBR Traffic Shaping

The UBR circular list is a circular linked list of segmentation VC structures. The traffic scheduler traverses the UBR circular list to identify the next UBR VC to serve. When a candidate is found, the traffic scheduler parks at that UBR VC until the next UBR opportunity; e.g., data is not available for the next CBR or VBR VC.

AAL5 CPCS-PDU Segmentation

This section describes the segmentation operation of SARA-2 using AAL5 as an example. Figure 3 shows the segmentation data flow.

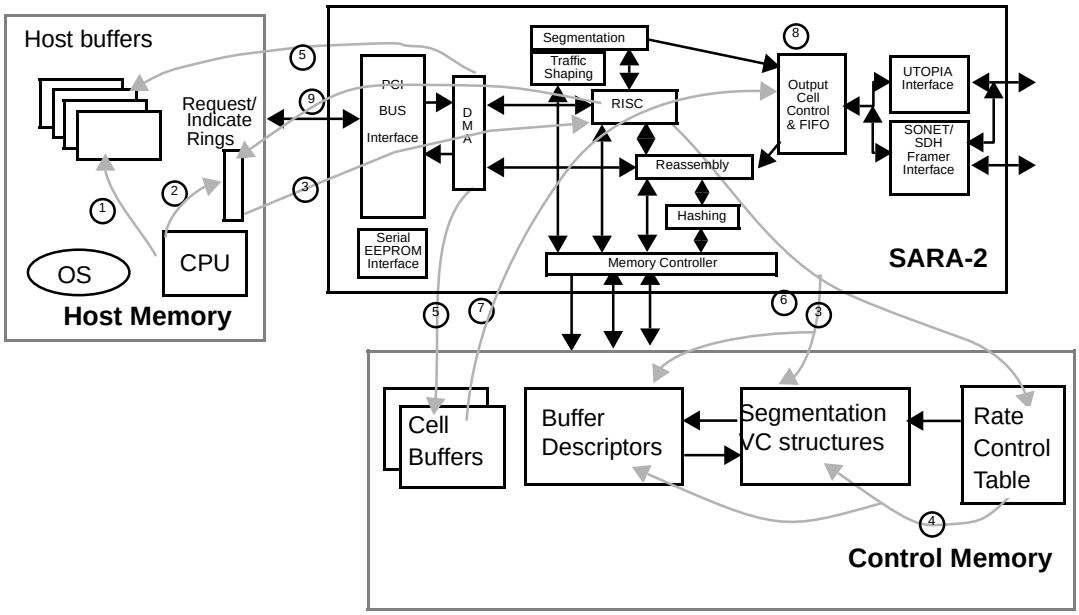


Figure 3. Segmentation Data Flow

The following numbered list describes the individual arcs shown in Figure 3.

1. The host CPU writes packets (CPCS-PDU payloads) that are to be segmented to buffers in host memory. A CPCS-PDU may be scattered among several host buffers.
2. As host buffers are filled with data, the host software generates a series of service interface request messages (one per host buffer). Each request message specifies the VC, buffer size and host memory address. The message also specifies whether the host buffer is associated with the last fragment of a CPCS-PDU.
3. The SARA-2 processes the request messages and adds the resulting buffer descriptors to a linked list pointed to by the segmentation VC structure. This linked list enables multiple host buffers on the same VC to be set up for segmentation.
4. When the traffic scheduler services the Rate Control Table (RCT), the Segmentation VC structures are retrieved. If the CURR_BUFF_DESCR in a Segmentation VC structure is NULL, then no data exists for the VC. Otherwise, if there are host buffers active for segmentation, the CURR_BUFF_DESCR provides a pointer to the linked list of buffer descriptors. Each buffer descriptor provides the address to access data in host memory.

5. The DMA controller makes a request on the PCI bus. Once the request is granted, the SARA-2 becomes a master on the PCI bus. The DMA controller also fetches a free cell buffer from the free cell buffer pool in SARA-2 control memory. The DMA controller fills the free cell buffer with data from the PCI memory, decrementing the size and incrementing the address fields of the buffer descriptor. If the data belongs to the last cell of a PDU, the DMA controller writes the specified number of padding bytes into the cell buffer and then copies the CPCS-PDU trailer.
6. The segmentation processing logic processes the AAL Specific Fields of the Segmentation VC structure and flags from the buffer descriptor to generate the AAL SAR-PDU header and trailer fields. The SARA-2 writes back to control memory the partial CRC, data address and data size fields, and updates the flags and cell count.
7. When the output cell FIFO can accept a cell, the output control logic retrieves the cell from the cell buffer to prepare it for transmission. The cell buffer is released to the free cell buffer pool.
8. In the UTOPIA mode, if the external interface is ready to accept a cell, the cell is sent out. If in the framer mode, the cell is mapped into the payload of the SONET/SDH frame and the framer adds the SONET/SDH overhead bytes.
9. When a CPCS-PDU is completely segmented, the SARA-2 sends a service interface indicate message, with or without an interrupt, releasing the buffers associated with the CPCS-PDU for re-use by the host.

Reassembly Operation

The SARA-2 continuously receives and reassembles ATM cells at up to 155 Mbit/s, supporting CBR, VBR and UBR traffic classes. Simultaneous reassembly of up to 64,000 VC's is supported with each VC specified as AAL1, AAL3/4 or AAL5. AAL0 or Raw cells, OAM cells and RM cells are also supported. When a VC is requested by the host software, the Reassembly VC structure and Hash Table are initialized by the microcode with the AAL type and the ATM cell header. The host software must provide the SARA-2 with a supply of host buffers which may be used for reassembly of CPCS-PDUs. Descriptors for these buffers are maintained by SARA-2 in a reassembly buffer pool. The reassembly control logic performs AAL-specific functions and reassembles the CPCS-PDU directly in host memory using a sophisticated scatter method that allows the use of multiple buffers to store an incoming CPCS-PDU (receive-buffer chaining). When a new CPCS-PDU arrives, or a buffer used to store cells from an incoming CPCS-PDU is filled, the device obtains an empty buffer from the reassembly buffer pool. When a CPCS-PDU is completely reassembled, the SARA-2 notifies the host with an indicate message. Figure 4 shows the reassembly data flow.

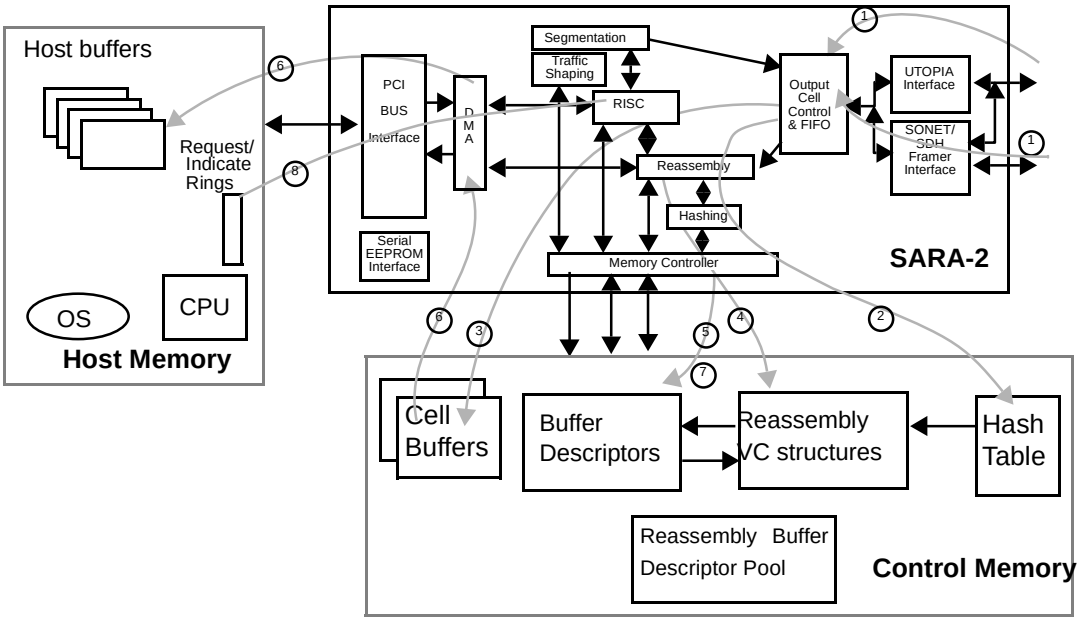


Figure 4. Reassembly Data Flow

AAL5 CPCS-PDU Reassembly

The following numbered list describes the individual arcs shown in Figure 4.

1. If the internal framer mode is used, the SARA-2 delineates cells after framing to the transmission format. If the UTOPIA mode is used, the SARA-2 receives complete 53-byte ATM cells.
2. The hash control logic processes the ATM cell header of the received cell to provide a hash table index. The hash table entry provides a pointer to the Reassembly VC structure corresponding to the ATM cell.
3. The SARA-2 fetches a free cell buffer and writes the cell to the control memory. This allows adequate system throughput even under delayed access to the PCI bus (due to usage of the PCI bus by other devices).
4. The Reassembly VC structure fields are read to determine the AAL type and obtain reassembly flags. The CLP and PTI fields of the incoming cell are also processed. AAL-specific functions are performed and the reassembly structure fields are updated.

5. The DMA controller gets a buffer descriptor pointer. If the reassembly VC has host buffers allocated to it, the VC structure points to an available buffer descriptor, and that BD is used. Otherwise, the SARA-2 fetches a new buffer descriptor from the reassembly buffer pool. If this is not the first cell of a CPCS-PDU, the SARA-2 reads the partial CRC information from the Reassembly VC structure as well.
6. The PCI bus interface makes a request to the PCI bus. When the bus request is granted, the DMA controller transfers the 48-byte AAL5 payload from the cell buffer to the host buffer, computing AAL5 CRC as the data is transferred. If the host buffer is filled, the current descriptor is appended to the end of the linked list of descriptors already used for this CPCS-PDU. The SARA-2 fetches a new descriptor from the reassembly buffer pool and continues with the transfer. The partial CRC is then written to the Reassembly VC structure. The cell buffer is then released to the free cell buffer pool.
7. When a cell has been transferred, the size and host buffer address in the buffer descriptor are updated. When the last cell of a CPCS-PDU is transferred, the AAL5 CRC and length fields are verified and errors, if any, flagged.
8. When the reassembly of a CPCS-PDU is complete, the SARA-2 sends an indicate message for each used buffer, with or without an interrupt, releasing the buffer(s) associated with the CPCS-PDU. The used buffer descriptors are copied to the indicate ring for host processing. The buffer descriptors are released for reuse.

LINE INTERFACE

The SARA-2 provides two different operating modes: byte-parallel UTOPIA mode and internal SONET/SDH framer mode, with the internal framer mode supporting both a byte-parallel interface and a bit-serial interface. In the byte-parallel framer mode interface, the framer shares leads with the UTOPIA interface. The UTOPIA mode is selected when lead UTOP/$\overline{\text{FMR}}$ is set high, and the SONET/SDH framer mode is selected when this lead is set low.

UTOPIA Mode

In the UTOPIA mode, the SARA-2 is designed to connect to several commercial devices: TranSwitch's CUBIT ATM switching device, a cell delineation device such as TranSwitch's CDB or other ATM UNI physical layer devices compliant to ATM Forum's UTOPIA Level 1 interface specification. The cell interface can be configured to be in the UTOPIA master mode (ATM) or UTOPIA slave mode (PHY) using the control bit CUP in Mode Register 2. The SARA-2 generates a separate reference clock using the SYSCLK lead for the UTOPIA interface. In the UTOPIA-ATM layer mode, this reference clock may be used to clock external devices. In the UTOPIA-PHY layer mode, an external clock source may be connected to separate clock inputs. The interface can also be configured to operate in cell level handshake mode or byte-level handshake mode using the control bit CHS in Mode Register 2. The device also supports a parity bit on the UTOPIA data bus. In the transmit direction, an odd parity is generated. In the receive direction, the SARA-2 internally computes parity over the data lines and compares with the received parity; if different, a parity error is signalled. In this mode, the HEC fields of all transmitted cells are set to zero, and HEC bytes in received cells are ignored.

Framer Operation

Interface and Format Supported

The SARA-2 device supports the STS-1 and the STS-3c/STM-1 framing formats. STS-1 operation is selected by writing 1 to control bit S52 in Mode Register 2 and the STS-3c/STM-1 format is selected by writing a 0 to this bit. For either format, the SARA-2 device provides either a byte-parallel or bit-serial SONET/SDH interface. The 155 Mbit/s ECL serial interface is selected by writing a 1 to control bit SFE in Mode Register 2. The selection configures the interface for both the receive and transmit directions. The byte-parallel interface, which operates at 19.44 Mbit/s, is selected by writing a 0 to control bit SFE.

Transport Overhead Bytes

For STS-1 operation, the following TOH bytes are supported. The transmitted values are also given.

A1	A2	C1
B1		
H1	H2	H3
B2		K2
	Z2(M1)	

f6	28	01
BIP-8	00	00
00	00	00
62	0a	00
BIP-8	00	00 Note 2
00	00	00
00	00	00
00	00	00
00	Rcv B2 errors	00

Note 1. The other TOH bytes in the STS-1 format, for example D1 to D12, are transmitted as a 00 hex.
Note 2. K2 is normally transmitted as 00 hex. A line RDI transmits a 06 hex in the K2 byte, while a line AIS transmits all ones in the line overhead and SPE bytes.

The following Transport Overhead bytes are supported in the STS-3c/STM-1 format.

A1	A1	A1	A2	A2	A2	C11	C12	C13
B1								
H1	H1*	H1*	H2	H2*	H2*	H3	H3	H3
B2	B2	B2				K2		
					Z23			

f6	f6	f6	28	28	28	01	02	03
BIP-8	00	00	00	00	00	00	00	00
00	00	00	00	00	00	00	00	00
Note 1	93	93	0a	ff	ff	00	00	00
BIP-24			00	00	00	Note 2	00	00
00	00	00	00	00	00	00	00	00
00	00	00	00	00	00	00	00	00
00	00	00	00	00	00	00	00	00
00	00	00	00	00	Rcv B2 errors	00	00	00

Note 1: Equal to 62 (size bits equal to 00 hex for STS-3c), or 6A (size bits equal to 10 hex for STM-1).
Note 2: Equal to 00 hex for no alarms, a line RDI transmits a 06 hex in the K2 byte, while a line AIS transmits all ones in the line overhead and SPE bytes.

PRODUCT PREVIEW

Framing:

The A1 and A2 bytes are allocated for framing. The A1 byte is set to F6 hex (11110110), and the A2 byte is set to 28 hex (00101000). In the receive direction, the A1 and A2 bytes are monitored for out of frame and loss of frame alignment. In addition, the signal is monitored for loss of signal. The receive framing circuit meets the ANSI/Bellcore/ITU requirements for frame alignment, including the requirement that a Bit Error Rate (BER) of 10^{-3}, assuming a Poisson distribution, will not cause an Out Of Frame alarm once every six minutes. An internal framing circuit is enabled for both the serial and parallel modes. An external framing pulse is not required for establishing byte boundaries when the parallel mode is selected.

B1 Byte:

The B1 byte is assigned to carry a BIP-8 even parity indication. The receive and transmit value of the BIP-8 parity is calculated by performing a modulo-2 sum, column-by-column, of all of the bytes of the Transport Overhead and the payload bytes of a frame prior to unscrambling. In the receive direction, the results are added, modulo-2, to the value received in the B1 byte in the frame that immediately follows after unscrambling. Each non-zero bit position of the sum is one BIP-8 B1 bit error. The number of BIP-8 B1 bits found to be in error (one to eight) is counted in the B1 byte 16-bit performance counter. This counter is accessed via a Service Interface request (using Request Primitive "Get Stats"), as described in the SARA-*Lite* Service Interface Technical Manual, which may be requested from TranSwitch Marketing Department (TXC-05551-TM1).

Scrambling and Descrambling:

The scrambler/descrambler is always enabled. Excluding the A1, A2, and C1 bytes, the remaining bytes in the format are scrambled/descrambled. The scrambler/descrambler uses the generating polynomial $1 + x^6 + x^7$ and resets to 1111111 on the most significant bit (MSB) of the byte following the C1 byte.

Pointer Tracking:

The pointer tracking state machine determines the starting location of the J1 byte in the Path Overhead by processing the pointer value carried in the H1/H2 pointer bytes. The pointer tracking state machine uses the latest state machine specified by ITU and Bellcore. For example, a pointer offset of 0 indicates that, in STS-1, the SPE (POH and payload bytes) starts in the byte location that immediately follows the H3 byte (pointer action byte). Two alarm indications are provided: path AIS and Loss Of Pointer. Path AIS is an all ones signal that is carried in the H1/H2 bytes and the SPE to indicate a failure mode. Writing a 1 to control bit SSEN will transmit the size bits in the H1 byte as 10 for STM-1 operation, and will declare LOP if the received size bits are not equal to 10. When SSEN is 0, the size bits in the H1 byte will be transmitted as 00, and will be ignored in the received signal.

Pointer Generation:

The H1/H2 bytes are transmitted as 62/0A hex (0110 00 1000001010) for the STS-1 format. This is equivalent to a disabled NDF (0110), size bits set to 00, and an offset value of 522, as indicated by the 4-2-10 bit grouping shown above. For the STS-3c format the H1/H2 bytes are also transmitted as 62/0A hex (0110 00 1000001010). For the STM-1 signal, the transmitted H1/H2 bytes are equal to 6A/0A hex (0110 10 100001010). This is equivalent to a disabled NDF, size bits set to 10, and an offset value of 522.

B2 Byte Processing:

The B2 byte is assigned to carry a BIP-8 even parity indication. The received value of the BIP-8 parity is calculated by performing a modulo-2 sum, column-by-column, of all of the bytes of the Line Overhead and the payload bytes of a frame prior to unscrambling. This result is added, modulo-2, to the value received in the B2 byte in the frame that immediately follows. Each non-zero bit position of the sum is one BIP-8 B2 bit error. The number of BIP-8 B2 bits found to be in error (one to eight for STS-1, one to twenty four for STS-3c/STM-1) is counted in the B2 byte 16-bit performance counter. This counter is accessed via a Service Interface request (using Request Primitive "Get Stats"), as described in the SARA-*Lite* Service Interface Technical Manual, which may be requested from TranSwitch Marketing Department (TXC-05551-TM1).

K2 Byte:

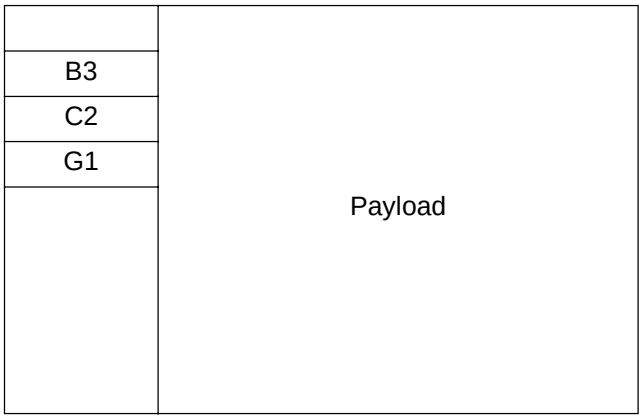
Two alarm indications are carried in the K2 byte, Line AIS and Line RDI. The other bits in the K1 and K2 bytes are ignored. A Line AIS alarm is declared when bits 6, 7, and 8 are 111 for five consecutive frames. Recovery occurs when bits 6, 7, and 8 have any pattern other then 111 for five consecutive frames. A Line RDI alarm is declared when bits 6, 7, and 8 are 110 for five consecutive frames. Recovery occurs when bits 6, 7, and 8 have any pattern other then 110 for five consecutive frames. These alarms are accessed via a Service Interface request (using Request Primitive "Get Stats"), as described in the SARA-*Lite* Service Interface Technical Manual, which may be requested from TranSwitch Marketing Department (TXC-05551-TM1).

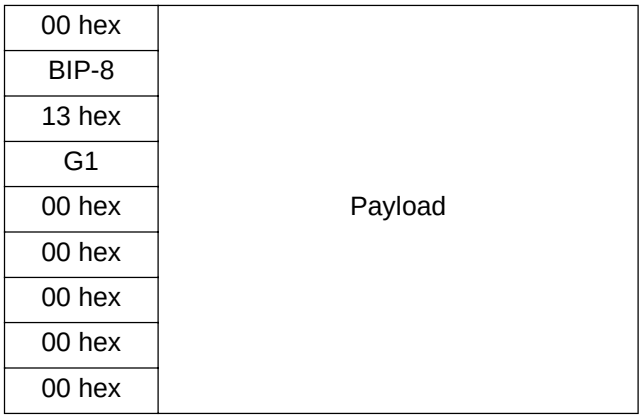
Z2 Byte:

Receive line FEBE processing consists of counting the number of errors carried in bits 5 through 8 in the Z2 byte. The number of errors is encoded in binary format. Line FEBE count is equal to the binary value of the B2 BIP-8 (STS-1) or BIP-24 (STS-3c/STM-1) errors detected at the far-end receiver. The number of received errors is counted in a 16-bit counter. This counter is accessed via a Service Interface request (using Request Primitive "Get Stats"), as described in the SARA-*Lite* Service Interface Technical Manual, which may be requested from TranSwitch Marketing Department (TXC-05551-TM1).

Path Overhead Bytes

The STS-1 SPE consists of 87 columns by 9 rows, which is further broken down into one column of POH bytes and 86 columns of payload. The STS-3c SPE and STM-1 VC-4 consists of 261 columns by 9 rows, which is further broken down into one column of POH bytes and 260 columns of payload. The placement of POH bytes in the SPE or VC-4 is shown below:





Notes: B3 value depends on payload contents.
G1 value depends on incoming parity errors and RDI states

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B3 Byte:

For the STS-3c/ STM-1 format, B3 parity calculation is performed over the 261 columns of the payload and POH bytes, while for the STS-1 format, the B3 parity error calculation is performed over 87 columns of the payload and POH bytes. The B3 calculation is performed as the per-column modulo-2 sum of the bytes of the payload and POH bytes. The calculated value is compared against the received B3 byte in frame n+1. Each non-zero bit, when each of the columns are compared, corresponds to one observed B3 bit error count. The error count is counted in a 16-bit performance counter. This counter is accessed via a Service Interface request (using Request Primitive "Get Stats"), as described in the SARA-*Lite* Service Interface Technical Manual, which may be requested from TranSwitch Marketing Department (TXC-05551-TM1).

C2 Signal Label:

The received C2 byte value is checked for a mismatch, and for unequipped status. The received C2 value is compared against the value of 13 hex. A Signal Label Mismatch alarm occurs when the received C2 byte differs from the 13 hex value five times in succession, provided the alarms specified earlier have not occurred, and unequipped status (00 hex) has not been detected. The mismatch alarm is exited when five consecutive correct C2 values (as compared against the 13 hex value) are received.

An Unequipped status alarm occurs when the received C2 byte is equal to all-zeros for 5 consecutive frames. The Unequipped status alarm is exited when five consecutive non-zero C2 values are received.

The C2 byte is transmitted with a fixed value of 13 hex (0001 0011).

G1 Byte:

The first four bits in the G1 byte are assigned for FEBE (Far End Block Errors). Received FEBE values within the range 1 to 8, inclusive, are added to the current value of the FEBE 16-bit counter. Any received value equal to 0, or between 9 and 15, is treated as a zero error count, and no accumulation will result.

Bits 5, 6, and 7 in the G1 byte are monitored for RDI and enhanced RDI. Enhanced RDI allows three types of remote defect indications to be detected: payload, connectivity, and server. The following table reflects the possible states associated with RDI:

Bit 5	Bit 6	Bit 7	Interpretation
0	0	0	No defect indication
0	0	1	No defect indication
0	1	0	Remote Payload Defect
0	1	1	No defect indication
1	0	0	Remote defect indication
1	0	1	Remote Server Defect
1	1	0	Remote Connectivity Defect
1	1	1	Remote defect indication

These states must be detected for five consecutive frames before the interpretation is indicated. These bits are accessed via a Service Interface request (using Request Primitive "Get Stats"), as described in the SARA-*Lite* Service Interface Technical Manual, which may be requested from TranSwitch Marketing Department (TXC-05551-TM1).

SONET/SDH Tests

The framer has the ability to loop back the transmit interface data output to the receive interface data input, force path errors and perform other tests. These Capabilities must be accessed through the Service Interface.

Cell Delineation

The cell delineation block frames to the ATM cell boundaries using the HEC field found in the cell header. The cell delineation is performed according to the ITU I.432 specification. The block detects out of cell delineation (OCD) and, if the OCD state persists for 4 ms, loss of cell delineation (LCD) alarm is declared. LCD is removed when no OCD condition has been detected for 4 ms. Once cell delineation is achieved, incoming cells with no HEC errors are passed into the cell FIFO for reassembly processing. In addition, if the control bit HCS is set, single bit errors are corrected. If the HCS bit is set to 0, single bit errored cells are also discarded. In either case, multi-bit errored cells are always discarded. Using firmware, counters may be maintained to accumulate corrected HEC errors and uncorrectable HEC errors.

In the transmit direction, the SARA-2 generates the correct HEC field for both data cells and null cells used for cell rate decoupling. If the control bit HCD is set to a 1, the HEC coset is not X-ORed to the CRC. If the FHC bit is set, the contents of FRPATN register are X-ORed into the result of the HEC calculation. This allows arbitrary errors to be introduced into the HEC field for test purposes. These control and alarm fields are accessed via a Service Interface request (using Request Primitive "Get Stats"), as described in the SARA-*Lite* Service Interface Technical Manual, which may be requested from TranSwitch Marketing Department (TXC-05551-TM1).

Cell Rate Decoupling

The SARA-2 performs cell rate decoupling by discarding unassigned or idle cells received from the line if the control bit NLD is set to 1. It is also possible to discard all cells with cell loss priority 1 by setting the control bit C1D in Mode Register 1. In the transmit direction, if there are no data cells the device generates idle cells to perform cell rate decoupling.

Cell Payload Scrambling and Descrambling

In the receive direction, the SARA-2 implements a self-synchronous descrambler on the 48-byte cell payload using the $x^{43} + 1$ polynomial. The descrambler is disabled for the duration of the cell header. In the transmit direction, the SARA-2 scrambles the cell payload.

THE ATM COMMUNICATIONS PROCESSOR (ACP)

The SARA-2 device includes a powerful RISC processor core called the *ATM Communications Processor (ACP)*. The ACP executes up to 50 million instructions per second, allowing it to perform many of the application-specific protocol functions in firmware rather than hardware. The complete ACP firmware module is supplied by TranSwitch and is loaded into SARA-2 RAM by the host CPU during the device initialization process. The ACP communicates with the remainder of the SARA-2 through on-chip queues and device registers which are address-mapped into the core register set to permit fast, low-overhead access. The ACP has been optimized for high performance processing of ATM applications. Although it is not necessary for the SARA-2 user to program the ACP or to understand the details of its design, this section provides an overview of its architecture so that the user may better understand the overall SARA-2 architecture and the role played by the ACP.

ACP Architecture

The high level architecture of the ACP is shown in Figure 5. The major functional units are: the I-Cache Unit, the I-Fetch Unit, the RALU, the Load Unit, and the MicroControl Unit. The I-Cache Unit includes two distinct instruction sources: a 2560-location instruction RAM (IRAM) and a 512-location two-way set-associative instruction cache (ICACHE). The IRAM is initialized at reset by the host CPU, while the ICACHE is auto-loaded from the SARA-2 control memory following a cache miss. Real-time critical code is located in the IRAM while initialization code, error recovery code and other non-critical code is cached as needed. The ACP supports a 24-bit external (control) memory address space. The lower 64k bytes of the SARA-2 control memory address space are allocated to instruction storage. This is more than sufficient for code expansion and eliminates risk of corruption by control memory data access. Instructions are 32 bits and are broadcast to the other units for local decoding.

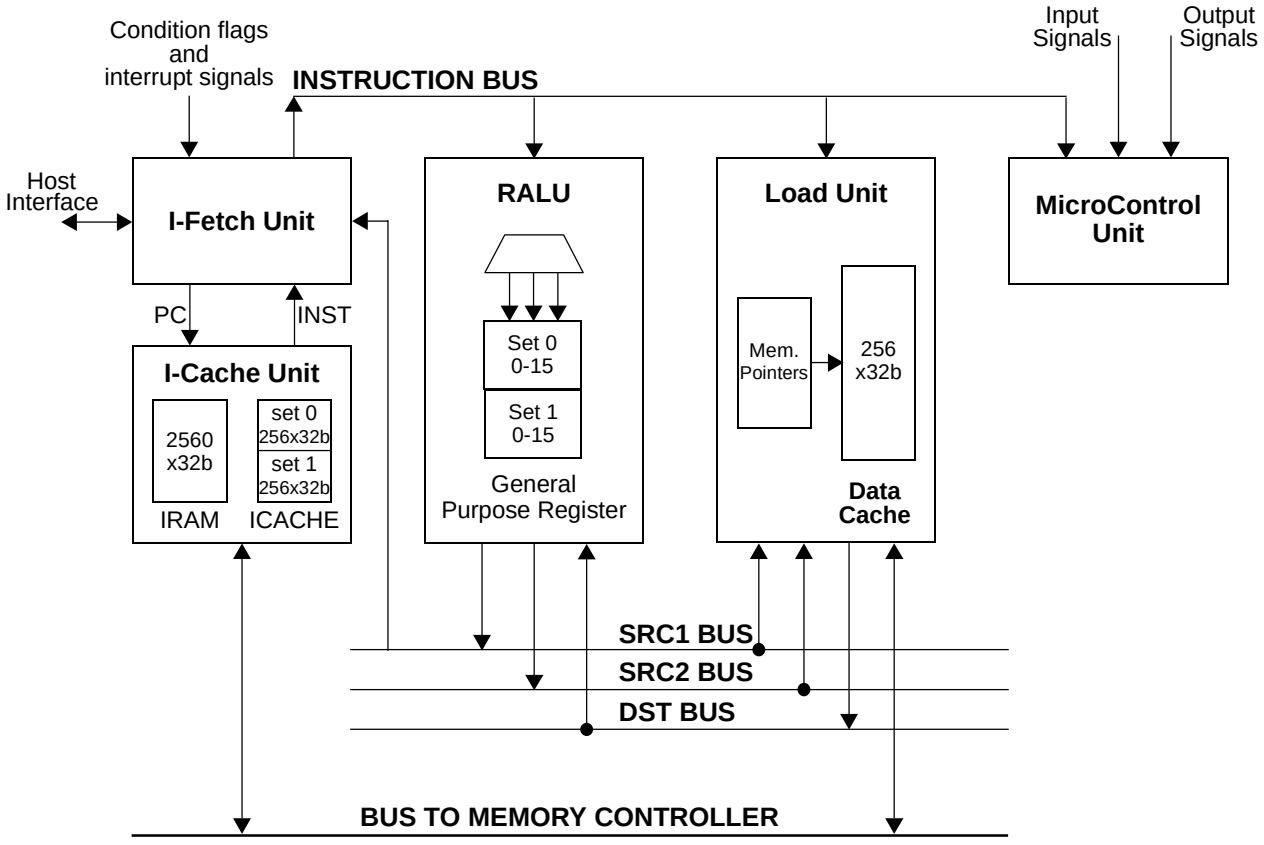

Figure 5. ACP RISC Core Architecture

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The I-Fetch Unit is responsible for instruction sequencing. During normal execution, the I-Fetch control can test condition codes it receives from the RALU or elsewhere in the device. Many of the real-time tasks are interrupt-driven to meet the critical response time requirements. Accordingly, the ACP implements a fast, but flexible, interrupt handler. Each interrupt source can be independently masked under microcode control; priority is also assigned to each source. When the I-Fetch Unit recognizes an interrupt, control is transferred to a dedicated interrupt vector. At the interrupt vector location, the program then jumps to the *interrupt handler*. The location and function of the interrupt handlers are programmable. To enable fast context-switching, some ACP registers, including the entire general-purpose register file, are shadowed.

The RALU includes a general-purpose register file and a full-function Arithmetic and Logic Unit (ALU). The data path is 16 bits. Support for 32-bit operations is provided, although 32-bit operations are far less common. The register file is partitioned into two 16-location banks. Interrupts, as noted above, automatically switch context between the two banks, but context can also be switched under program control. The register file is three-ported, pipelined and includes forwarding logic so that updated registers are always available in the next cycle. The ALU functions typically operate on two register source operands to create one register destination. The register sources and destinations available include not only the general-purpose register file but 32 *special registers* located elsewhere in the ACP and 96 *control registers* located in the SARA-2 outside the ACP. The special register group includes control memory pointers, real-time clocks and interrupt support registers. The control group includes the queues, status registers and control signals through which the ACP interacts with and controls the SARA-2. Through careful performance optimization and the use of a 16-bit data path, the RALU can operate on direct-mapped control registers without incurring any delay cycles or hardware interlocks.

The ALU implements the full complement of standard RISC operations; however, it also provides a number of functions specialized to ATM processing. Among the latter are hardware support for the floating point operations used in the UBR rate calculations.

The traffic rate parameters and other software counters are processed on-chip by the RALU. For this reason, the Load Unit includes a 256 x 32-bit direct-mapped data cache and implements a simple, but powerful, set of load/store operations between memory and the general-purpose registers or special registers. In the case of *load*, a selected register (general-purpose or special) is loaded with data from an arbitrary 24-bit control memory address. All memory addresses use *base/displacement* mode; that is, they are computed as the sum of a memory pointer stored in the Load Unit and an offset which may be encoded in the instruction or located in a general-purpose register. This mode is particularly well-suited to the many table look-ups required by the SARA-2 firmware. Memory addresses can be 8b, 16b or 32b. Although the RALU datapath is 16-bit, control memory transfer of 32-bit register pairs is supported to conserve control memory bandwidth. Data is automatically aligned. If the addressed location is resident on-chip, there is a “cache hit” and the data is transferred from the cache to the RALU; upon cache-miss a pipeline stall is entered, followed by load of the cache and RALU from control memory. Similar operations occur in the case of the store.

Several performance optimizations are included. Uncached loads (and stores) are permitted so that, for instance, active cached blocks need not be replaced in the case of an isolated table lookup. A burst buffer is also included in the Load Unit so that a block of data can be packed for transfer.

The MicroControl Unit complements the assembly language operations of the ACP with low-level *microcontrol instructions* optimized for the ACP function in the SARA-2. The microcontrol instructions are used to toggle signals controlling blocks peripheral to the ACP and also to test local combinations of inputs from the peripherals. Either of these operations could be implemented with a conventional sequence of move, mask and test or set operations; however, the Microcontrol Unit provides needed efficiency.

ACP Functions

The ACP is responsible for the following functions in the SARA-2:

1. *Maintenance of host messaging interface:* Much of the interaction with the host system, including the maintenance of request/indicate rings and the processing of messages, is performed in ACP firmware.
2. *ATM/AAL Protocol processing*: Much of the service-specific portion of the adaptation layer is implemented via firmware running on the ACP. In addition, the maintenance of statistics and the checking of errors in the ATM layer are also performed by the ACP.
3. *Buffer management*: The ACP is responsible for high-level buffer management: for example, the firmware is used to recover from temporary host bus blockages.
4. *Handling of signaling and OAM flows*: The host messaging system provides a service interface whereby signaling and OAM cell flows can be passed to the host for processing, and accepted from the host for insertion into the outgoing cell stream.
5. *Virtual circuit setup and removal*: While the host CPU is expected to use the signaling facilities to negotiate for and create virtual connections, firmware running on the ACP can set up and remove the state structures corresponding to those connections.

DMA CONTROLLER

The DMA controller works in conjunction with the PCI interface to facilitate data transfer to and from the SARA-2. The DMA Controller also permits internal firmware to read and write general data items (e.g., data blocks, control structures, etc.) from and to the host memory. These transfers take place independently of the cell processing tasks, and run at the lowest priority to ensure that cell transfer is not interrupted. Two transfers (one incoming for received data, one outgoing for transmitted data) are concurrently supported by the DMA Controller. The transfers are multiplexed at the burst level to ensure minimum latency on the PCI host bus.

The DMA Controller is controlled by the ACP, but performs its tasks independently of the ACP activities, and uses separate memory access channels to reduce the impact of DMA transfers on firmware processing. Firmware on the ACP can cause the DMA Controller to transfer cell payloads to or from the PCI host memory simply by writing or reading cell buffer pointers to the dedicated DMA Controller buffer pointer queues. The DMA Controller reports data flow conditions (e.g., full or empty host buffers) by placing descriptor or buffer pointers into a separate service queue.

The DMA Controller incorporates very powerful and general scatter-gather algorithms, using chains of linked *buffer descriptors* to describe the locations of arbitrarily-sized blocks of transmit or receive data placed on arbitrary byte boundaries within the host memory. It is capable of dealing with fragmented and incomplete AAL PDUs in an efficient manner. The DMA Controller is also responsible for computing the standard AAL5 32-bit CRC when performing an incoming or outgoing transfer.

TRAFFIC SHAPING

The Traffic Shaping block is a traffic scheduler, which is responsible for segmenting AAL Protocol Data Units (PDUs) and rate shaping outgoing cell streams on a per-virtual-circuit basis using a mixture of Constant Bit Rate (CBR), Variable Bit Rate (VBR) and Unspecified Bit Rate (UBR) traffic models for the ALL0, AAL1, AAL3/4 and AAL5 protocols. It carries out segmentation and rate control using the Rate Control Table (RCT) and the UBR circular list. The traffic scheduler autonomously traverses the RCT and the UBR circular list and selects candidate virtual circuits for segmentation. The RISC core may dynamically update the data structures used by the traffic scheduler without interfering with traffic scheduler operation, allowing for the efficient chaining of payloads.

The traffic scheduler separates and prioritizes CBR/VBR (i.e., time-sensitive) traffic and UBR (i.e., low-priority, time-insensitive) traffic. This maximizes the probability that CBR latency and bandwidth guarantees will be met. In addition, the transmit UBR circular list mechanism ensures fairness among multiple UBR virtual circuits, prevents low-bandwidth UBR channels from blocking high-bandwidth channels, and provides a timer-controlled segmentation mechanism for supporting flow control of individual UBR VCs in an efficient manner.

The traffic scheduler can automatically compensate for delays in transmitted CBR traffic introduced by short periods of overload on the host bus. If access to the host bus is blocked for a time long enough to drain the transmit buffers, the framer interface will automatically begin rate decoupling by inserting NULL cells into the outgoing stream. When the blockage clears, the traffic scheduler attempts to compensate for the lost CBR cell slots by skipping over CBR entries in the RCT until the CBR stream is again aligned properly.

MEMORY CONTROLLER

A control memory is required by the SARA-2 to hold data structures needed to perform segmentation and reassembly, virtual circuit control, host communications, etc., as well as cell buffers for transmit and receive cells. The SARA-2 integrates a complete memory controller to support this control memory.

The memory controller directly addresses up to 16,777,216 bytes of control memory. In addition, internal address decoding logic provides four pre-decoded chip select outputs that divide the memory space into four banks of 4 megabytes each. The memory controller uses a 32-bit memory datapath width and special phase-locked-loop (PLL) clocking and delay compensation mechanisms to allow it to sustain up to 200 Mbit/s of transfer bandwidth to high-speed SRAM devices.

PCI INTERFACE

The SARA-2 contains an integrated 32-bit PCI interface for transferring data and control information. The PCI bus interface in the SARA-2 is compliant with the PCI Local Bus Specification version 2.1. The device implements a complete master/slave interface between the SARA-2 internal control logic and the external host. When the SARA-2 is the master, the bus interface block uses burst DMA cycles to read or write data from the PCI bus. When the SARA-2 is the slave, the bus interface block allows the PCI host to access the SARA-2 internal registers and the control memory.

Communication between the host and the SARA-2 is also possible using a set of request/indicate rings in the host memory. Each ring has two priorities. Messages with the higher priority will be served first. A number of operational and failure conditions can be reported to the host processor via interrupts, multiplexed onto a single PCI bus interrupt line. A control register permits masking (i.e., disabling) of different interrupt conditions on an individual basis. A status register allows the host to obtain all key operational status conditions using a single register read. The PCI bus master and slave interface incorporate several FIFO buffers to allow masking of latency and significant improvement in throughput.

PCI Bus Master

The control logic of SARA-2 is responsible for accepting read and write commands from the DMA controller and in turn acquiring mastership of the PCI bus and generating transactions to perform the actual data transfers. The PCI bus master control logic contains logic required to support arbitration on the PCI bus. The arbitration priority scheme implemented by a system may be fixed, rotational, or custom. The arbitration latency is a function of the system, not the SARA-2.

A set of read, write and command FIFO buffers are implemented to enable burst writes and reads, as well as to decouple the SYSCLK from the PCICLK. To guarantee that the bus master does not reduce the efficiency of transfers on the PCI bus, the PCI bus master logic will always ensure, before beginning a transaction, that free space is available for a PCI bus read transaction and that FIFO data are available to be sent on the PCI bus for a write transaction. The maximum number of wait states introduced before the assertion of $\overline{\text{IRDY}}$ by the master

after the address cycle or turnaround cycle is one cycle of PCICLK. The SARA-2 uses a 16-word write command/data FIFO, a 4-word read command FIFO and a 16-word read data FIFO to insulate the DMA Controller from bus access latencies.

The PCI bus specification permits devices to perform burst transfers of unspecified length for maximum efficiency, limited only by the latency timer in the master device. To allow low-latency multiplexing of read and write transfers, the PCI bus master logic breaks up long read or write bursts. To prevent a long read burst from excessively increasing the write latency (or vice versa), the bus master logic implements a software configurable maximum burst length counter. The burst counter is started at the beginning of each read or write burst transaction, and counts the actual number of words transferred during the burst; when the burst counter reaches the limit, the burst is terminated and a new burst with an associated address phase is begun. The maximum number of words that can be transferred in a single transaction by the PCI bus master logic can be set to a value between 1 and 255.

To reduce overhead on the PCI bus, the control logic implements a merge operation allowing a new read or write sequence to be a continuation of the currently running bus transaction, effectively extending the previously started transaction and eliminating the need to supply a new address.

PCI Bus Slave

The PCI slave control logic allows external PCI bus masters to access on-chip control/status registers and control memory data structures, and also to read and write the PCI configuration registers. This allows the host software to configure, control and poll the SARA-2, and to communicate with firmware running on the ACP RISC core. The PCI slave logic also implements read and write FIFO buffers that interface between the slave control logic and DMA controller and internal registers. The FIFO buffers allow burst writes and reads to be performed from the PCI bus to the local memory or on-chip registers, and they also decouple the SYSCLK from the PCI bus clock. The FIFOs speed up burst reads and writes performed by the master to the local resources by buffering read addresses and prefetched read data and absorbing latency during consecutive writes. The SARA-2 PCI bus slave logic uses a 4-word write command/data FIFO, and an 8-word read command FIFO. These two slave FIFOs permit the host interface to implement a write-behind/fetch-ahead behavior: memory write commands are buffered and memory read data words are prefetched to hide memory access latencies.

The PCI slave unit can be used to access the on-chip device debug resources, which supports efficient system testing and device debug. The RISC core, DMA Controller and Link Controller can be easily halted and restarted using bits in the host interface control registers.

Serial EEPROM Interface

After a PCI reset, the SARA-2 can be configured for a specific application by downloading device set-up information from an external serial EEPROM into the device configuration registers, as shown in Figure 10. The SARA-2 can also be used in a default configuration, with no external EEPROM device. Reset values for the user-definable PCI configuration registers are shown in Figure 10.

Immediately after the deassertion of the PCI reset signal, if the $\overline{\text{EPS}}$ pin is tied low, the initialization procedure must be started. Configuration accesses by the host CPU to the SARA-2 must produce PCI bus wait states until the SARA-2 finishes downloading all configuration information from the serial EEPROM. If the Vendor ID obtained from the EEPROM is FFFF hex the default configuration must be used. Otherwise it would violate the PCI specification, which stipulates that a Vendor ID value of FFFF hex is illegal.

Data Alignment

The bus master data path contains byte rotate/merge logic to allow it to perform the required byte alignment on the data latched from (or written to) the PCI bus before it is written to the read data FIFO (or read from the write data FIFO). Byte swapping control logic is also implemented to facilitate Big-Endian or Little-Endian host buffer formats. In slave mode, the format is Little-Endian.

PCI Bus Performance

The performance of the PCI bus, in general, is a function of a number of system parameters. The performance metrics are latency and maximum sustained bandwidth. Please refer to Figures 6 and 7 for the timing of the read and write operations.

Target Initial Latency: The number of clocks from the assertion of $\overline{\text{FRAME}}$ to complete the initial data phase by either asserting $\overline{\text{TRDY}}$, or asserting $\overline{\text{STOP}}$ in the Retry and Target-Abort cases. Furthermore, all targets are required to complete the initial data phase of a read or write transaction within 16 clocks from the assertion of $\overline{\text{FRAME}}$.

Target Subsequent Latency: The number of clocks from the completion of a data phase ($\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are both asserted) to the assertion of $\overline{\text{TRDY}}$ or $\overline{\text{STOP}}$ for the next data phase should be within 8 clocks.

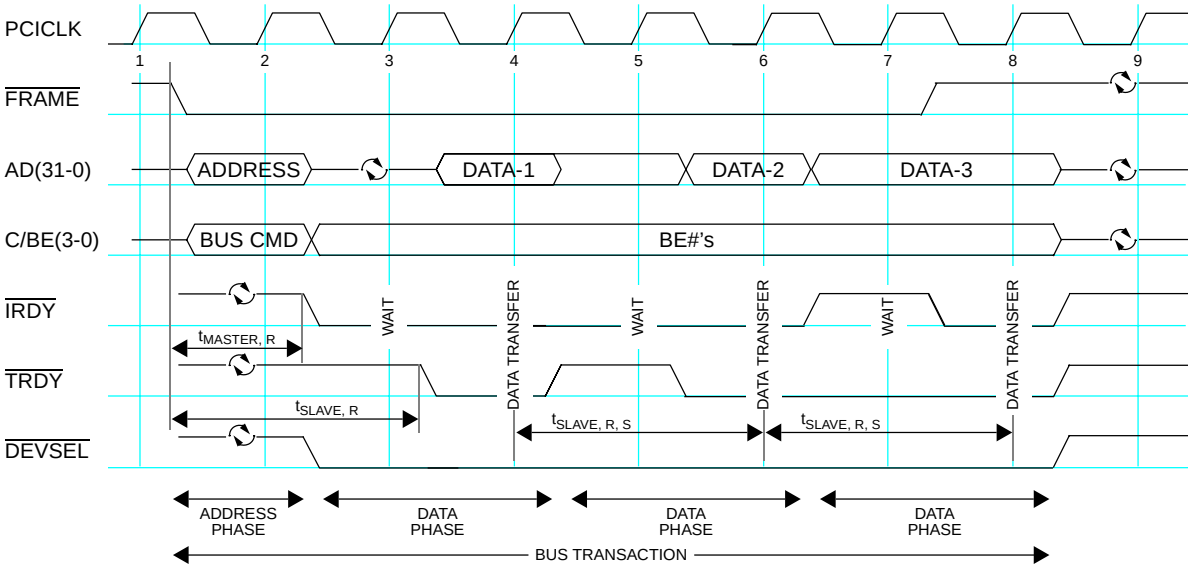
Master Data Latency: The number of clocks the master takes to indicate that it is ready to transfer data via the assertion of $\overline{\text{IRDY}}$. $\overline{\text{IRDY}}$ must be asserted within eight clock cycles from the assertion of $\overline{\text{FRAME}}$ on the initial data phase and within eight clocks on all subsequent data phases. This applies to all bus masters.

Maximum Sustained Bandwidth: The maximum sustained bandwidth figures shown in Figures 8 and 9 assume that a long sequence of reads or writes is performed and that the address, idle and turnaround phases can therefore be neglected. The slave burst write assumes that flow control is used once the internal FIFO fills up (otherwise the maximum sustained bandwidth is 1 cycle per word).

Figures 8 and 9 give the performance of the PCI interface under the following assumptions:

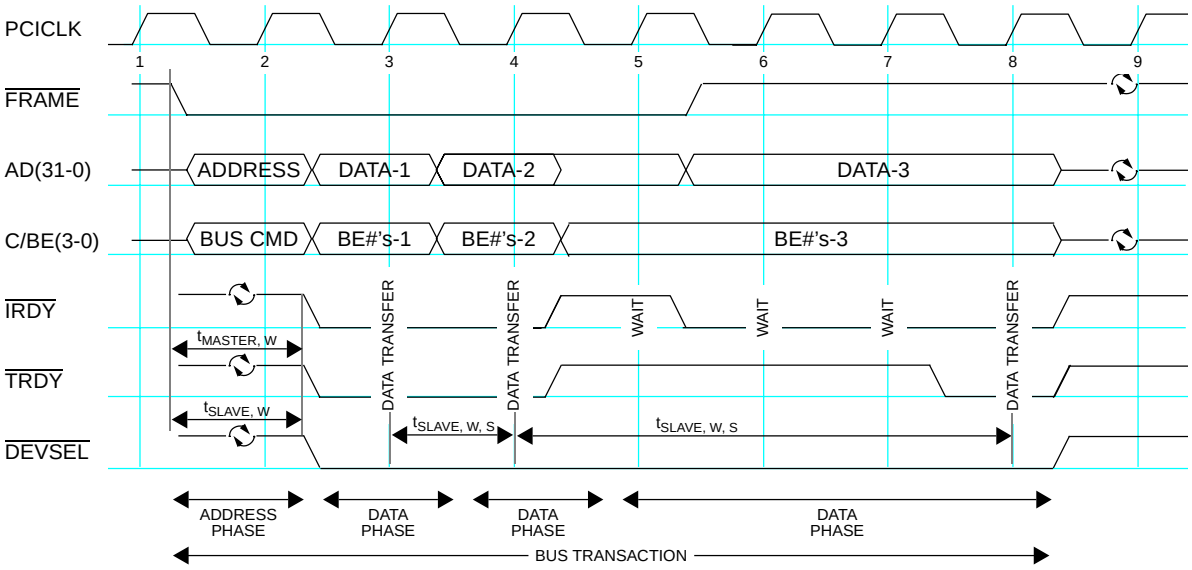
- PCICLK is 33 MHz and SYSCLK is 50 MHz
- PCI bus arbitration delay is assumed to be zero. If the arbiter parks the bus with the master that initiated the last transaction, the arbitration delay for that master is zero for the subsequent transaction. Otherwise, the additional delay required to obtain access to the bus must be factored into the performance calculation.
- The SARA-2 PCI bus master is assumed to be idle at the time the DMA controller initiates a transaction. Otherwise, the time to complete the last transaction must be factored into the latency calculations.
- When the SARA-2 acts as a bus master, it is assumed that the addressed target responds in one clock cycle.
- All addresses are aligned to a word boundary. When the SARA-2 acts as a bus master, an unaligned burst transaction will be broken up into unaligned and word-aligned data transfers, resulting in a maximum of two additional data phases beyond that required for transferring the same amount of word-aligned data. When the SARA-2 acts as a slave, if the burst transaction initiated by the external bus master is unaligned, the SARA-2 transfers a single word and then signals a target disconnect. This forces the external master to break up the unaligned burst into a sequence of single-word transfers.

Figure 6. PCI Bus Read Operation



Notes:
$t_{MASTER, R}$ is the master data latency time in the read operation.
$t_{SLAVE, R}$ is the target initial latency time in the read operation.
$t_{SLAVE, R, S}$ is the target subsequent latency time in the read operation.

Figure 7. PCI Bus Write Operation



Notes:
$t_{MASTER, W}$ is the master data latency time in the write operation.
$t_{SLAVE, W}$ is the target initial latency time in the write operation.
$t_{SLAVE, W, S}$ is the target subsequent latency time in the write operation.

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Transaction Type	Maximum Latency in PCICLK cycles		Maximum Sustained Bandwidth
	Master Initial Latency	Master Subsequent Latency	
Burst Read	TBD	TBD	1 word / cycle
Burst Write	TBD	TBD	1 word / cycle

Figure 8. PCI Bus Master Performance

Transaction Type	Maximum Latency in PCICLK cycles		Maximum Sustained Bandwidth	Comment
	Target Initial Latency	Target Subsequent Latency		
Single-word Read	TBD	N/A	N/A	Includes all address and idle phases
Single-word Write	TBD	N/A	N/A	Includes all address and idle phases
Burst Read	TBD	TBD	1 word / 1.2 cycles	Sustained rate excludes address/idle
Burst Write	TBD	TBD	1 word / 1.2 cycles	Sustained rate excludes address/idle

Figure 9. PCI Bus Slave Performance

PCI Configuration Register Descriptions

The initial registers in the table of Figure 10 constitute the 256-byte PCI configuration space header, organized as 64 32-bit registers. The following device-specific registers are accessed when the PCI interface is a target and a configuration cycle is in progress. These registers can be used by the host processor to initialize, control and monitor the PCI bus interface logic. Figure 10 shows the entries that may be configurable by the user when using an external serial EEPROM connected to the SARA-2. On power-up reset, the SARA-2 uploads the registers that can be modified by the user from the serial EEPROM if a low is applied to the $\overline{\text{EPS}}$ input.

Byte 0 Address (Note 1)	Configuration Register Definition (bits 31 - 0)				Reset Value	EEPROM Loadable?
	Byte 3	Byte 2	Byte 1	Byte 0		
0x00	Device ID		Vendor ID		0x15AF128B	yes
0x04	Status		Command		0x00800000	
0x08	Class Code			Revision ID	0x02030001	yes
0x0C	BIST	Header Type	Latency Timer	Cache Line Size (unused)	0x00000000	Byte 1 only
0x10	Local Memory Base Address				0x00000008	Byte 3 only
0x14 0x38	Unused				0x00000000	
0x3C	Max_Lat	Min_GNT	Interrupt Lead	Interrupt Line	0x00030100	Bytes 3, 2, 0 only
0x40	0x000000 (22 bits)	MError (1 bit)	MRd (1 bit)	Max Burst Len		Byte 0 only
0x44	Current Master Read Address					
0x48	Current Master Write Address					
0x52 0x7C	Unused				0x00000000	

Notes
1. Addresses 0x00 - 0x3F are the PCI configuration space header.
   Addresses 0x40 - 0x7F are device-specific registers.
2. The SARA-2 outputs addresses 0x00 - 0x43 on its serial EEPROM interface. The address that is output by the SARA-2 directly corresponds to the PCI configuration space register that is to be loaded. If the address is that of a non-EEPROM loadable register then the corresponding data from the serial EEPROM is ignored.
3. Bits 0 and 1 of address 0x42 are test bits. They must be written to 0 if the address is written.

Figure 10. PCI Configuration Space

The following describes the individual fields in the PCI Configuration space - the reset values are shown above:

Device ID: 16-bit device identification of SARA-2 (05551 = 0x15AF)

Vendor ID: 16-bit PCI vendor identifier code allocated by the PCI SIG (0x128B)

Status: This 16-bit register contains the PCI status information. All of the implemented status bits are latched. To clear a bit, a 1 should be written to that bit. Bits to which a 0 is written will not change state.

15	14	13	12	11	10 9	8	7	6 0
DPE	SSE	RMA	RTA	STA	DST	DPR	FBBC	Reserved

DPE: Detected Parity Error. This bit is set whenever a parity error is detected. It functions independently of the setting of the Command Register Bit 6.

SSE: Signaled System Error. This bit is set whenever the SARA-2 asserts the signal $\overline{\text{SERR}}$.

RMA: Received Master Abort. This bit is set whenever a bus master abort occurs in response to a PCI bus master transaction.

RTA: Received Target Abort. This bit is set whenever the SARA-2 has one of its own bus master cycles terminated by the currently addressed target.

STA: Signaled Target Abort. This bit is hard-coded to zero as the SARA-2 never generates a target abort during a slave access cycle.

DST: Device Select Timing. These bits define the signal behavior of the $\overline{\text{DEVSEL}}$ lead from the SARA-2 when accessed as a target. These bits are hard-coded to zeros as the SARA-2 asserts the $\overline{\text{DEVSEL}}$ lead using fast (1-cycle) response timing.

DPR: Data Parity Reported. This bit is set upon the detection of a data parity error or an active $\overline{\text{PERR}}$ input for a transfer involving the SARA-2 as the master. The Parity Error Enable bit (Bit 6 of the Command Register) must be set in order for this bit to be set.

FBBC: Fast Back-to-Back Capable. This bit is hard-coded to 1, which indicates that the SARA-2 can accept fast back-to-back cycles as a target when the transactions are not to the same agent.

Reserved: These reserved bits are hard-coded to zeros.

Command: This 16-bit register contains the PCI control information.

15 10	9	8	7	6	5	4	3	2	1	0
Reserved	FBBE	SEE	WCE	PEE	PSE	MWIE	SCE	BME	MSE	IOSE

FBBE: Fast Back-to-Back Enable. When set to 1, this bit permits the SARA-2 to perform fast back-to-back bus master cycles to different devices. When set to 0, the SARA-2 can only perform fast back-to-back transactions to the same device.

SEE: System Error Enable. When set to 1, this bit permits the SARA-2 to drive the open drain output lead $\overline{\text{SERR}}$. The $\overline{\text{SERR}}$ lead driven active low normally signifies an address parity error on the address/control bus.

WCE: Wait Cycle Enable. This bit controls whether the SARA-2 does address/data stepping. Since the SARA-2 never uses stepping, it is hard-coded to 0.

PEE: Parity Error Enable. When set to 1, parity errors are checked and reported on the $\overline{\text{PERR}}$ signal line. When set to 0, the SARA-2 ignores parity errors and continues normal operation.

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PSE: Palette Snoop Enable. This bit is used solely for PCI-based VGA devices and is hard-wired to zero.

MWIE: Memory Write and Invalidate Enable. The SARA-2 does not support the Memory Write and Invalidate command, so this bit is hard-coded to 0.

SCE: Special Cycle Enable. The SARA-2 does not monitor special cycles. This bit is hard-wired to zero.

BME: Bus Master Enable. This bit, when set to 1, allows the SARA-2 to function as a bus master.

MSE: Memory Space Enable. This bit allows the SARA-2 to decode and respond as a target for the memory region that is defined in its local memory base address register.

IOSE: This bit is hard-wired to zero as the SARA-2 does not implement I/O space.

Class Code: The 24-bit class code identifies the generic function of the device.

Revision ID: The revision identifier bits specify the SARA-2 device revision identifier.

BIST: The Built-In Self-Test register permits the control and status reporting of Built-In Self-Test.

Header Type: The header type defines the format for bytes 10H to 3FH. It is hard-code to zeros.

Latency Timer: The latency timer specifies the value of the latency timer used for PCI master accesses by the PCI bus master logic. This should be set appropriately by the PCI BIOS at system initialization**.**

Cache Line Size: The cache line size field is used by the system to define the cache line size. The SARA-2 does not use the Memory Write and Invalidate PCI bus cycle command when operating in the bus master mode, and therefore does not internally require this register.

Local Memory Base Address: The base address register provides a mechanism to set the base address of the local register/memory resources mapped into the PCI address space. It is up to the device driver to initialize this register. Bits 23-0 are hardwired to the value 0x000008, and the upper byte (bits 31-24) can be written with any value, so that the SARA-2 can be mapped in the host's memory space on 16 Mbyte boundaries.

0x14 - 0x3B: These registers are not used by the SARA-2.

Expansion ROM Base Address: This register is hard-wired to zero as the SARA-2 does not support an expansion ROM.

Max_LAT: The maximum latency register is used by bus masters to specify how often the device needs PCI bus access. The SARA-2 has no specific requirements and this register is reset to zero.

Min_GNT: This register is used by bus masters to specify how long a burst period the device needs. The SARA-2 has no specific requirements in this regard and the register is reset to 0x03.

Interrupt Lead: This register identifies which PCI interrupt is connected to the SARA-2's PCI interrupt leads. The SARA-2 uses the INTA line on the PCI bus, so this register is hard-wired to 0x01.

Interrupt Line: The interrupt line field is used to indicate interrupt routing information. The ultimate value for this register is system specific and should be set by the PCI host.

MError: This read-only bit indicates that the PCI bus master has encountered a fatal error. If a PCI bus error occurs, the MRd, CurrMasterRdAddr and CurrMasterWrAddr registers indicate where the error occurred. The BME bit in the command register needs to be reset to 0 for 16 PCI bus clock cycles and then to be set to 1 to re-enable the PCI bus master after MError bit becomes set to 1.

MRd: This read-only bit indicates that the PCI bus master is currently performing a read transaction. It is only valid when the MError bit is a 1. If this bit is a 1 when MError becomes set to 1 then the CurrMasterRdAddr register contains the offending address. If this bit is a 0 when the MError bit is set to 1, then the CurrMasterWrAddr register will contain the offending address.

Max Burst Len: Maximum single-transaction burst length (read/write by PCI host only).

CurrMasterRdAddr: This read-only 32-bit field is the current read target address used by the PCI bus master. It is valid only when the MError bit is a 1.

CurrMasterWrAddr: This read-only 32-bit field is the current write target address used by the PCI bus master. It is valid only when the MError bit is a 1.

PCI Host Address Map

The host processor's view of the SARA-2 external local memory, and configuration and control registers, is given in the memory map of Figure 11. The upper 8 bits of the Local Memory Base Address register in the PCI configuration space header must be added to the upper 8 bits of the address offsets given in the table below to determine the absolute address of the SARA-2 device and external local memory resources with reference to the PCI bus address space. The first four banks of the address space are used for reading and writing to the four banks of local memory that can be interfaced to the SARA-2 local memory bus. The remaining portion of the address map is used for accessing various communication device configuration and control registers within the SARA-2.

Byte Address Offset	Addressed Resource
0X00FFFFFF	Reserved
0X00FF0100	
0X00FF00FF	Communication Registers
0X00FF00C0	
0X00FF00BF	Device Debug Registers
0X00FF0080	
0X00FF007F	Device Configuration Registers
0X00FF0040	
0X00FF003F	Control / Status Registers
0X00FF0000	
0X00FEFFFF	Reserved
0X00FE0000	
0X00FDFFFF	External Memory Bank # 3
0X00C00000	
0X00BFFFFF	External Memory Bank # 2
0X00800000	
0X007FFFFF	External Memory Bank # 1
0X00400000	
0X003FFFFF	External Memory Bank # 0
0X00000000	

Figure 11. PCI Host Address Memory Map

REGISTER DESCRIPTIONS

The registers are summarized in the following table and described in detail in the subsequent text.

Register Name	Addr(Hex)	Description	Type*	Reset Value**
STATUS	00FF 0000	Interrupt Status Register	RO	0000 0100
CONTROL/ENABLE	00FF 0004	Control and Interrupt Enable Register	RW	0000 3800
MACCVS	00FF 0008	Memory Access Violation Source Register	RO	0X0X 0000
MACCVA	00FF 000C	Memory Access Violation Address Register	RO	0000 0000
ITIMER	00FF 0010	Interrupt Holdoff Timer Control Register	RW	0000 0000
Reserved	00FF 0014-00FF 003F	Reserved		
MODE_REG_0	00FF 0040	Mode Register 0	RW	0000 0000
MODE_REG_1	00FF 0044	Mode Register 1	RW	0000 0032
MODE_REG_2	00FF 0048	Mode Register 2	RW	0000 0000
Reserved	00FF 004C	Reserved		
MACC0	00FF 0050	Memory Access Control Register Bank 0	RW	0000 FFFF
MACC1	00FF 0054	Memory Access Control Register Bank 1	RW	0000 FFFF
MACC2	00FF 0058	Memory Access Control Register Bank 2	RW	0000 FFFF
MACC3	00FF 005C	Memory Access Control Register Bank 3	RW	0000 FFFF
IRAM_WE/$\overline{\text{PROTECT}}$	00FF 0060	Instruction RAM write enable register. Only bit 0 is defined. All other bits are reserved and should be written with 0.	R/W	0000 0000
Reserved	00FF 0064-00FF 007F	Reserved		
Reserved	00FF 0080 - 00FF 00BF	Reserved		
IR0BASE	00FF 00C0	Indicate Ring 0 Base Address Register	RW	0000 0000
IR0CSR	00FF 00C4	Indicate Ring 0 Control and Status Register	RW	0000 0000
IR0HEAD	00FF 00C8	Indicate Ring 0 Head Pointer	RW	0000 0000
IR0TAIL	00FF 00CC	Indicate Ring 0 Tail Pointer	RO	0000 0000
IR1BASE	00FF 00D0	Indicate Ring 1 Base Address Register	RW	0000 0000
IR1CSR	00FF 00D4	Indicate Ring 1 Control and Status Register	RW	0000 0000
IR1HEAD	00FF 00D8	Indicate Ring 1 Head Pointer	RW	0000 0000
IR1TAIL	00FF 00DC	Indicate Ring 1 Tail Pointer	RO	0000 0000
RR0BASE	00FF 00E0	Request Ring 0 Base Address Register	RW	0000 0000
RR0CSR	00FF 00E4	Request Ring 0 Control and Status Register	RW	0000 0000
RR0HEAD	00FF 00E8	Request Ring 0 Head Pointer	RW	0000 0000
RR0TAIL	00FF 00EC	Request Ring 0 Tail Pointer	RW	0000 0000

Register Name	Addr(Hex)	Description	Type*	Reset Value**
RR1BASE	00FF 00F0	Request Ring 1 Base Address Register	RW	0000 0000
RR1CSR	00FF 00F4	Request Ring 1 Control and Status Register	RW	0000 0000
RR1HEAD	00FF 00F8	Request Ring 1 Head Pointer	RW	0000 0000
RR1TAIL	00FF 00FC	Request Ring 1 Tail Pointer	RW	0000 0000

* R/W=Read and Write, RO=Read-Only. Reserved bits should be written with zeros.
** X indicates a bit that is not affected by reset.

Status Register

The STATUS register contains status bits which are set by certain events. Every bit in the STATUS register has an associated interrupt enable bit in the CONTROL/ENABLE register. If a particular interrupt enable bit is set to a 1, then the corresponding status bit will result in the generation of an interrupt. If a particular interrupt enable bit is set to a 0, then the corresponding status bit will not result in the generation of an interrupt, but will be set when the event occurs. The status bits are automatically cleared when the corresponding interrupt conditions are removed. The INT_STATUS field permits the host processor to determine the source of an interrupt.

31 14	13 11	10 0
Reserved	OPER_STATUS	INT_STATUS

The following describes the individual bits in the STATUS Register:

Bits 31-14: Reserved

Bit 13: ACPRUN:

This bit indicates the operating status of the ACP RISC core. This bit is cleared to 0 only when the ACPHALT bit is set to 1, indicating that the ACP has been forced to halt.

Bit 12: DMARUN:

This bit indicates the operating status of the DMA controller. This bit is cleared to 0 only when the DMA controller or the PCI bus master encounters a catastrophic error, or if the DMAHALT bit is set to 1.

Bit 11: LIRUN:

This bit indicates the operating status of the line interface. This bit is cleared to 0 only when a memory access violation occurs, or an instruction breakpoint is triggered by the ACP.

Bit 10: ACPINT:

This bit is set when the interrupt output from the ACP RISC core to the host is asserted.

Bit 9: EXTINT:

This bit indicates that the external interrupt input lead has been asserted low by an external device.

Bit 8: HALT:

This bit is set to 1 when any of the OPER_STATUS bits is set to 0 and is cleared to 0 when all of the OPER_STATUS bits are set to 1.

Bit 7: MACCV:

This bit is set to 1 whenever a memory address space violation occurs. This bit is cleared to 0 by the memory controller when the OPER_CTRL bits in the control register are cleared, indicating that normal device operation can continue.

Bit 6: BRKPT:

This bit, when set to 1, indicates that a breakpoint was encountered by the ACP. This bit is cleared to 0 when the ACPHALT bit is reset, allowing the ACP to resume operation.

Bit 5: PMERR:

This bit is set to 1 by the PCI bus master logic to indicate an error encountered during operation, causing the bus master to stop running. This bit is cleared to 0 when the PCI bus master has been re-enabled via the PCI configuration registers.

Bit 4: PMPERR:

This bit is set to 1 to indicate that the PCI bus master encountered a data parity error during its operation. This bit is automatically cleared to 0 when this register is read.

Bit 3: RR1INT:

This bit may be cleared to 0 by filling the request ring 0 buffer beyond the one quarter mark.

Bit 2: RR0INT:

This bit may be cleared to 0 by filling the request ring 1 buffer beyond the one quarter mark.

Bit 1: IR1INT:

This bit may be cleared to 0 by emptying the indicate ring 0 buffer.

Bit 0:IR0INT:

This bit may be cleared to 0 by emptying the indicate ring 1 buffer.

Control/Enable Register

The CONTROL/ENABLE register permits the host CPU to reset the SARA-2, configure and disable the device, and set up interrupt enables for various interrupt signals.

31 16	15	14	13 11	10 0
Reserved	RESET	Reserved	OPER_CTRL	INT_ENABLE

Bit 31-16: Reserved:

Bit 15: RESET

This bit, when set to 1, causes a complete device level reset of the SARA-2, excluding the PCI slave interface and the CONTROL/ENABLE register itself. This bit is cleared by either a hardware reset or by setting it to 0.

Bit 14: Reserved:

Bit 13: ACPHALT: ACP Halt

This bit, when set to 1, halts the ACP and must be set to 0 to resume normal operation.

Bit 12: DMAHALT: DMA Controller Halt

This bit, when set to 1, halts the DMA controller and must be set to 0 to resume normal operation.

Bit 11: LIHALT: Line Interface Halt

This bit, when set to 1, halts the line interface and must be set to 0 to resume normal operation.

Bit 10: EACPINT: Enable ACP Interrupt

This bit must be set to 1 to enable ACPINT interrupt.

Bit 9: EEXTINT: Enable External Interrupt:

This bit must be set to 1 to enable EXTINT interrupt.

Bit 8: EHALT: Enable Device Halt Interrupt:

This bit must be set to 1 to enable HALT interrupt.

Bit 7: EMACCV Enable Memory Access Violation Interrupt:

This bit must be set to 1 to enable MACCV interrupt.

Bit 6: EBRKPT: Enable Breakpoint Interrupt:

This bit must be set to 1 to enable BRKPT interrupt.

Bit 5: EPMERR: Enable PCI Master Error Interrupt:

This bit must be set to 1 to enable PMERR interrupt.

Bit 4: EPMPERR: Enable PCI Master Bus Parity Error Interrupt:

This bit must be set to 1 to enable PMPERR interrupt.

Bit 3: ERR1INT: Enable Request Ring 0 Interrupt:

This bit must be set to 1 to enable RR0INT interrupt.

Bit 2: ERR0INT: Enable Request Ring 1 Interrupt:

This bit must be set to 1 to enable RR1INT interrupt.

Bit 1: EIR1INT: Enable Indicate Ring 0 Interrupt:

This bit must be set to 1 to enable IR0INT interrupt.

Bit 0: EIR0INT: Enable Indicate Ring 1 Interrupt:

This bit must be set to 1 to enable IR1INT interrupt.

Interrupt Holdoff Timer Control Register (ITIMER)

This allows the host to set a programmable delay between interrupts caused by the message hardware, and thereby place an upper bound on the message interrupt rate. This register allows the host to set up a 16-bit interrupt holdoff timer for the communication queues. If a non-zero value is written to this register, an internal timer begins counting down this value at 1-microsecond intervals (i.e., it is decremented every microsecond). Until the register contents have been decremented to zero, interrupts to the host as a result of unread messages present in the two indicate rings (denoted by either or both the IR0INT and IR1INT bits in STATUS register being set to 1) or space available in the request rings (RR0INT or RR1INT, or both, bits in STATUS register being set to 1) will be disabled, regardless of the state of the corresponding enable bits in the CONTROL/ENABLE register. Thus, the host may hold off ring interrupts by any value between 1 and 65535 microseconds. The host may also clear (load with zero) this register at any time to defeat the timer function. The current value of the internal countdown timer can be read by reading this same register.

31 16	15 0
Reserved	INT_TIMER

Instruction RAM Write Enable Register (IRAM_WE/$\overline{\text{PROTECT}}$)

31 1	0
Reserved	IRAM_WE

Bits 31-1 are reserved and must be written with zero. Bit 0 is the IRAM_WE bit. It must be set to 1 to enable writing into the RISC instruction RAM. It should be set to 0 for normal operation.

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Host Communication Ring Registers

The host communication ring registers allow the host to pass requests to the SARA-2 via the request queue, and to receive indicate/response messages from the two indicate rings (referred to as ring #0 and ring #1, respectively).

Each ring is controlled by a set of 4 registers: Base Address, Head Pointer, Tail Pointer, and Control/Status registers. The Base Address register is 32 bits wide and only the lower 16 bits of the 32 bits are used from the other three registers. Their upper 16 bits are ignored when written and they return zeros when read.

The host communication ring register subspace is organized as follows:

Register Name	Register Function
IR0BASE	Indicate ring #0 base address register (32-bits)
IR0CSR	Indicate ring #0 control/status register (16 bits)
IR0HEAD	Indicate ring #0 head index register (16 bits)
IR0TAIL	Indicate ring #0 tail index register (16-bits)
IR1BASE	Indicate ring #1 base address register (32-bits)
IR1CSR	Indicate ring #1 control/status register (16 bits)
IR1HEAD	Indicate ring #1 head index register (16 bits)
IR1TAIL	Indicate ring #1 tail index register (16 bits)
RR0BASE	Request ring #0 base address register (32-bits)
RR0CSR	Request ring #0 control/status register (16 bits)
RR0HEAD	Request ring #0 head index register (16 bits)
RR0TAIL	Request ring #0 tail index register (16-bits)
RR1BASE	Request ring #1 base address register (32-bits)
RR1CSR	Request ring #1 control/status register (16 bits)
RR1HEAD	Request ring #1 head index register (16 bits)
RR1TAIL	Request ring #1 tail index register (16 bits)

The IR0BASE and IR1BASE registers contain the base address for each of the indicate ring buffers in host memory. They should be set up by the host device driver at initialization time to point to dedicated regions of its physical memory space that may be used by the SARA-2 communication logic as ring buffers.

The actual offsets of the read and write pointers of the rings are supplied by the head (IR0HEAD and IR1HEAD) and tail (IR0TAIL and IR1TAIL) index registers, respectively. The IR0HEAD and IR1HEAD registers must be updated by the host device driver after messages are read from the ring buffers. The IR0TAIL and IR1TAIL registers are updated by the SARA-2 as messages are written to the ring buffers.

The IR0CSR and IR1CSR registers provide configuration parameters for their corresponding indicate rings, as shown in the table below. These should be set up by the host prior to beginning communication.

15 8	7 4	3 0
RING_TIMER	MSG_CNT	RING_SIZE

The number of messages in the ring buffer is indicated by $2^{(RING\_SIZE - 1)}$. Valid values of RING_SIZE are between 3 and 15, supporting a number of messages in the ring buffer ranging from 4 to 16384 in multiples of 2.

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The 4-bit MSG_CNT field is incremented by the SARA-2 whenever a message has been transferred to the appropriate ring. This field thus contains a modulo-16 count of the number of transferred messages.

The 8-bit RING_TIMER field permits message transfer efficiency to be enhanced by defining a holdoff period for each indicate ring channel. The ring logic will attempt to transfer up to four consecutive messages at a time using a single (merged) PCI bus burst sequence, which significantly reduces message transfer overhead. This implies that at least four messages should be available in the source linked list before the ring logic is permitted to start transferring; otherwise, a 4-message burst cannot be performed. However, to place a latency bound on the message, the RING_TIMER field is used to reload an internal timer whenever a burst message transfer sequence has been completed (whether four messages have been transferred or not); no more message transfers are then attempted until the timer has counted down to zero. This allows the required number of messages to be queued to the ring prior to the next transfer start. To summarize, transfer commences when four messages are available or when the timer reaches zero, whichever occurs first. The RING_TIMER field counts in increments of 1 microsecond, and may indicate any holdoff value between 0 and 255 microseconds. A value of zero essentially defeats the holdoff mechanism.

The RR0BASE, RR0HEAD, RR0TAIL, RR1BASE, RR1HEAD, and RR1TAIL provide the base address, head and tail pointers for the two request rings. The RR0BASE and RR1BASE registers contain the base address for each of the request ring buffers in host memory. They should be set up by the host device driver at initialization time to point to dedicated regions of its physical memory space that may be used by the SARA-2 communication logic as ring buffers.

The actual offsets of the read and write pointers of the rings are supplied by the head (RR0HEAD and RR1HEAD) and tail (RR0TAIL and RR1TAIL) index registers respectively. The RR0HEAD and RR1HEAD registers are updated by the SARA-2 as messages are read from the ring buffers. The RR0TAIL and RR1TAIL registers must be updated by the host device driver after messages are written to the ring buffers. If the number of messages in the ring buffer (as determined by the difference between the head and tail index registers) is less than one quarter of the allocated ring size (in messages), an interrupt (RR0INT or RR1INT) is generated.

The RR0CSR and RR1CSR registers provide configuration parameters for their corresponding request rings, as shown in the table below. These should be set up by the host prior to beginning communication.

15 8	7 4	3 0
RING_LATENCY	MSG_THRESH	RING_SIZE

The number of messages in the ring buffer is indicated by $2^{(RING\_SIZE - 1)}$. Valid values of RING_SIZE are between 3 and 15, supporting a number of messages in the ring buffer ranging from 4 to 16384 in multiples of 2. The RING_SIZE field is cleared to zero upon reset and must be set to a valid value to resume normal operation.

The 4-bit MSG_THRESH field permits message transfer efficiency to be enhanced by defining a threshold count. If the number of messages is less than the threshold value, the SARA-2 will attempt to wait until more than MSG_THRESH messages are present in the ring before commencing a message transfer. It will then attempt to transfer MSG_THRESH consecutive messages using a single (merged) PCI burst sequence, which significantly reduces message transfer overhead. The MSG_THRESH field can be set to any value between 0 and 15.

The 8-bit RING_LATENCY field allows the SARA-2 or the host device driver to place a latency bound on messages present in the ring. If this field is set to a non-zero value, an internal timer will be started whenever at least one message is present in the ring (as indicated by the head and tail indices); if the timer counts down to zero, then a message transfer will be started regardless of whether the number of messages in the ring exceeds the MSG_THRESH field value. This prevents messages from waiting an unduly long time in the request ring if the total number of available messages is less than MSG_THRESH. The RING_LATENCY field indicates increments of 1 microsecond, and may be set to any value between 0 and 255 microseconds. A

value of zero essentially defeats the latency limiting mechanism. The RING_LATENCY timer is stopped and cleared whenever the number of messages in the ring is greater than MSG_THRESH, as this condition automatically triggers a message transfer.

Memory Access Control Registers

The MACC0, MACC1, MACC2 and MACC3 registers configure the memory controller to trap accesses to unimplemented portions of the SARA-2 local memory address space. Each 16-bit access control register is dedicated to a particular bank, and operates in an identical manner. In general, address checking for a given bank is configured by setting bits in the corresponding access control register. Each bank of the SARA-2 memory space is addressed using 22 address lines (the upper 2 bits of the 24-bit SARA-2 physical address are decoded to generate the bank chip selects). When any memory access is made to a particular bank, the upper 16 bits of this 22-bit memory address are logically ANDed with the Boolean inverse of the contents of the dedicated access control register. If the result is non-zero, an access violation has occurred.

An access violation can occur either because of an internal SARA-2 logic access (i.e., the ACP, DMA Controller, or Line Interface) or if the access was initiated by the host itself via the PCI slave port. The two cases, internal access violation versus host slave access violation, are treated the same by the SARA-2 chip.

For example, in the case of an internal access violation, the SARA-2 memory controller does not complete the access but halts the SARA-2 chip and signals an interrupt to the host if the EMACCV bit is set in CONTROL/ ENABLE register. The access violation will cause the MACCV bit in the STATUS register to be set. The host must remove the halt state (by clearing to 0 the OPER_CTRL bits in the CONTROL/ENABLE register) before the SARA-2 can continue operation; this will simultaneously clear the access violation.

The address checking hardware provides access control on 128-byte boundaries. To define the memory regions accessible for a particular bank, it is merely necessary to set those bits in the access control register that correspond to address bits that could be a logic '1' during a valid access.

For example, if a 32 kbyte SRAM bank were mapped into bank three in the range between 0 and 7FFF hex, bits 0 through 8 of MACC3 would be set to ones, and bits 9 through 15 would be set to zeros.

Note: The PCI host slave read accesses must be restricted to 1 word less than the MACCn value to avoid a memory access violation.

Mode Register 0

Mode Register 0 is used to configure various implementation-specific features of the memory type used for control memory. The following describes the individual bits in Mode Register 0:

Bits 31-16: Reserved

These bits are ignored when written and return zeros when read.

Bits 15-14: MXSEL:

The MXSEL bits determine which Control Memory Address (CA) bits are output on the Multiplexed Control Memory Address CMA (10-0) signal lines when SRAM is being accessed.

MXSEL		Control Memory Address (CA) bits that are output on the Multiplexed Control Memory Address CMA (10-0) signal lines										
15	14	CMA 10	CMA 9	CMA 8	CMA 7	CMA 6	CMA 5	CMA 4	CMA 3	CMA 2	CMA 1	CMA 0
0	0	20	19	18	17	16	15	14	13	12	11	10
0	1	21	20	19	18	17	16	15	14	13	12	11
1	0	2	21	20	19	18	17	16	15	14	13	12
1	1	3	2	21	20	19	18	17	16	15	14	13

Example: When MXSEL = 1,1 then CA[3, 2, 21..13] are output on CMA[10..0] during SRAM accesses.

Bit 13: Reserved

Bit 12: Reserved

Bits 11-9: MTYPE3:

Memory type selection for bank 3. See the following table.

Bits 8-6: MTYPE2:

Memory type selection for bank 2. See the following table.

Bits 5-3: MTYPE1:

Memory type selection for bank 1. See the following table.

Bits 2-0: MTYPE0:

Memory type selection for bank 0. See the following table.

The above four sets of bits define the type of memory connected to banks 3, 2, 1 and 0, respectively. They should be initialized by the host device driver prior to allowing the SARA-2 to access memory. The bits are coded as follows:

MTYPEn	Memory Type	Speed (maximum access time)	$\overline{\text{CRDY}}$ controllable?
000	Asynchronous SRAM	12 ns	No
001	Reserved (do not use)		
010	Reserved (do not use)		
011	Reserved (do not use)		
100	Reserved (do not use)		
101	Reserved (do not use)		
110	Reserved (do not use)		
111	Reserved (do not use)		

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Mode Register 1

Mode Register 1 is used to configure various implementation-specific features of the SARA-2. The following describes the individual bits in Mode Register 1:

15 12	11	10	9	8 6	5 0
Reserved	ND_BENDIAN	MD_BENDIAN	Reserved	Reserved	PRESCALER

Bits 31-12: Reserved

These bits are ignored when written and return zeros when read.

Bit 11: ND_BENDIAN

This bit controls the byte order for any data that originates from or is placed into ATM cells by the DMA controller.

0 - Little Endian byte order (default)

1 - Big Endian byte order

If this bit is set to 1, a byte swap is performed, swapping bytes 0 and 3, and bytes 1 and 2 to transform the data into Big-Endian format from the default Little-Endian format.

Bit 10: MD_BENDIAN

This bit controls the byte order for message data transfer to and from the communication queues.

0 - Little Endian byte order (default)

1 - Big Endian byte order

If this bit is set to 1, a byte swap is performed, swapping bytes 0 and 3, and bytes 1 and 2 to transform the message into Big-Endian format from the default Little-Endian format.

Bit 9: Reserved

This bit must be set to 0.

Bits 8-6: Reserved

These bits are reserved. Bit 8 must be written with a 1 and bits 7 and 6 must be written with a 0.

Bits 5-0: PRESCALER

The PRESCALER bits control the divide ratio used by the prescaler that drives the on-chip real-time clock counter. It should be set up to allow the prescaler to generate a 1 MHz output from the SYSCLK input; for instance, a SYSCLK frequency of 50 MHz implies that decimal 50 (0x32) should be loaded into this field.

Mode Register 2

The bits in Mode Register 2 are used to configure the framer.

Bit 15: C1D (Enable Discard Cells for CLP Equal to One):

A 1 enables the SARA-2 device to discard received cells which have a CLP field equal to 1.

Bit 14: NLD (Discard Cells for VCI and VPI Equal Zero Enable):

A 1 enables the SARA-2 device to discard received cells which have VCI and VPI fields equal to 0.

Bit 13: AIS2LOP (Enable AIS to LOP Transition):

Enables the AIS to LOP transition in the SONET/SDH pointer state machine. For North American applications the transition is not specified.

Bit 12: SSEN (SS-Bits Enable):

A 1 enables the SS-bits defined in the H1 byte to be used in the pointer tracking state machine. In the transmit direction the SS-bits will sent equal to 10. A 0 disables the SS-bit checking sequence in the pointer tracking state machine. The transmit bits are sent as 00. For North American applications the SS-bits are not used.

Bit 11: LB (Loopback Enable):

A 1 enables a SONET/SDH Loopback. Transmit data is looped back as receive data. The receive line is disabled, and the transmit data is sent.

Bit 10: ALRMCLR (Alarm Clear):

A 1 clears the received alarm states.

Bit 9: Not Used.

Bit 8: S52 (STS-1 Frame Format Enable):

A 1 enables the SONET/SDH framer to interface with the STS-1 format. A 0 enables the framer to interface with the STS-3c/STM-1 frame format.

Bit 7: CHS: Cell Handshake

If set to 1, enables cell level handshaking for UTOPIA interface; otherwise, enable octet level handshaking.

Bit 6: TCS (Transmit Clock Sense):

A 0 enables parallel SONET/SDH data signal to be clocked out on rising edges of the clock. A 1 enables the data to be clocked out falling edges of the clock. This bit does not affect serial mode operation.

Bit 5: RCS (Receive Clock Sense):

A 0 enables parallel SONET/SDH data signal to be clocked in on rising edges of the clock. A 1 enables the data to be clocked in on falling edges of the clock. This bit does not affect serial mode operation.

Bit 4: SFE (Serial Framer Enable):

A 1 selects the 155 Mbit/s bit-serial framer interface. A 0 selects a byte-parallel framer interface.

Bit 3: HCD: Disable HEC coset during cell generation / extraction

If this bit is set to 1, the coset is disabled during HEC generation. This bit must be set to 0 for normal HEC generation.

Bit 2: HCS: Enable HEC correction

If this bit is set to 1, HEC correction is enabled on received cells. If set to 0, all cells with HEC errors are discarded.

Bit 1: CUP: Configure UTOPIA PHY mode

If this bit is set to 1, the SARA-2 cell interface acts as a PHY device to be able to connect to an external ATM layer device such as an ATM switch. If this bit is set to 0, the cell interface acts as an ATM layer device and can connect to any UTOPIA compliant PHY layer device.

Bit 0: DCRD: Disable Cell Rate Decoupling

This function is used in the UTOPIA mode only. When this bit is set to 1, unassigned cells that are generated by the SARA-2 are not passed out of the SARA-2. When this bit is set to 0, unassigned cells are passed out of the SARA-2.

Memory Access Violation Status Register (MACCVS)

The read-only MACCVS register provides the source and status of an illegal memory access when the MACCV bit is set to 1 in the STATUS register. When the MACCV status bit is cleared to 0, the contents of the MACCVS register are not defined.

Bits 31-11: Reserved

These bits are reserved.

Bit 10: HMAERR

This bit is set to 1 if a host slave access to read or write a memory location caused an access violation.

Bit 9: LOERR:

This bit is set to 1 if a line output interface block access to a memory location caused an access violation.

Bit 8: LIERR:

This bit is set to 1 if a line input interface block access to a memory location caused an access violation.

Bit 7: DMAOERR:

This bit is set to 1 if a DMA output block access to a memory location caused an access violation.

Bit 6: DMAIERR:

This bit is set to 1 if a DMA input block access to a memory location caused an access violation.

Bit 5: ACPLERR:

This bit is set to 1 if an ACP load access to a memory location caused an access violation.

Bit 4: ACPFERR:

This bit is set to 1 if an ACP fetch access to a memory location caused an access violation.

Bits 3-0: MWE:

These bits reflect the per-byte memory write enable signals if the access violation was caused by a write operation. If the access violation was caused by a read operation these bits are set to 0.

Memory Access Violation Address Register (MACCVA)

This read-only MACCVA register permits the host to determine the target of an illegal memory access. The least significant 24 bits of this register give the 24-bit address of the illegal memory access when the MACCV bit is set to 1 in the STATUS register. When the MACCV status bit is cleared to 0, the contents of the MACCVA register are not defined.

Framer Control and Status Registers

The SONET Framer communicates to its outside world through status and control registers. Of these registers, only mode register 2 is visible to the host. Mode register 2 is a control register (i.e., written by the host or the RISC Core, and read by the framer) that contains setup information for the framer. Most of these bits are configured once at startup, and are only modified for mode changes. The only exception is the ALRM_CLR bit, which clears all the receive-side alarms in the framer, and thus might be used during operation. Since the RISC Core can set mode register 2, these bits can be set via the Service Interface.

The remaining framer registers are only accessible to the RISC Core, and can be divided into 4 groups: framer run bits (reset and enable), transmit side force controls, receive side alarms, and ATM performance counters.

Transmit side force controls are used to send out test (alarm) conditions on the transmit path. These error and alarm-insertion features are controlled by a control register and a pattern register.

Receive side alarms can be either status bits that reflect the result of a hardware-calculated alarm, or information provided so the firmware can calculate an alarm. Also included in the group are the path, line and section BIP error counters. The current number of errors is reported by the hardware; the accumulator is maintained by firmware.

Finally, there are 4 ATM performance counters: RXCELLS, RXLOST, TXCELLS and TXFILLS.

The internal framer registers are not accessible to the host, except via the Service Interface. See "SARA-*Lite* Service Interface Technical Manual" (TXC-05551-TM1).

DATA STRUCTURES

This section is provided only to help the user understand more about the SARA-2. The data structure is not intended to be accessed by the host. The field definitions of the data structure are dependent on the microcode implementation, and may also change in future revisions of the SARA-2 device.

The control memory contains data structures which are used by both host software and the SARA-2 to maintain dynamic state information. It is also used to communicate between the SARA-2 and the host software entity. The SARA-2 control memory holds the following data structures:

- Segmentation VC Structure
- Rate Control Table (RCT)
- Buffer Descriptor (BD)
- Reassembly Hash Table
- Reassembly VC Structure
- Reassembly Buffer Pool
- Message Pool
- Request Ring / Indicate Ring
- Cell Buffers

Each of the above data structures is described in the following sections.

Segmentation VC Structure

The segmentation virtual circuit (VC) table contains information relating to each virtual connection set up for segmentation. A separate entry is present for each virtual circuit, whether it is CBR/VBR. When a virtual connection is established, the contents of the entry corresponding to the virtual circuit are initialized by software. A VC structure entry indicates the AAL type associated with the virtual circuit and contains other control and status information specific to the virtual circuit. Additional fields in the entry indicate the virtual circuit segmentation rate and provide a pointer to active buffer descriptors. The organization of each VC structure entry is shown in Figure 12, and the fields are described below.

Virtual Circuit Mode Bits	BurstSize/CNT_Nrm
CellCount	CURRENT_BUFF_DESCR
LAST_BUFF_DESCR	ATM Header
AAL-Specific Field	Next UBR VC Pointer
Reserved	Reserved
Reserved	Reserved
Out-of-Rate RM Cell/OAM Cell Pointer	LANEHDR
VC Structure Index	HEAD_BUFF_DESCR
UBR parameters	

Figure 12. Segmentation Virtual Circuit Parameters

Virtual Circuit Mode Bits

The organization of the virtual circuit mode bits is shown below.

AAL_TYPE	OAM	Reserved	FCT	LANEM	Reserved

The AAL_TYPE field indicates the AAL segmentation algorithm desired. These bits further define the AAL-specific fields. The AAL_TYPE field (Bits 31,30) is coded as follows:

00 - AAL0 or raw cell (null AAL)
01 - AAL1
10 - AAL3/4
11 - AAL5

When the OAM field (Bit 29) is set, it indicates that the OAM Cell Pointer field contains a valid pointer to an out-of-rate RM cell or an OAM cell that is to be sent prior to any data cells.

The FCT field, if set, indicates that entire 64-byte cells buffers must be transferred from the host memory rather than only 48-byte payloads. This bit is used only when the AAL_TYPE is set to 00.

The LANEM bit must be set to 1, if LAN Emulation support is desired.

BurstSize

For VBR virtual circuits, this 8-bit field determines the number of cells to send in a burst when this virtual circuit is serviced.

CellCount

This is a 16-bit counter that counts the total number of cells transmitted on this virtual circuit.

CURR_BUFF_DESCR

This 24-bit descriptor pointer points to the head of a linked list of buffer descriptors ready for segmentation on this virtual circuit. When the transmit scheduler services this virtual circuit, if this field is NULL, then no payload exists and UBR virtual circuits are serviced.

LAST_BUFF_DESCR

This 24-bit descriptor pointer points to the tail of the linked list of buffer descriptors ready for segmentation on the virtual circuit. When the host submits a new packet for segmentation, this pointer is used to link the buffer descriptors of the new packet.

ATM Header

These four bytes contain the ATM cell header of cells generated on the corresponding virtual circuit. The SARA-2 uses these bytes, without modification, as the ATM cell header, except for the PTI and CLP bits, which may be used from the Buffer Descriptor on a per-host buffer basis. The least significant bit of the PTI field is set appropriately for the last cell of an AAL5 packet independently of the settings of that bit in this field. Software should set these fields to conform to ATM standards.

AAL-Specific Field

This field serves a different purpose for each AAL type. For AAL5, this 32-bit field is used to maintain the residual 32-bit CRC value of the packet under segmentation. It is reset to all-ones at the start of segmentation of each CPCS-PDU. For AAL3/4, this field is used to maintain the sequence number (SN), segment type (ST) and the multiplexing identifier (MID) value. For AAL1, this field is used for two sets of CSI bits and the sequence number (SN) field.

Next UBR VC Pointer

This 24-bit field, used only for UBR virtual circuits, provides a pointer to the segmentation virtual circuit table entry for the next UBR virtual circuit. This entry is used to chain UBR virtual circuits into a circular linked list. The software must point the last UBR virtual circuit to the head of the UBR virtual circuit chain. The transmit scheduler traverses the circular list of UBR VCs sequentially, segmenting and sending cells on these VCs whenever possible. The Rate Control Table (discussed later) is used to service CBR and VBR virtual circuits.

OAM Cell Pointer

When the OAM bit is set to'1', this field provides a 24-bit pointer to an OAM cell that must be sent prior to any data cells.

LANEHDR

If the LANEM bit is set, this field used for the LAN Emulation header. During segmentation, the 2-byte LAN Emulation header is inserted into the first cell of every AAL5 PDU sent on this virtual circuit.

VC Structure Index

This 24-bit host-assigned VC identifier is used to refer to this segmentation VC structure entry when communicating with the host through the message queue.

HEAD_BUFF_DESCR

This is a 24-bit pointer to the head of intermediate buffer descriptor used by the firmware.

Rate Control Table

The SARA-2 uses the Rate Control Table (RCT) to provide precise control over the granularity of rates requested per virtual circuit and to provide flexibility in the multiplexing of different virtual circuits. It is also used to determine the burst size and sustainable cell rate (SCR) allocated to each virtual circuit. The traffic shaping hardware in the device traverses the Rate Control Table to schedule cell transmissions.

The RCT is a linear array of 32-bit entries, as illustrated in Figure 13. Each entry points to a segmentation VC structure entry. During segmentation, the RCT is traversed sequentially and each entry is provided service according to the control bits. Each entry in the table corresponds to a CBR or VBR virtual circuit. When an entry in the RCT is serviced, one or more ATM cells (based on the burst size in the Segmentation VC Structure) can be sent from that virtual circuit. More than one entry in the RCT may point to the same Segmentation VC Structure entry, allowing multiple service access to that virtual circuit in a single traversal of the RCT. This allows flexible multiplexing and bursting of cells from a virtual circuit. An UBR virtual circuit is serviced when the CBR or VBR virtual circuit pointed to by the RCT does not have cells to send. An RCT entry may also specify a NULL entry (an idle cell is sent) or a SKIP entry (that entry is skipped).

CTRL	Data Field 23 0
CTRL	Pointer to Segmentation VC Structure Entry 1
	Pointer to Segmentation VC Structure Entry 6
• • •	• • •
	Pointer to Segmentation VC Structure Entry n
• • •	• • •
• • •	• • •
000	Jump to Beginning of Table

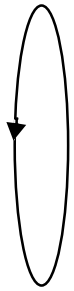


Figure 13. Rate Control Table

The 3-bit CTRL field determines the operation to be performed when the RCT is read and is interpreted as follows: if the CTRL field is set to 111, the data field provides a pointer to the segmentation VC structure from which cells must be sent. If the CTRL field is set to 000, data field provides the 24-bit jump address of the rate control table. Thus, null entries in the rate control table can be skipped by using such a jump control field. It can also be used to create loops in the RCT as shown in the last row of Figure 13. If the CTRL field is set to 011, a number of NULL cells indicated by the value in data field will be sent out to the line.

Buffer Descriptor Table

The SARA-2 segments and reassembles packets using the host buffer memory. The buffer descriptor (BD) is a set of 16-byte entries that describe the parameters of blocks of data or free buffers. Each entry contains parameters for segmenting packets and the location of the buffer in the packet memory. When a packet is set up for segmentation, an available buffer descriptor, as described in Figure 14, is initialized with the packet parameters. Similarly, free buffer descriptors, as described in Figure 15, are used to reassemble cells into packets. Buffer descriptors are chained together in a linked list to support scatter and gather algorithms and to support efficient packet memory management.

Descriptor Mode	NEXT_PTR
HOST_BUFF_ADDR	SIZE
Trailer	

Figure 14. Buffer Descriptor Parameters for Segmentation

NEXT_PTR	HOST_BUFF_ADDR
SIZE	

Figure 15. Buffer Descriptor Parameters for Reassembly

The general format of a buffer descriptor entry is illustrated in Figure 14 and the fields are described below.

Descriptor Mode Bits

The organization of the eight descriptor mode bits is shown below.

EOP	NOTIFY	TRLR	ABORT	Reserved	CNG	EOM_EN	CLP_EN

EOP - Indicates that this buffer descriptor contains the end of the packet.

NOTIFY - Notify after this buffer descriptor is processed.

TRLR - When set, address 0CH gives the PDU trailer.

ABORT - Abort segmentation on this packet.

CNG - Value to use for bit 1 of the PTI field in the ATM cell header when sending data from this buffer.

EOM_EN - Value to use for bit 0 of the PTI field in the ATM cell header when sending data from this buffer. For AAL5, if this buffer contains the end of packet, PTI 0 is automatically set to 1 on the last cell to indicate end of packet.

CLP_EN - Value to use for CLP bit in the ATM header when sending data from this buffer.

NEXT_PTR

The SARA-2 allows a single packet to be scattered among different host buffers. This 24-bit field provides the pointer to the next buffer descriptor for this virtual circuit. This linked list of descriptors provides efficient packet memory buffer management. Multiple packets, each scattered among several host buffers, may be linked using this mechanism. Note that the end of a packet is indicated by the EOP bit in the descriptor mode bits.

HOST_BUFF_ADDR

This field provides the 32-bit address of the data buffer in host memory.

SIZE

This 16-bit field is the size of the host buffer in bytes.

Trailer

This is the 32-bit CPCS-PDU trailer to be appended to the CPCS-SDU.

Reassembly Hash Table

The Reassembly Hash Table consists of a linear array of 24-bit pointers to chains of Reassembly VC Structure entries, as illustrated in Figure 16. The hash table logic performs a hash on the VPI/VCI fields of each received ATM cell header to derive a table index to an entry in the Reassembly Hash Table. The hash index computation is controlled by a set of three registers which provide two 16-bit masks and a 4-bit shift value. By programming different binary patterns into the mask registers and using different shift values, different hash functions may be generated.

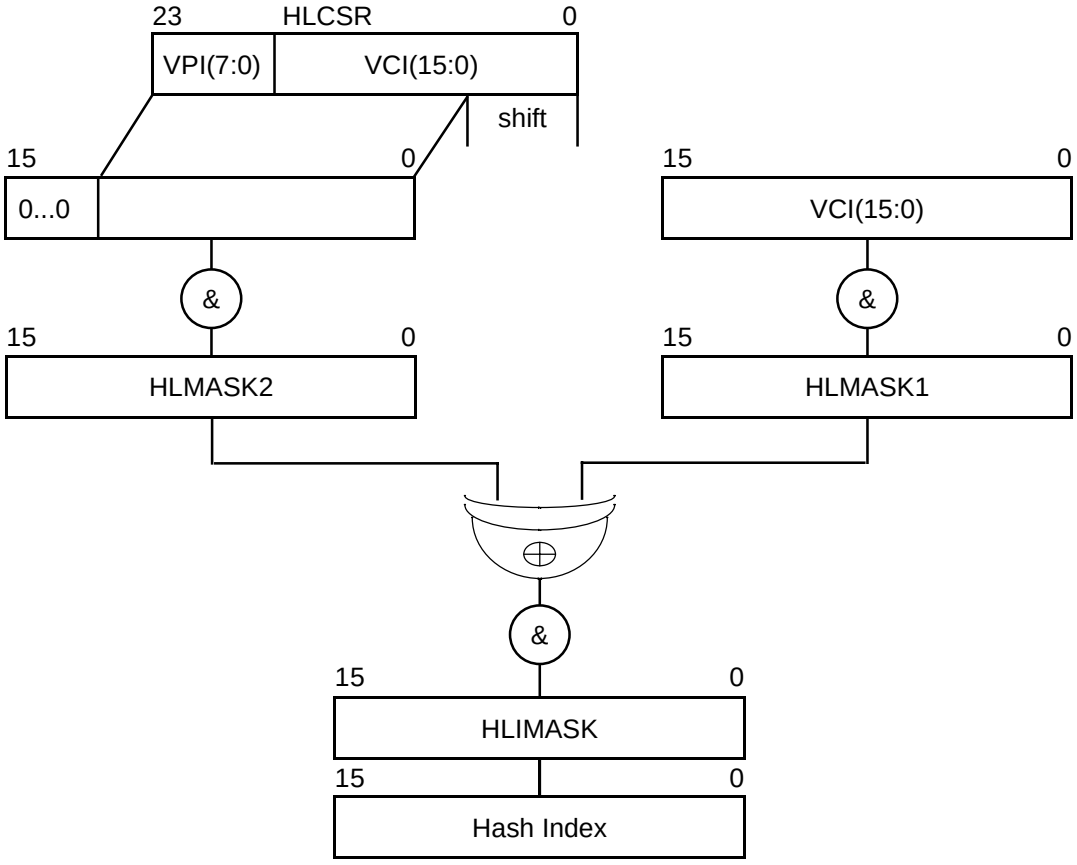
The index generated by the hashing logic is used to read a 32-bit word from the hash table, which is a pointer to a hash bucket. Each hash bucket corresponds to the first three 32-bit words of the Reassembly VC Structure. A hash bucket chain is a linked list of Reassembly VC Structure entries. The ATM Header from the Reassembly VC Structure is compared against the incoming cell header. A header comparison is performed by logically ANDing the ATM Header Mask bits and ATM Header bits from the Reassembly VC Structure and the 32-bit ATM header of the received cell. If the comparison fails, the NEXT_VC_PTR in the Reassembly VC Structure is used to traverse the hash bucket chain until an ATM cell header match is found or the end of the chain is reached.

Pointer to first Reassembly VC Structure Entry in Hash Bucket Chain # 1
Pointer to first Reassembly VC Structure Entry in Hash Bucket Chain # 2
Pointer to first Reassembly VC Structure Entry in Hash Bucket Chain # 3
• • •
Pointer to first Reassembly VC Structure Entry in Hash Bucket Chain # (n-1)
Pointer to first Reassembly VC Structure Entry in Hash Bucket Chain # n

Figure 16. Reassembly Hash Table

Hash Computation Logic

The hash index computation is controlled by a set of 16-bit registers: HLMASK1, HLMASK2, HLIMASK and HLCSR. The least significant 4 bits of the HLCSR register indicate a shift value *shift* that is used in the hash index computation shown in Figure 17. Another register HLBASE is used by the firmware to indicate the starting address of the receive reassembly hash table. The resulting hash index is added to the HLBASE register to obtain the 24-bit memory address of the reassembly hash table entry. The registers HLMASK1, HLMASK2, HLIMASK, HLCSR and HLBASE are set via the Service Interface. For details, please refer to the SARA-*Lite* Service Interface Technical Manual, document number TXC-05551-TM1.



Note: "&" indicates 16 two-input AND gates operating on the corresponding bits of the registers or gates immediately above and below it, with the 16-bit result passed downwards.

Figure 17. Hash Index Computation Logic

Reassembly VC Structure

The reassembly virtual circuit table contains information relating to each virtual connection set up for reassembly. When a virtual connection is established, the contents of the entry corresponding to the virtual circuit are initialized by software. A VC structure entry indicates the AAL type associated with the virtual circuit and contains various control and status information related to the virtual circuit. The organization of each VC structure entry is illustrated in Figure 18 and the fields are described below.

ATM Header	ATM Header Mask
NEXT_VC_PTR	AAL_CTRL
CELL_CTR	FLAGS
CURR_BUFF_DESCR	TAIL_BUFF_DESCR
AAL-specific field	HEAD_BUFF_DESCR
LAST_BUFF_DESCR	PKT_CELL_CNT
VC Structure Index	BASize

Figure 18. Reassembly Virtual Circuit Parameters

ATM Header

This 32-bit field is used in conjunction with the ATM Header Mask field by the hash control logic to detect received cell header match. If the comparison succeeds, the received cell belongs to this virtual circuit and the AALTYP sub-field of AAL_CTRL gives the associated AAL type. Note that, although a 32-bit ATM cell header is supported, the PTI and CLP bits may be masked using the ATM Header Mask field.

ATM Header Mask

This 32-bit field is the mask field used by the hash control logic. See the Reassembly Hash Table description above for details.

NEXT_VC_PTR

This 24-bit field is a pointer to the next Reassembly VC structure entry in the hash bucket chain. See the Reassembly Hash Table description above for details.

AAL_CTRL

The 16-bit AAL_CTRL field contains sub-fields, as shown below:

AALTYP	Reserved	MID_SEL	Reserved	STATUS

AALTYP: The AALTYP field (Bits 31, 30) is coded as follows:

00 - AAL1
01 - AAL3/4
10 - AAL5

MID_SEL: Bits 27-24 indicate the number of significant bits of the MID field to use for reassembly (used for AAL3/4 only)

STATUS: Bits 19-16 are status bits that provide the PTI and non-zero GFC indication

Bit 19: CNG indication from received cells

Bit 18: Set if a non-zero GFC cell is received on this virtual circuit

BIt 17: CRC-10 error indication (used only for AAL 3/4 and OAM virtual circuits)

Bit 16: PTI Alert indication

CELL_CTR

This 16-bit field counts the number of received cells for this virtual circuit.

FLAGS

This 8-bit field provides is formatted as follows:

NOALLOC	SKIP_HDR	FCT	Reserved

If the NOALLOC field is set, the SARA-2 does not allocate a free host buffer descriptor from the reassembly buffer pool for this virtual circuit.

If the SKIP_HDR field is set, for AAL 3/4 virtual circuits, the 4-byte CPCS-PDU header is not transferred to the host memory.

If the FCT bit is set, 64-byte cell buffers are transferred to the host memory when AALTYP is set to 00.

CURR_BUFF_DESCR

This 24-bit field provides the pointer to the data buffer descriptor that is currently being used for reassembly.

TAIL_BUFF_DESCR

This 24-bit field provides the tail of the linked list of buffer descriptors.

AAL-specific Field

This 32-bit field is used differently based on the AALTYP field. For AAL5, the 32-bit field is used to maintain the residual 32-bit CRC value of the packet under reassembly. It is reset to all-ones at the start of reassembly of each CPCS-PDU. For AAL3/4, this field is used to maintain the sequence number (SN), segment type (ST) and the BTAG value. For AAL1, this field is used for two sets of CSI bits.

HEAD_BUFF_DESCR

This 24-bit field provides the pointer to the data buffer descriptor that is used for the first cell of a packet.

LAST_BUFF_DESCR

This 24-bit field provides the pointer to the data buffer descriptor that is used for the last cell of a packet.

PKT_CELL_CNT

This 16-bit field provides the number of cells received for the current packet (the CELL_CTR field provides the total number of cells received for this VC, as described above).

VC Structure Index

This 24-bit host-assigned VC identifier is used to refer to this segmentation VC structure entry when communicating with the host through the communication queue.

BASize

This is a 16-bit buffer allocation size field, for AAL3/4 virtual circuits.

Reassembly Buffer Pool

The reassembly buffer pool is a linked list of free buffer descriptors. It is used by the SARA-2 to queue the buffer descriptors to host buffers that are available for packet reassembly. When the SARA-2 receives the first cell of a packet, it fetches a descriptor from this queue and starts reassembly in the host buffer pointed to by the descriptor.

Message Pool

The message pool is a linked list of free 16-byte request message descriptors. The messages from the request rings in host memory are transferred into these descriptors. These descriptors will then be linked to the VC structure or to the reassembly buffer pool. If the message is a packet for segmentation, this descriptor is linked to VC structure, but if it is a host buffer for a received cell it is linked to the reassembly buffer pool.

Cell Buffers

The cell buffers are 64-byte memory segments in local control memory used for temporary storage of cells for segmentation and reassembly. These buffers allow lossless reassembly even under large PCI latency restrictions.

Request Ring / Indicate Ring

The SARA-2 host interface logic implements a set of host request ring / indicate ring buffers and associated logic which facilitate the exchange of messages between the host software (e.g., device drivers) and the on-chip RISC firmware with very low overhead in either an interrupt-driven or polled manner. The SARA-2 uses these queues to communicate to the host the completion of segmentation or reassembly of a packet. The communication queue registers in SARA-2 have hardware support for minimizing message interrupt overhead and also for setting bounds on interrupt overhead. Further details are provided in the Register Descriptions section.

EXTERNAL CIRCUIT REQUIREMENTS

The external circuits shown in Figure 19 are required for proper operation of the SARA-2 device

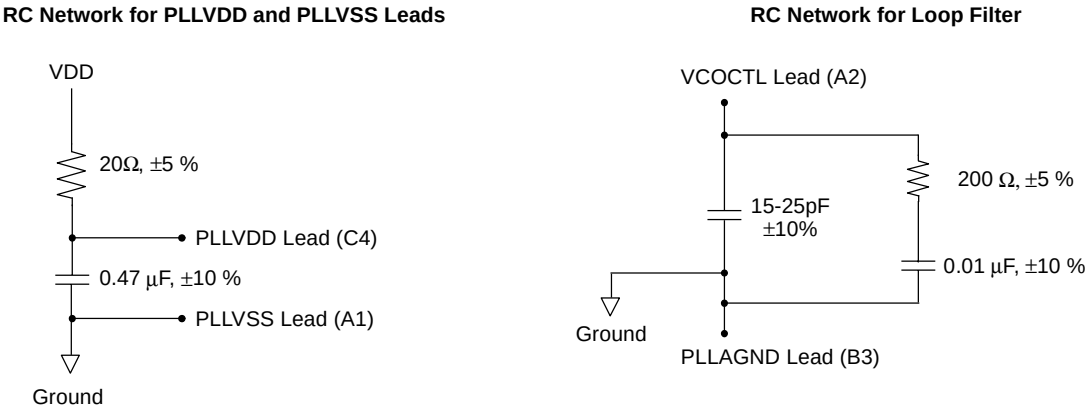


Figure 19. External Circuit Requirements for SARA-2

TEST ACCESS PORT

(Information on the Boundary Scan capability will be added in a later edition of this Data Sheet.)

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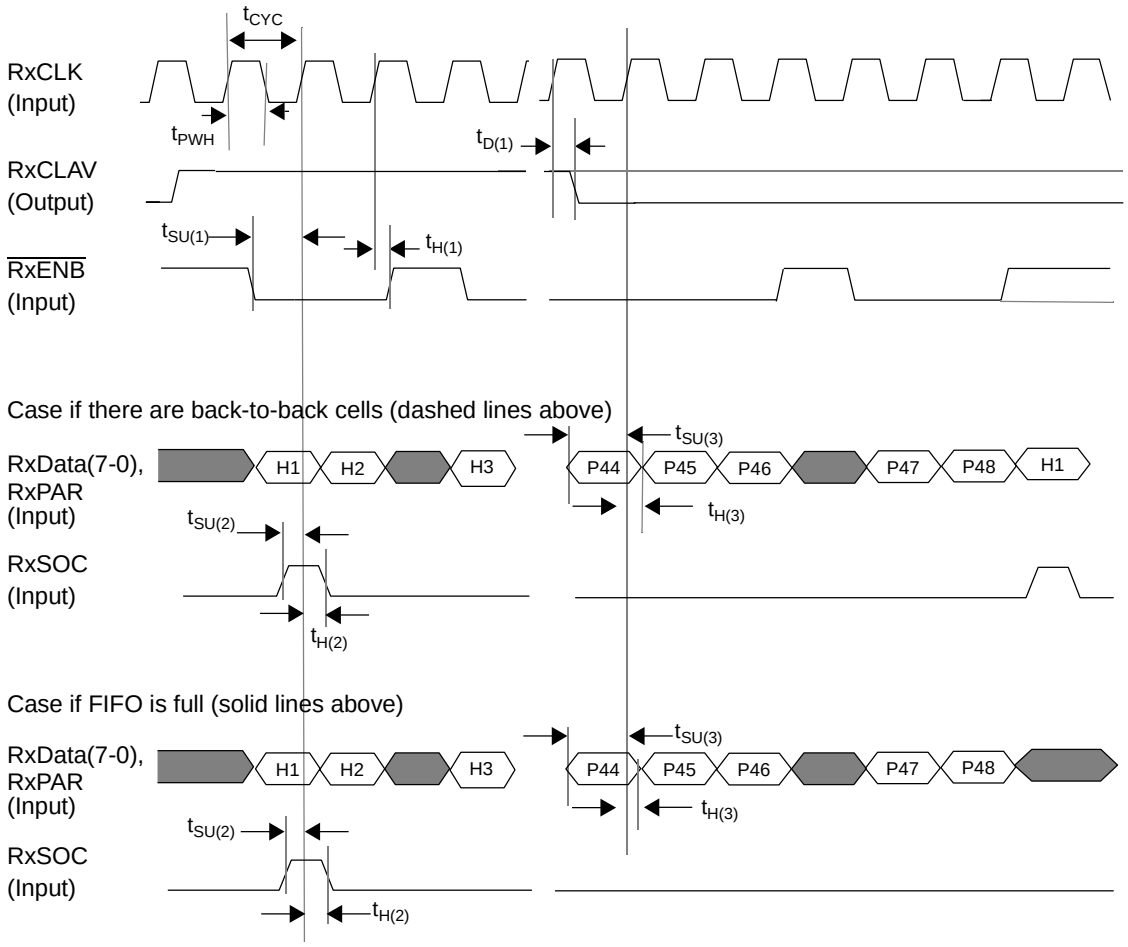
TIMING CHARACTERISTICS

Detailed timing diagrams for the SARA-2 device are provided in Figures 20 through 35, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a maximum load capacitance of 25 pF (except for Figures 32 through 35, which use 50 pF). Timing parameters are measured at voltage levels of $(V_{IH}+V_{IL})/2$ and $(V_{OH}+V_{OL})/2$, for input and output signals, respectively.

LINE INTERFACE

Cell Interface UTOPIA-PHY Mode

Figure 20. Cell Receive Timing - Cell Level Handshake for UTOPIA-PHY Mode



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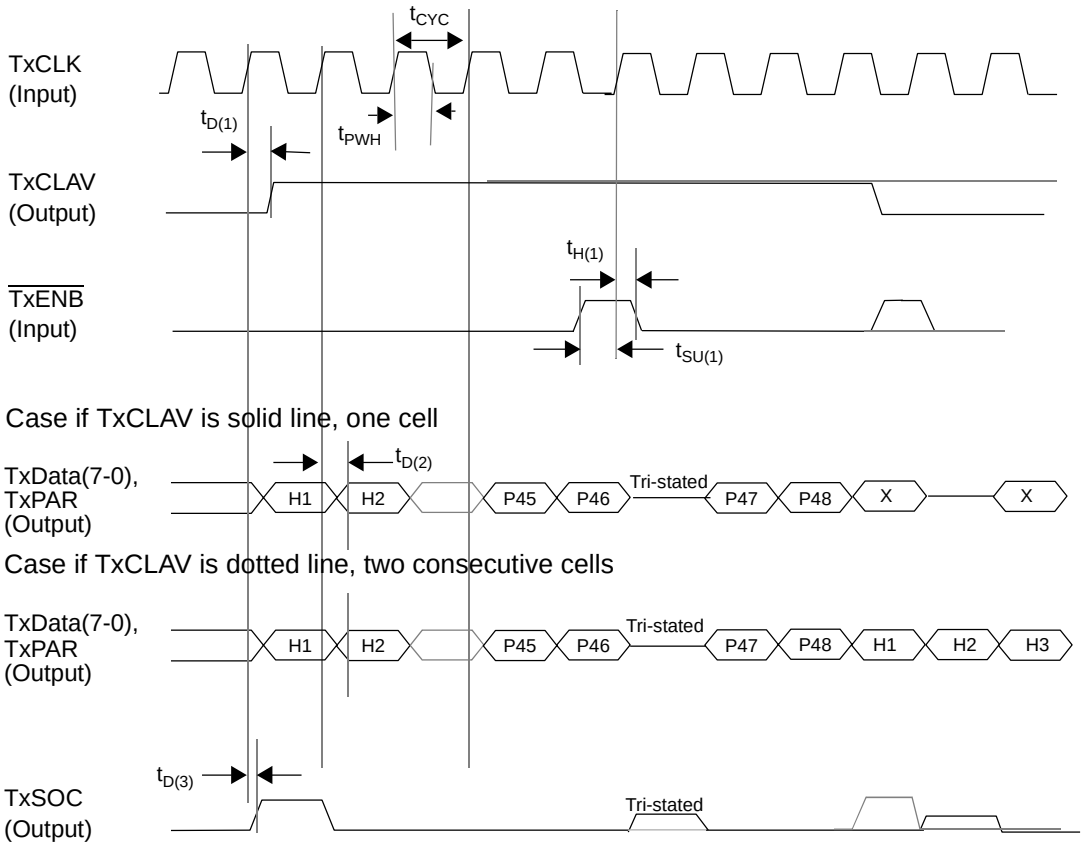
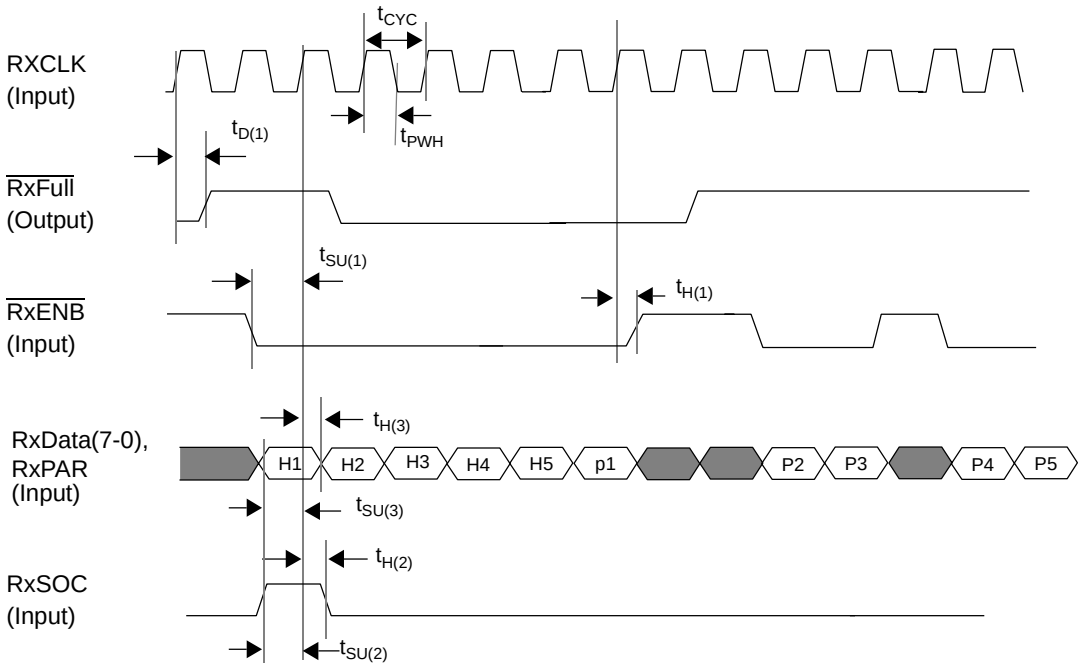
Parameter	Symbol	Min	Typ	Max	Unit
RxCLK clock period	t_{CYC}	40			ns
RxCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
RxCLAV delay from RxCLK↑	$t_{D(1)}$	7.0		19	ns
$\overline{\text{RxENB}}$ setup time before RxCLK↑	$t_{SU(1)}$	4.0			ns
$\overline{\text{RxENB}}$ hold time after RxCLK↑	$t_{H(1)}$	2.0			ns
RxSOC setup time before RxCLK↑	$t_{SU(2)}$	4.0			ns
RxSOC hold time after RxCLK↑	$t_{H(2)}$	3.0			ns
RxData(7-0) and RxPAR setup time before RxCLK↑	$t_{SU(3)}$	4.0			ns
RxData(7-0) and RxPAR hold time after RxCLK↑	$t_{H(3)}$	2.0			ns

Figure 21. Cell Transmit Timing - Cell Level Handshake for UTOPIA-PHY Mode



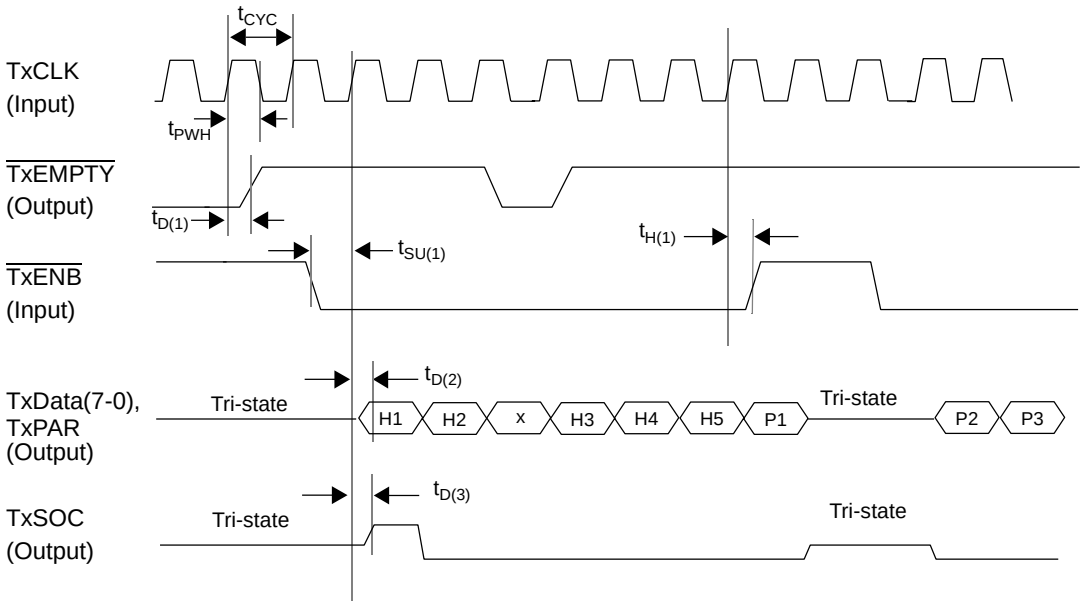
Parameter	Symbol	Min	Typ	Max	Unit
TxCLK clock period	t_{CYC}	40			ns
TxCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
TxCLAV delay after TxCLK↑	$t_{D(1)}$	6.0		21	ns
$\overline{\text{TxENB}}$ setup time before TxCLK↑	$t_{SU(1)}$	3.0			ns
$\overline{\text{TxENB}}$ hold time after TxCLK↑	$t_{H(1)}$	3.0			ns
TxData(7-0) and TxPAR delay after TxCLK↑	$t_{D(2)}$	7.0		24	ns
TxSOC delay after TxCLK↑	$t_{D(3)}$	7.0		22	ns

Figure 22. Cell Receive Timing - Octet Level Handshake for UTOPIA-PHY Mode



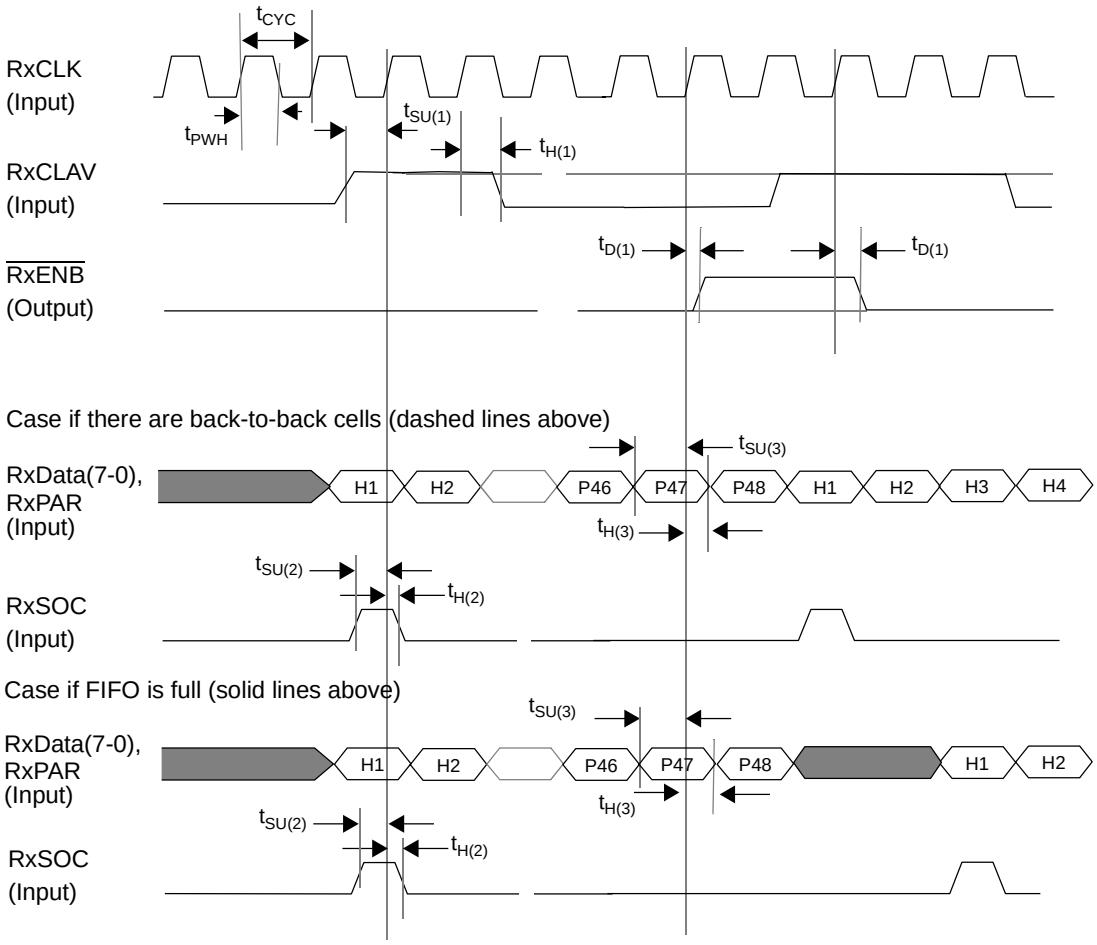
Parameter	Symbol	Min	Typ	Max	Unit
RxCLK clock period	t_{CYC}	40			ns
RxCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{RxFULL}}$ delay time after RxCLK↑	$t_{D(1)}$	9.0		22	ns
$\overline{\text{RxENB}}$ setup time before RxCLK↑	$t_{SU(1)}$	4.0			ns
$\overline{\text{RxENB}}$ hold time after RxCLK↑	$t_{H(1)}$	3.0			ns
RxSOC setup time before RxCLK↑	$t_{SU(2)}$	4.0			ns
RxSOC hold time after RxCLK↑	$t_{H(2)}$	3.0			ns
RxData(7-0) and RxPAR setup time before RxCLK↑	$t_{SU(3)}$	4.0			ns
RxData(7-0) and RxPAR hold time after RxCLK↑	$t_{H(3)}$	2.0			ns

Figure 23. Cell Transmit Timing - Octet Level Handshake for UTOPIA-PHY Mode



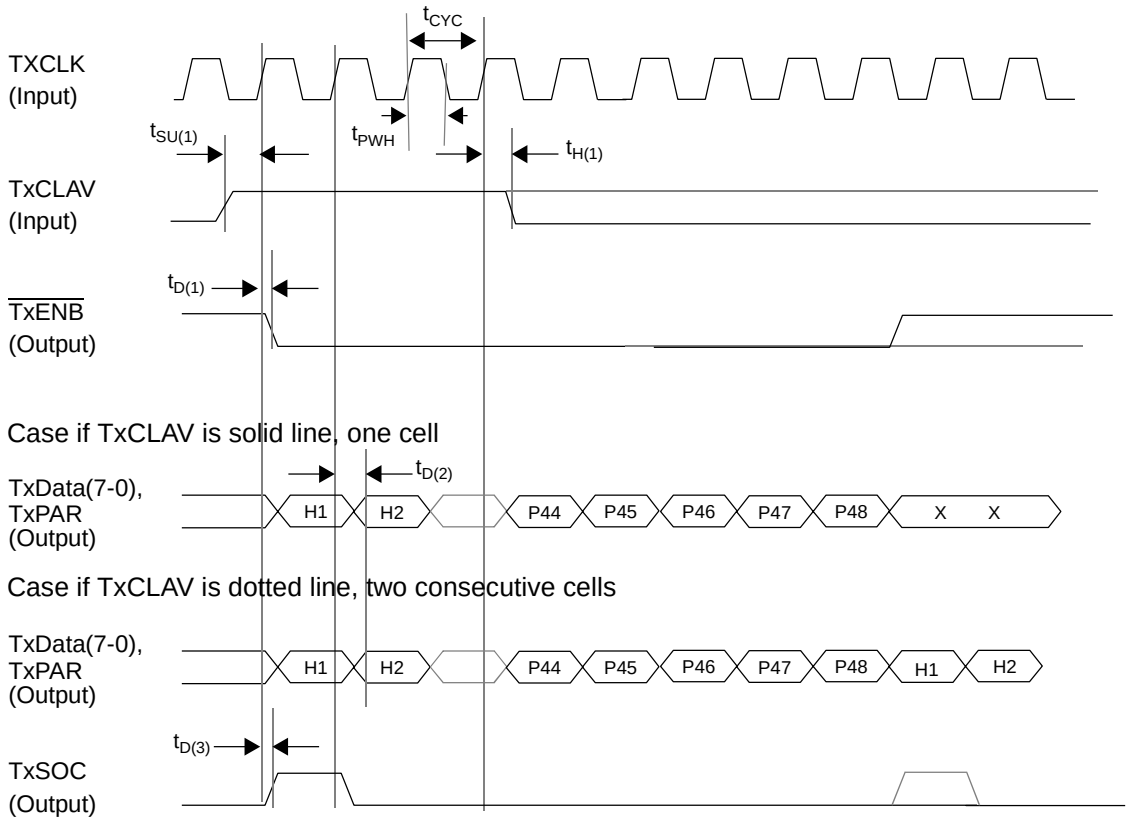
Parameter	Symbol	Min	Typ	Max	Unit
TxCLK clock period	t_{CYC}	40			ns
TxCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{TxEMPTY}}$ delay time after TxCLK↑	$t_{D(1)}$	8.0		24	ns
$\overline{\text{TxENB}}$ setup time before TxCLK↑	$t_{SU(1)}$	3.0			ns
$\overline{\text{TxENB}}$ hold time after TxCLK↑	$t_{H(1)}$	3.0			ns
TxData(7-0) and TxPAR delay time after TxCLK↑	$t_{D(2)}$	8.0		27	ns
TxSOC delay time after TxCLK↑	$t_{D(3)}$	8.0		25	ns

Figure 24. Cell Receive Timing - Cell Level Handshake for UTOPIA-ATM Mode



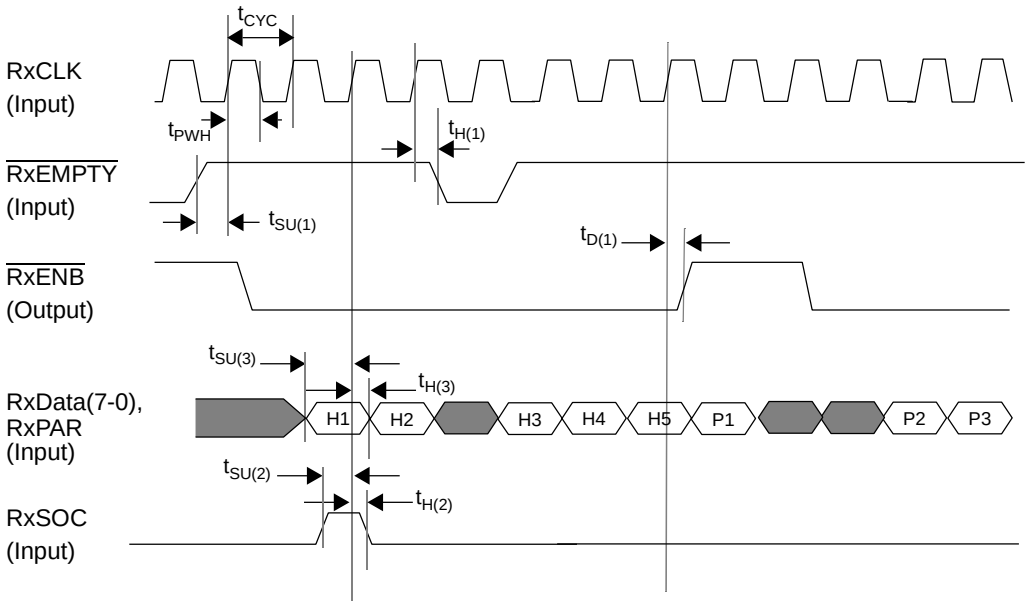
Parameter	Symbol	Min	Typ	Max	Unit
RxCLK clock period	t_{CYC}	40			ns
RxCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
RxCLAV setup time before RxCLK↑	$t_{SU(1)}$	3.0			ns
RxCLAV hold time after RxCLK↑	$t_{H(1)}$	3.0			ns
$\overline{\text{RxENB}}$ delay after RxCLK↑	$t_{D(1)}$	9.0		24	ns
RxSOC setup time before RxCLK↑	$t_{SU(2)}$	3.0			ns
RxSOC hold time after RxCLK↑	$t_{H(2)}$	3.0			ns
RxData(7-0) and RxPAR setup time before RxCLK↑	$t_{SU(3)}$	3.0			ns
RxData(7-0) and RxPAR hold time after RxCLK↑	$t_{H(3)}$	2.0			ns

Figure 25. Cell Transmit Timing - Cell Level Handshake for UTOPIA-ATM Mode



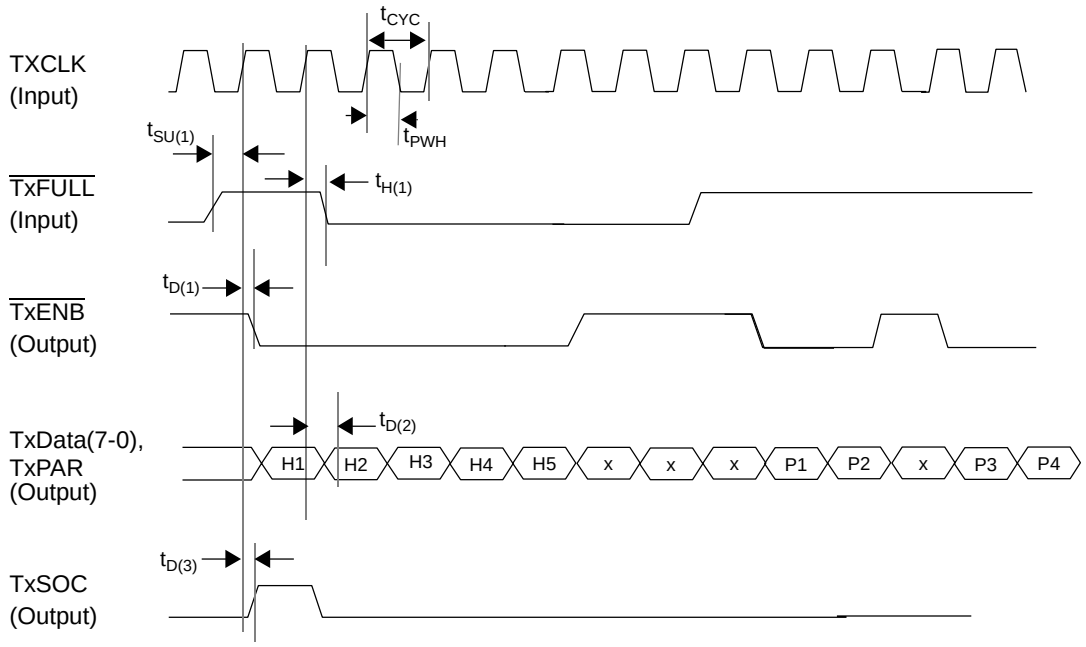
Parameter	Symbol	Min	Typ	Max	Unit
TxCLK clock period	t_{CYC}	40			ns
TxCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
TxCLAV setup time before TxCLK↑	$t_{SU(1)}$	3.0			ns
TxCLAV hold time after TxCLK↑	$t_{H(1)}$	3.0			ns
$\overline{\text{TxENB}}$ delay after TxCLK↑	$t_{D(1)}$	9.0		24	ns
TxData(7-0) and TxPAR delay after TxCLK↑	$t_{D(2)}$	8.0		28	ns
TxSOC delay after TxCLK↑	$t_{D(3)}$	3.0		23	ns

Figure 26. Cell Receive Timing - Octet Level Handshake for UTOPIA - ATM Mode



Parameter	Symbol	Min	Typ	Max	Unit
RxCLK clock period	t_{CYC}	40			ns
RxCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{RxEMPTY}}$ setup time before RxCLK↑	$t_{SU(1)}$	3.0			ns
$\overline{\text{RxEMPTY}}$ hold time after RxCLK↑	$t_{H(1)}$	3.0			ns
$\overline{\text{RxENB}}$ delay after RxCLK↑	$t_{D(1)}$	9.0		24	ns
RxSOC setup time before RxCLK↑	$t_{SU(2)}$	3.0			ns
RxSOC hold time after RxCLK↑	$t_{H(2)}$	3.0			ns
RxData(7-0) and RxPAR setup time before RxCLK↑	$t_{SU(3)}$	3.0			ns
RxData(7-0) and RxPAR hold time after RxCLK↑	$t_{H(3)}$	2.0			ns

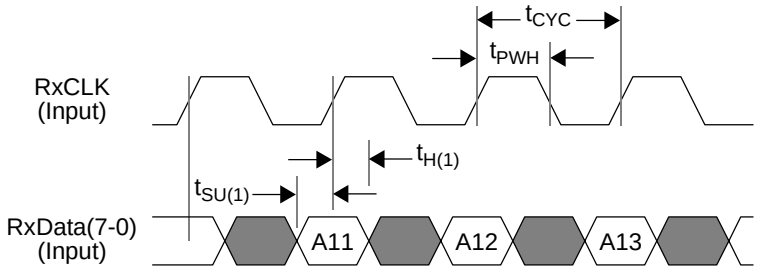
Figure 27. Cell Transmit Timing - Octet Level Handshake for UTOPIA-ATM Mode



Parameter	Symbol	Min	Typ	Max	Unit
TxCLK clock period	t_{CYC}	40			ns
TxCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{TxFULL}}$ setup time before TxCLK↑	$t_{SU(1)}$	3.0			ns
$\overline{\text{TxFULL}}$ hold time after TxCLK↑	$t_{H(1)}$	3.0			ns
$\overline{\text{TxENB}}$ delay after TxCLK↑	$t_{D(1)}$	9.0		24	ns
TxData(7-0) and TxPAR delay after TxCLK↑	$t_{D(2)}$	8.0		28	ns
TxSOC delay after TxCLK↑	$t_{D(3)}$	8.0		23	ns

Line Input/Output Byte-Parallel Framer Mode

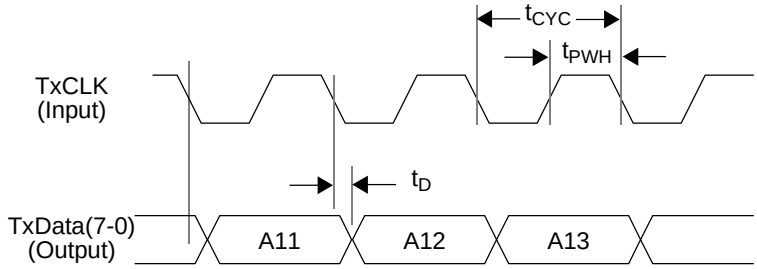
Figure 28. Byte-Parallel Receive Line Interface Timing



Note 1: Shown with RCS = 0; Data is clocked in on the opposite edge when RCS = 1.

Parameter	Symbol	Min	Typ	Max	Unit
Clock frequency	$1/t_{CYC}$	6.48-20 ppm		19.44+20 ppm	MHz
Clock duty cycle	t_{PWH}/t_{CYC}	40		60	%
RxData(7-0) set-up time to RxCLK↑	$t_{SU(1)}$	4			ns
RxData(7-0) hold time after RxCLK↑	$t_{H(1)}$	5			ns

Figure 29. Byte-Parallel Transmit Line Interface Timing

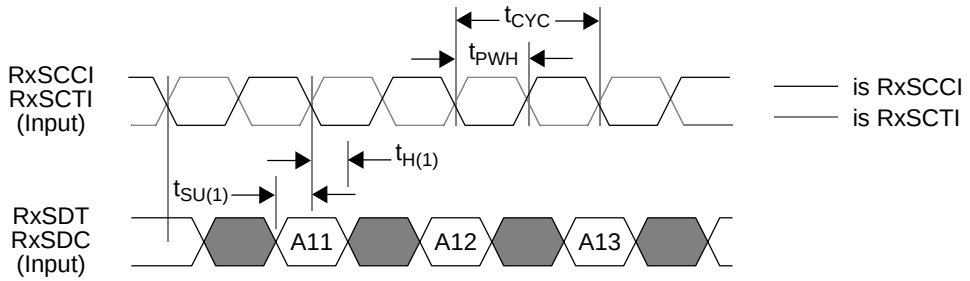


Note 1: Shown with TCS = 1; Data is clocked out on the opposite edge when TCS = 0

Parameter	Symbol	Min	Typ	Max	Unit
Clock frequency	$1/t_{CYC}$	6.48-20 ppm		19.44+20 ppm	MHz
Clock duty cycle	t_{PWH}/t_{CYC}	40		60	%
TxData(7-0) delay after TxCLK↓	t_D			25	ns

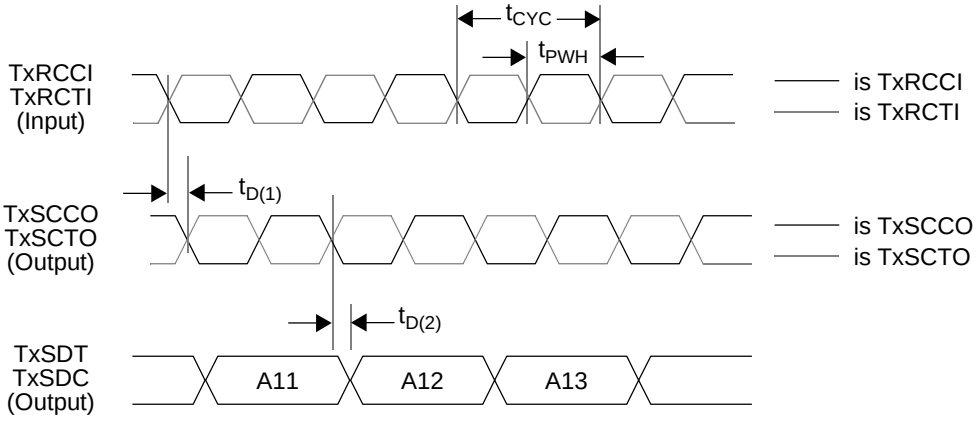
Line Input/Output Bit-Serial Framer Mode

Figure 30. Bit-Serial Receive Line Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
Clock frequency	$1/t_{CYC}$	51.48-20 ppm	155.52	155.52+20 ppm	MHz
Clock duty cycle	t_{PWH}/t_{CYC}	40		60	%
RxSDT/RxSDC set-up time to RxSCTI↑	t_{SU}	1.0			ns
RxSDT/RxSDC hold time after RxSCTI↑	t_H	1.0			ns

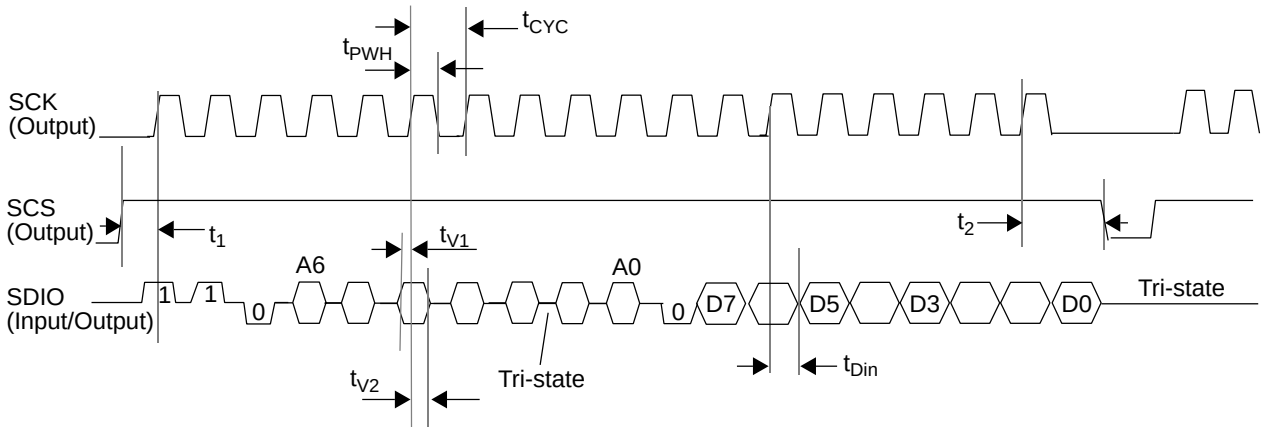
Figure 31. Bit-Serial Transmit Line Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
Clock frequency	$1/t_{CYC}$	51.48-20 ppm	155.52	155.52+20 ppm	MHz
Clock duty cycle	t_{PWH}/t_{CYC}	40		60	%
Clock delay after TxRCTI↑	$t_{D(1)}$	2.0		6.0	ns
Data delay after TxSCTO↑	$t_{D(2)}$	1.0		4.0	ns

SERIAL EEPROM INTERFACE

Figure 32. Read Instruction Timing for Serial EEPROM Interface



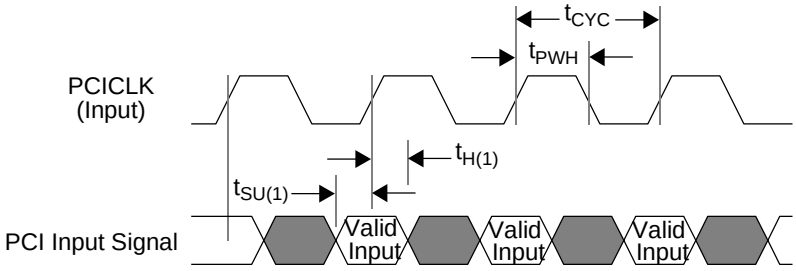
Parameter	Symbol	Min	Typ	Max	Unit
SCK clock period	t_{CYC}		36		Note 1
SCK pulse width high time	t_{PWH}		8.0		Note 1
Delay from SCS asserted to first SCK↑ output	t_1		35		Note 1
Delay from last SCK↑ to SCS deasserted	t_2		37		Note 1
SDIO output becomes valid before SCK↑	t_{V1}		4.0		Note 1
SDIO output remains valid after SCK↑	t_{V2}		4.0		Note 1
SDIO input delay after SCK↑	t_{Din}	0.0		34	Note 1

Note 1: All values are in units of PCICLK periods.

PCI INTERFACE

PCI Input Signals Timing

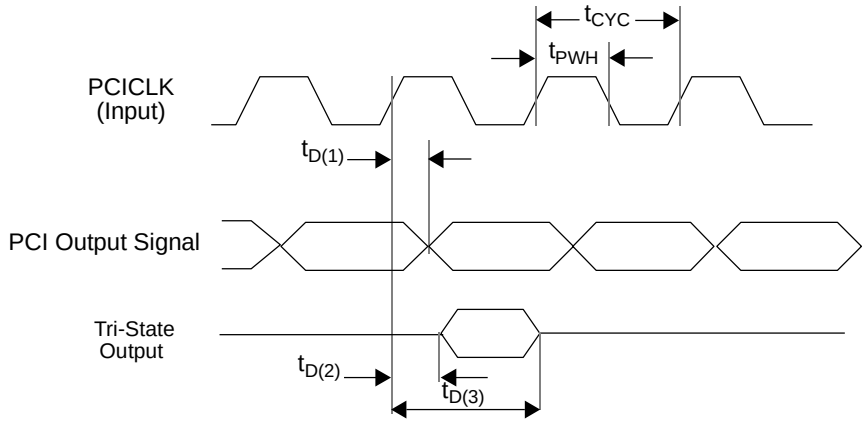
Figure 33. PCI Signals Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
PCICLK clock period	t_{CYC}	30			ns
Clock duty cycle	t_{PWH}/t_{CYC}	40		60	%
Set-up time from valid input to PCICLK↑	$t_{SU(1)}$	7.0			ns
Valid input hold time after PCICLK↑	$t_{H(1)}$	0.0			ns

PCI Output Signals Timing

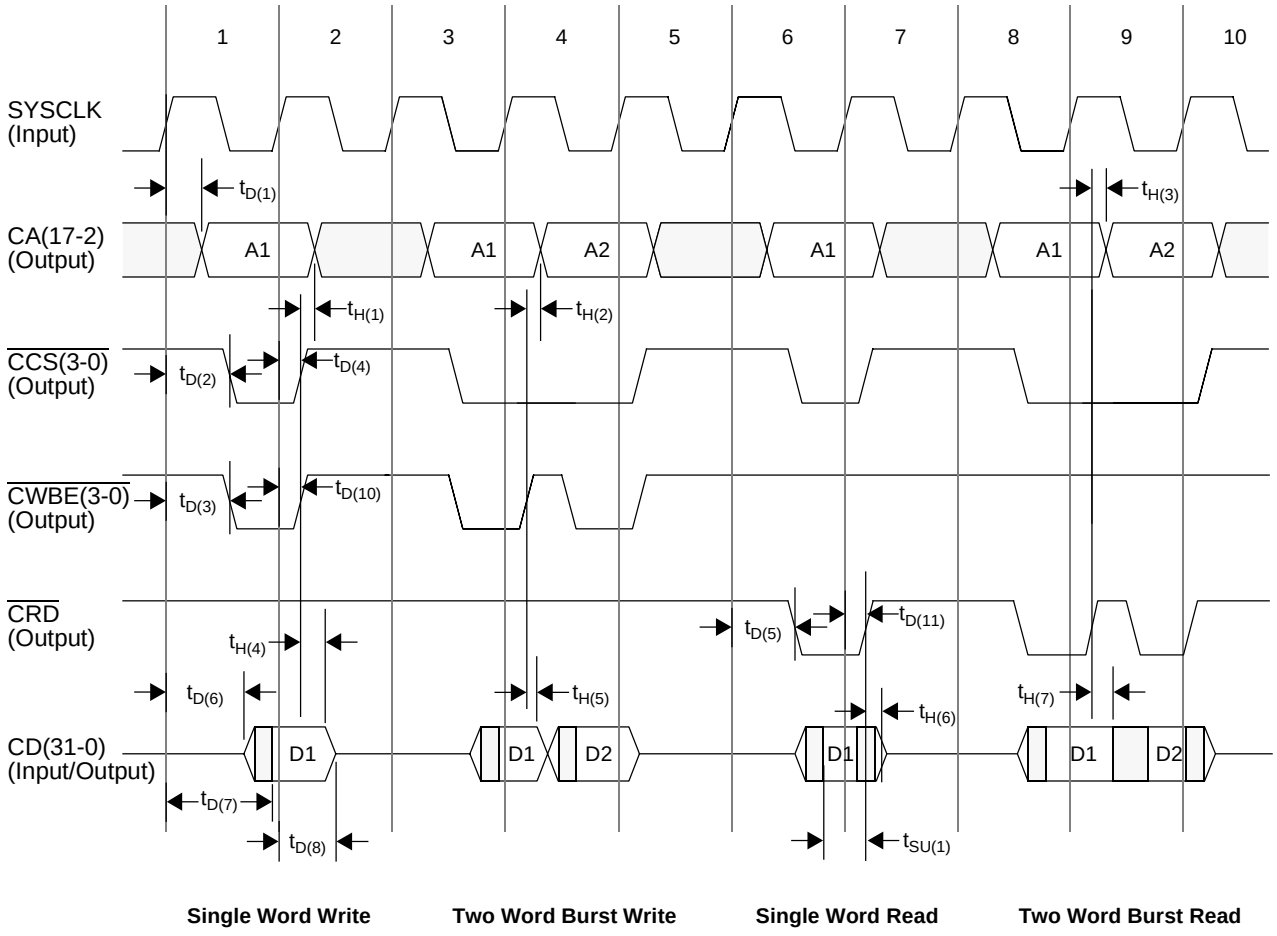
Figure 34. PCI Signals Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
PCICLK clock period	t_{CYC}	30			ns
Clock duty cycle	t_{PWH}/t_{CYC}	40		60	%
Output signal delay time after PCICLK↑	$t_{D(1)}$	2.0		11	ns
Tri-state output delay time from Hi-Z to active level after PCICLK↑	$t_{D(2)}$	2.0			ns
Tri-state output delay time from active level to Hi-Z after PCICLK↑	$t_{D(3)}$			28	ns

CONTROL MEMORY INTERFACE

Figure 35. Control Memory Read/Write Timing



Notes:
(1) Access is to bank "i". $\overline{CCS(i)}$ toggles as shown above while all other $\overline{CCS(3\text{-}0)}$ remain deasserted.
(2) Parameter values are shown in table on next page.

PRODUCT PREVIEW

Parameter	Symbol	Min	Typ	Max	Unit
SYSCLK clock period	t_{CYC}	20			ns
SYSCLK clock duty cycle	t_{PWH}/t_{CYC}	40		60	%
CA(17-2) delay from SYSCLK↑	$t_{D(1)}$	2.0		11	ns
$\overline{CCS(3-0)}$↓ delay after SYSCLK↑	$t_{D(2)}$	3.0		11	ns
$\overline{CCS(3-0)}$↑ delay after SYSCLK↑	$t_{D(4)}$	3.0		11	ns
$\overline{CWBE(3-0)}$↓ delay after SYSCLK↑	$t_{D(3)}$	2.0		9.0	ns
$\overline{CWBE(3-0)}$↑ delay after SYSCLK↑	$t_{D(10)}$	2.0		9.0	ns
$\overline{CRD}$↓ delay after SYSCLK↑	$t_{D(5)}$	5.0		16	ns
$\overline{CRD}$↑ delay after SYSCLK↑	$t_{D(11)}$	3.0		10	ns
CD(31-0) from Hi-Z to active delay after SYSCLK↑	$t_{D(6)}$	2.0		10	ns
CD(31-0) valid delay after SYSCLK↑	$t_{D(7)}$	3.0		16	ns
CD(31-0) active to Hi-Z delay after SYSCLK↑	$t_{D(8)}$	2.0		16	ns
CA(17-2) hold time after $\overline{CWBE}$↑	$t_{H(1)}$, $t_{H(2)}$	1.0			ns
CA(17-2) hold time after $\overline{CRD}$↑	$t_{H(3)}$	0.0			ns
CD(31-0) hold time after $\overline{CWBE}$↑	$t_{H(4)}$, $t_{H(5)}$	5.0			ns
CD(31-0) hold time after $\overline{CRD}$↑	$t_{H(6)}$, $t_{H(7)}$	3.0			ns
CD(31-0) set-up time before $\overline{CRD}$↑	$t_{SU(1)}$	0			ns

APPLICATIONS

ATM ACCESS HUB

The SARA-2 is typically used to implement the core functions of an ATM adapter card/hub/router by which LAN traffic is linked to an ATM switching system. In the application shown in Figure 36, the SARA-2 segments and reassembles packets directly in the packet data memory in which the LAN packets are stored. The figure also shows other TranSwitch products that may be used to build an ATM access switch connecting different types of traffic - LAN traffic segmented using SARA-2, or connection to an ATM network via an ALI-25/SALI-25 chip set using 25.6 Mbit/s ATM over category 3 wiring. The CUBIT device provides flexible ATM cell switching across a 32-bit bus called *CellBus.*

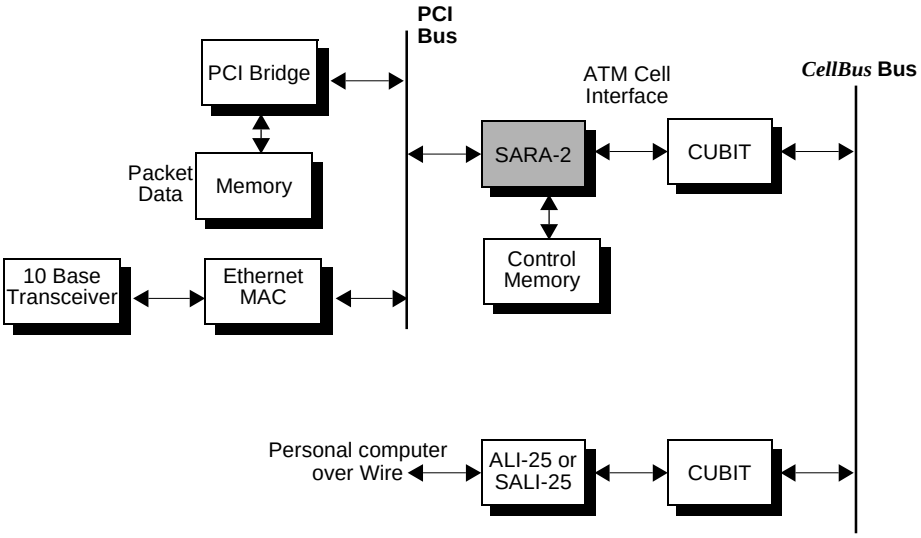


Figure 36. SARA-2 in an ATM Access Hub Application

ATM NETWORK INTERFACE CARD

The SARA-2 is a highly cost-effective solution for a PCI Network Interface Card (NIC) that provides high-performance connectivity to workstations and servers based on the PCI bus. The integrated SONET/SDH framer facilitates a NIC implementation with very few components, as shown in Figure 37.

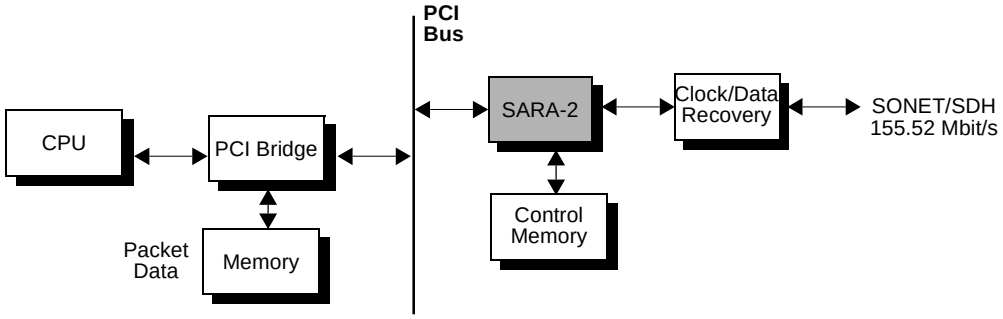
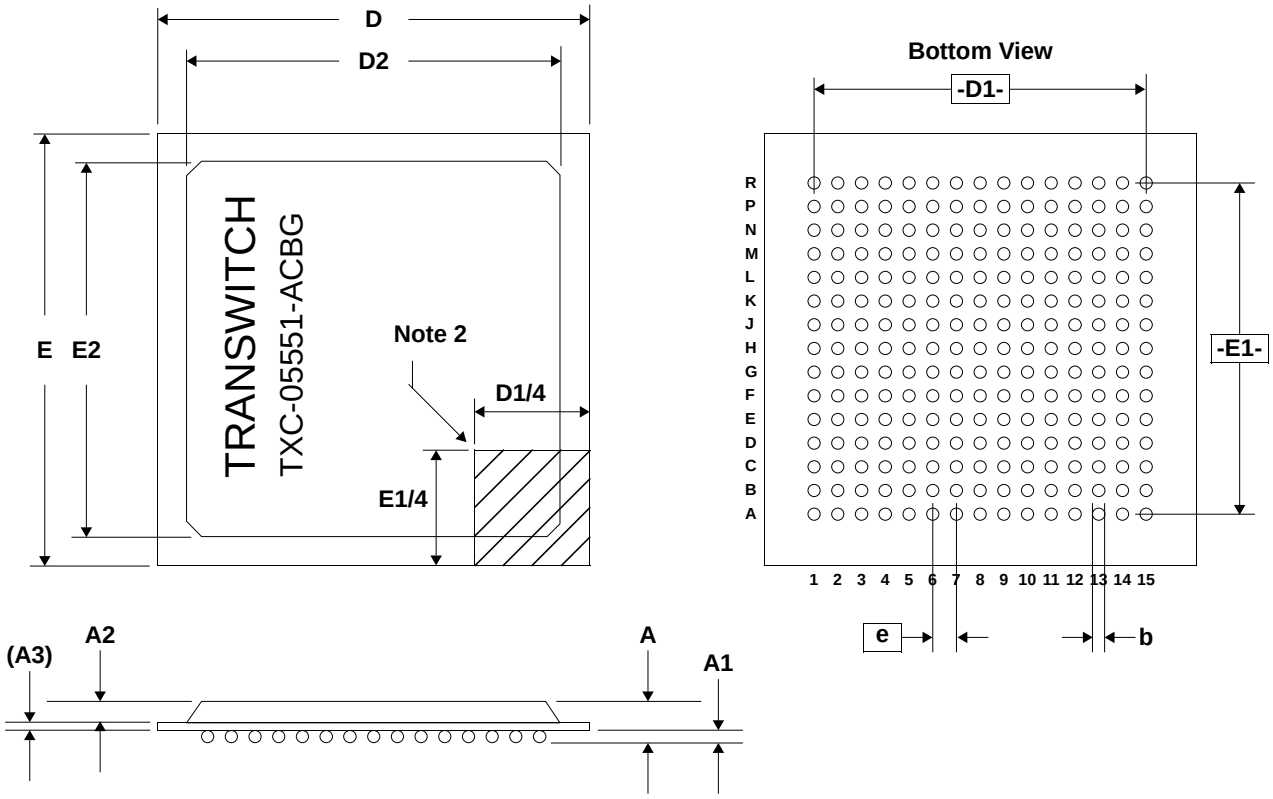


Figure 37. SARA-2 in an ATM Network Interface Card (NIC) Application

PRODUCT PREVIEW

PACKAGE INFORMATION

The SARA-2 device is packaged in a 225-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 38.



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.
3. Size of array: 15 x 15, JEDEC code MO-151-CAL-2.

Dimension (Note 1)	Min	Max
A	2.00	2.30
A1	0.50	0.70
A2	1.15	1.25
A3 (Ref.)	0.36	
b	0.60	0.90
D	26.50	27.50
D1 (BSC)	21.00	
D2	23.00	25.00
E	26.50	27.50
E1 (BSC)	21.00	
E2	23.00	25.00
e (BSC)	1.50	

Figure 38. SARA-2 TXC-05551 225-Lead Plastic Ball Grid Array Package

PRODUCT PREVIEW

ORDERING INFORMATION

VLSI Device

Part Number: TXC-05551-ACBG 225-lead plastic ball grid array package

SARA-*Lite*™ Microcode

The SARA-2 device is intended to be used in conjunction with microcode for its integral RISC CPU core that provides a specific functionality to the device. The first microcode introduced by TranSwitch provides the SARA-*Lite* functionality. For information on this SARA-*Lite* Microcode, please refer to the SARA-*Lite* Product Summary document, number TXC-05551-SCDA-PS1.

RELATED PRODUCTS

Related TranSwitch devices are briefly described below:

TXC-05150, CDB VLSI Device (Cell Delineation Block). Extracts/inserts ATM cells from/to DS1, DS3, E1, STS-1, STS-3c or STM-1 line interface signals. Serial, byte and nibble interfaces operate from 1.544 to 155.52 Mbit/s.

TXC-05801, CUBIT Device (ATM *CellBus* Bus Switch). Implements cost effective ATM multiplexing and switching systems, based on the 32-bit *CellBus* bus architecture. A single-chip solution, the CUBIT has the ability to send and also receive cells for control purposes over the same *CellBus* bus. *CellBus* bus technology works at aggregate rates of up to 1 gigabit per second and provides header translation, multiplexing, concentration and switching functions for a wide variety of small-to-medium size ATM systems.

TXC-05802, CUBIT-*Pro* VLSI Device. A *CellBus*-based ATM cell switching device that supports unicast and multicast transfers, and has all necessary functions for implementing a switch: inlet queuing, cell address translation, cell routing, and outlet cell queuing. This is a successor to the CUBIT device that has enhanced capabilities.

TXC-07025, ALI-25 VLSI Chip Set (ATM Line Interface). Controller and Transceiver devices together provide the complete ATM 25 Mbit/s physical layer function (TC, PMD) and operate over existing STP or UTP-3, 4, 5 cable plant.

TXC-07625, SALI-25C VLSI Device (Six ATM Line Interface at 25 Mbit/s). Six channel 25.6 Mbit/s ATM transmission convergence function for twisted pair cable. Supports UTOPIA Level 1 and 2. Provides multicasting capability and 4 level priority queuing.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum (U.S.A.):

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ETSI (Europe):

European Telecommunications Standards Institute
ETSI, 06921 Sophia - Antipolis
Cedex France

Tel: 33 92 94 42 00
Fax: 33 93 65 47 16

IEEE (U.S.A.)

The Institute of Electrical and Electronics Engineers, Inc.
Customer Service Department
445 Hoes Lane
P. O. Box 1331
Piscataway, NJ 08855-1331
Tel: 800-7014333 (In U.S.A.)
Tel: 908-981-0060
Fax: 908-981-9667

ITU-TSS (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (TSS)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk
700 Robbins Avenue
Building 4D
Philadelphia, PA 19111-5094

Tel: 212-697-1187
Fax: 215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
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LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated SARA-2 Data Sheet that have significant differences relative to the previous and now superseded SARA-2 Data Sheet:

Updated SARA-2 Data Sheet: *PRODUCT PREVIEW* Edition 4, January 1998

Previous SARA-2 Data Sheet: *PRODUCT PREVIEW* Edition 3, September 1997

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date, added ® to SARA in page headings.
Where Applicable	Changed TranSwitch street address in Shelton, CT.
Where Occurs	Changed ABR to UBR.
Where Occurs	Changed 'via a Service Interface request' to 'via a Service Interface request (using Request Primitive "Get Stats")'.
Where Occurs	Changed SARA-2 Service Interface documentation to SARA-*Lite* Service Interface Technical Manual.
Where Occurs	Changed TXC-05551-SCBB-FD to TXC-05551-TM1.
1	Added first item to Features column and deleted ABR from twelfth item. Made changes to Description column and diagram.
2-3	Updated Table of Contents and List of Figures.
4	Modified first and second paragraphs.
7	Deleted last sentence of sixth paragraph.
10	Changed Name/Function for Symbol $\overline{\text{RESET}}$
21	Changed OAM/RM to OAM and deleted last sentence in second paragraph. Deleted MCR and associated text in last paragraph.
22	Deleted the fourth through last sentence of the first paragraph.
33	Changed Available to Unspecified and added AAL0 in last paragraph.
45	Changed Bit 3: RR0INT to RR1INT, Bit 2: RR1INT to RR0INT, Bit 1: IR0INT to IR1INT and Bit 0: IR1INT to IR0INT. Added last sentence in description of Bit 15: RESET.
46	Changed Bit 3: ERR0INT to ERR1INT, Bit 2: ERR1INT to ERR0INT, Bit 1: EIR0INT to EIR1INT and Bit 0: EIR1INT to EIR0INT.

Page Number of Updated Data Sheet	Summary of the Change
49	Deleted fifth paragraph and added Note.
54	Changed mode register 0 to mode register 2 in first paragraph.
55	Modified Figure 12.
56	Changed OAM_RM to OAM in first paragraph. In "BurstSize/CNT_Nrm" description, removed reference to CNT_Nrm, and removed second paragraph.
57	Deleted second and third paragraph. Deleted out-of-rate RM cell from fourth paragraph.
58	Deleted text pertaining to MCR in second paragraph. Deleted second and third sentence in last paragraph.
82	Added TRANSWITCH and TXC-05551-ACBG to top view of package in Figure 38
83	Added microcode information to Ordering Information.
86 - 87	Updated List of Data Sheet Changes.
91	Updated Documentation Update Registration Form.

- NOTES -

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PRODUCT PREVIEW

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